Abstract

TRIPLE POLYSILICON EMBEDDED NVRAM CELL AND METHOD THREOF

A logic chip including a non-volatile random access memory (NVRAM) array and method of fabrication thereof. The chip includes devices with gates (162, 164, 174, 176) on one or more of three polysilicon layers (158, 144, 148). Chip logic uses normal FETs and array support includes high voltage FETs (174, 176). Both logic and support are CMOS. The gates (162, 164) of normal FETs in the chip logic are from the third, uppermost polysilicon layer (158). The third polysilicon layer (158) also is used as a mask for high voltage FETs (174, 176) and array word lines (180w, 182w), both of which use the second polysilicon layer (148) for gates. The first polysilicon layer (144) is used solely for cell floating gates (180f, 182f).

Fig 1