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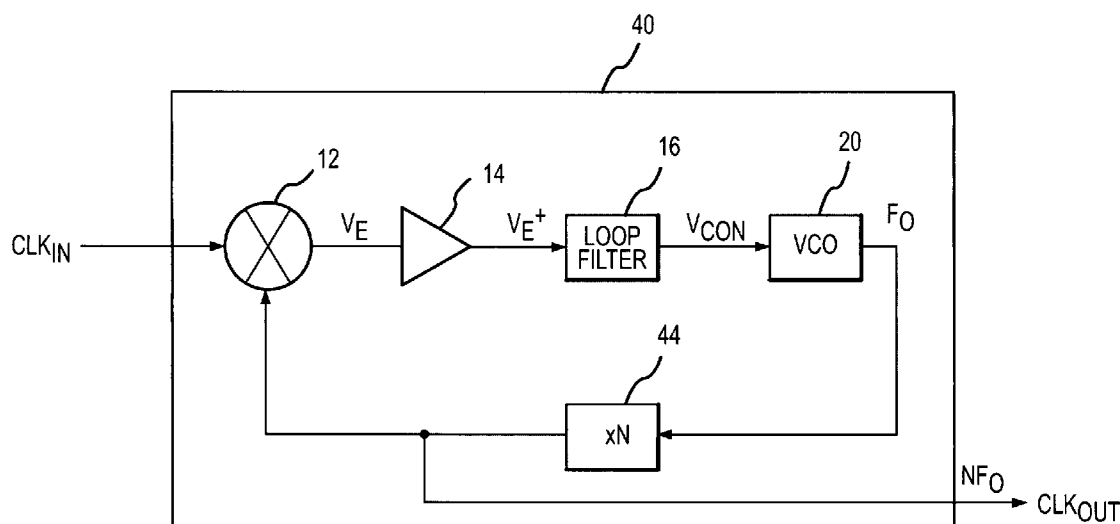
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(54) Title: LOW POWER AND LOW TIMING JITTER PHASE-LOCK LOOP AND METHOD



(57) Abstract: A phase-lock loop generates an output clock signal from an input clock signal. The output clock signal is coupled through a clock tree and is fed back to a phase detector, which compares the phase of the output clock signal to the phase of the input clock signal. The output clock signal is generated by a voltage controlled oscillator having a control input coupled to receive an output from the phase detector, and a frequency multiplier coupled to the output of the voltage controlled oscillator. As a result, the CLKOUT signal generated by the frequency multiplier has a relatively high frequency while the voltage controlled oscillator, by operating at a relatively low frequency, uses relatively little power.

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