CLAIMS

1. A process for fabricating a composite structure comprising a working layer made of single-crystal silicon carbide placed on a carrier substrate made of polycrystalline silicon carbide, the process comprising:

a) a step of providing an initial substrate made of polycrystalline silicon carbide, having a front side and comprising grains the average size of which, in the plane of said front side, is larger than 0.5 μm;

b) a step of forming a surface layer made of polycrystalline silicon carbide on the initial substrate, in order to form the carrier substrate, the surface layer being made up of grains the average size of which is smaller than 500 nm, and having a thickness comprised between 50 nm and 50 μm;

c) a step of preparing a free surface of the surface layer of the carrier substrate, in order to obtain a roughness lower than 1 nm RMS;

d) a step, based on molecular bonding, of transferring the working layer to the carrier substrate, the surface layer being positioned between the working layer and the initial substrate.

2. The fabricating process according to the preceding claim, wherein step a) is carried out using a chemical-vapour-deposition technique, at a temperature comprised between 1100°C and 1500°C.

3. The fabricating process according to Claim 1, wherein step a) is carried out using a sintering technique or using a physical-vapour-deposition technique.

4. The fabricating process according to one of the preceding claims, wherein step b) comprises depositing a layer made

of polycrystalline silicon carbide and is carried out using a chemical-vapour-deposition technique at a temperature lower than or equal to 1100°C, or even lower than or equal to 1000°C.

5. The fabricating process according to one of the preceding claims, wherein step b) is carried out in the same item of equipment as step a) and following the latter, without bringing the initial substrate back to ambient atmosphere.

6. The fabricating process according to one of Claims 1 to 3, wherein step b) comprises depositing a layer made of amorphous silicon carbide on the initial substrate and carrying out a recrystallization anneal, in order to form the surface layer made of polycrystalline silicon carbide.

7. The fabricating process according to one of the preceding claims, wherein the surface layer formed in step b) has a dopant concentration comprised between 1E18/cm^3 and 1E21/cm^3.

8. The fabricating process according to one of the preceding claims, wherein step c) comprises a chemical-mechanical polish of the surface layer, involving removal of an amount comprised between 1 and 10 times the average size of the grains making up said surface layer.

9. The fabricating process according to one of the preceding claims, wherein step d) comprises the following phases:

d1) providing a donor substrate;

d2) introducing light species into the donor substrate in order to form a buried weak plane delineating, with a front side of the donor substrate, the working layer to be transferred;

d3) joining the front side of the donor substrate to the carrier substrate, by molecular bonding;

d4) separating along the buried weak plane, leading to the transfer of the working layer to the carrier substrate.

10. The fabricating process according to claim 9, comprising forming a second surface layer, of the same nature as the surface layer, on the front side of the donor substrate, before or after the phase d2).

11. The fabricating process according to claim 9 or 10, wherein step d) comprises, before the joining phase d3), depositing an additional film made of a metal or of silicon on the surface layer of the carrier substrate and/or on the front side of the donor substrate.

12. A carrier substrate made of polycrystalline silicon carbide, comprising:

- an initial substrate comprising silicon-carbide grains, said grains having an average size larger than 0.5 μm,
- a surface layer placed at least on a front side of the initial substrate, comprising silicon-carbide grains the average size of which is smaller than 500 nm, and having a thickness comprised between 50 nm and 50 μm.

13. The carrier substrate according to claim 12, wherein a free surface of the surface layer has a roughness lower than 1 nm RMS and less than 1 defect/cm^2, as measured by reflected dark-field microscopy, with a threshold of 0.5 μm.

14. The carrier substrate according to claim 12 or 13, wherein the thickness of the surface layer is comprised between 200 nm and 5 μm.

15. The carrier substrate according to one of claims 12 to 14, wherein the surface layer has a dopant concentration comprised between 1E18/cm^3 and 1E21/cm^3.

16. A composite structure, comprising:
- the carrier substrate according to one of claims 12 to 15,
- a working layer made of single-crystal silicon carbide placed on the surface layer.

17. The composite structure according to claim 16, further comprising at least one power device on or in the working layer.