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<p>(21) International Application Number: PCT/US99/28410</p> <p>(22) International Filing Date: 30 November 1999 (30.11.99)</p> <p>(30) Priority Data: 09/201,270 30 November 1998 (30.11.98) US</p> <p>(63) Related by Continuation (CON) or Continuation-in-Part (CIP) to Earlier Application US 09/201,270 (CON) Filed on 30 November 1998 (30.11.98)</p> <p>(71) Applicant (for all designated States except US): EQUATOR TECHNOLOGIES, INC. [US/US]; Suite 900, 520 Pike Street, Seattle, WA 98101-4001 (US).</p> <p>(72) Inventor; and (75) Inventor/Applicant (for US only): ZHOU, Qinggang [CN/US]; 10306 Meridian Avenue North, #103, Seattle, WA 98133 (US).</p> <p>(74) Agents: SANTARELLI, Bryan, A. et al.; Graybeal Jackson Haley LLP, Suite 350, 155 108th Avenue Northeast, Bellevue, WA 98004 (US).</p>		<p>(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).</p> <p>Published <i>With international search report.</i></p>
<p>(54) Title: IMAGE PROCESSING CIRCUIT AND METHOD FOR REDUCING A DIFFERENCE BETWEEN PIXEL VALUES ACROSS AN IMAGE BOUNDARY</p> <div data-bbox="300 1205 1324 1601"> <pre> graph LR Input[IMAGE DATA FROM DECODER] --> 82 subgraph 82 [] 86[IMAGE STORAGE] --> 88[IMAGE PROCESSOR] end 88 --> 84 subgraph 84 [] 90[PROCESSED IMAGE STORAGE] --> 92[IMAGE DISPLAY] end 92 --> 82 </pre> </div> <p>(57) Abstract</p> <p>An image processing circuit (82) includes a processor (84) that receives at least a portion of an image including a boundary and first and second contiguous pixels disposed on opposite sides of the boundary, the first and second pixels having respective first and second pixel values. The processor generates a boundary value from the first and second pixel values, compares the boundary value to a comparison value, and reduces the difference between the first and second values if the boundary value has a specified relationship to the comparison value. For example, such a processing circuit can be used to reduce blockiness in an image that has undergone block-based digital compression.</p>		