CLAIMS

1. A microcontroller comprising:

a timer circuit;

a first register electrically connected to the timer circuit;

a CPU comprising a second register;

a controller; and

a power gate configured to supply power to the timer circuit, the first register, the CPU, the second register, and the controller,

wherein the microcontroller is capable of being:

a first mode, the first mode being a mode where the timer circuit, the first register, the CPU, the second register, and the controller operate;

a second mode, the second mode being a mode where the timer circuit, the first register, and the controller operate; and

a third mode, the third mode being a mode where the controller operates,

wherein the microcontroller is configured to shift from the first mode to one of the second and third modes by the CPU,

wherein the microcontroller is configured to shift from one of the second and third modes to the first mode by the controller, and

wherein the first register and the second register each comprises:

a first volatile memory; and

a first nonvolatile memory comprising a first transistor, wherein a channel formation region of the first transistor comprises a first oxide semiconductor layer.

2. The microcontroller according to claim 1,

wherein the CPU and the second register do not operate in the second mode, and

wherein the timer circuit, the first register, the CPU, and the second register do not operate in the third mode.

3. The microcontroller according to claim 1, further comprising:

an I/O port;

a third register electrically connected to the I/O port;

a comparator; and

a fourth register electrically connected to the comparator,

wherein the I/O port, the third register, the comparator, and the fourth register operate in the first mode, and do not operate in the second and third modes.

4. The microcontroller according to claim 1, further comprising:

an interrupt controller; and

a fifth register electrically connected to the interrupt controller,

wherein the interrupt controller and the fifth register operate in the first mode, and do not operate in the second and third modes.

5. The microcontroller according to claim 1, further comprising:

an interrupt controller; and

a fifth register electrically connected to the interrupt controller,

wherein the interrupt controller and the fifth register operate in the first mode, and do not operate in the second and third modes, and

wherein the fifth register comprises:

a second volatile memory; and

a second nonvolatile memory comprising a second transistor, wherein a channel formation region of the second transistor comprises a second oxide semiconductor layer.

6. The microcontroller according to claim 1, further comprising:

a RAM electrically connected to the CPU,

wherein the RAM comprising a third transistor, and

wherein a channel formation region of the third transistor comprises a third oxide semiconductor layer.

7. The microcontroller according to claim 1,

wherein the timer circuit is configured to output a signal at regular intervals, and

wherein the microcontroller is configured to shift from the second mode to the first mode by the controller in accordance with the signal supplied from the timer circuit.

8. The microcontroller according to claim 1,

wherein the first nonvolatile memory is configured to back up a data stored in the first volatile memory before power supply is stopped by the power gate, and

wherein the data backed up in the first nonvolatile memory is written into the first volatile memory in a case where power supply is started again by the power gate.

9. The microcontroller according to claim 1,

wherein the first oxide semiconductor layer comprises indium, gallium, and zinc.

10. A microcontroller comprising:

a timer circuit;

a first register electrically connected to the timer circuit;

a CPU comprising a second register;

a controller; and

a power gate configured to supply power to the timer circuit, the first register, the CPU, the second register, and the controller,

wherein the microcontroller is capable of being:

a first mode, the first mode being a mode where the timer circuit, the first register, the CPU, the second register, and the controller operate;

a second mode, the second mode being a mode where the timer circuit, the first register, and the controller operate; and

a third mode, the third mode being a mode where the controller operates,

wherein the microcontroller is configured to shift from the first mode to one of the second and third modes by the CPU,

wherein the microcontroller is configured to shift from one of the second and third modes to the first mode by the controller, and

wherein the first register and the second register each comprises:

a first volatile memory; and

a first nonvolatile memory comprising a first transistor and a fourth transistor, wherein a channel formation region of the first transistor comprises a first oxide semiconductor layer, and wherein a channel formation region of the fourth transistor comprises single crystal silicon.

11. The microcontroller according to claim 10,

wherein the CPU and the second register do not operate in the second mode, and

wherein the timer circuit, the first register, the CPU, and the second register do not operate in the third mode.

12. The microcontroller according to claim 10, further comprising:

an I/O port;

a third register electrically connected to the I/O port;

a comparator; and

a fourth register electrically connected to the comparator,

wherein the I/O port, the third register, the comparator, and the fourth register operate in the first mode, and do not operate in the second and third modes.

13. The microcontroller according to claim 10, further comprising:

an interrupt controller; and

a fifth register electrically connected to the interrupt controller,

wherein the interrupt controller and the fifth register operate in the first mode, and do not operate in the second and third modes.

14. The microcontroller according to claim 10, further comprising:

an interrupt controller; and

a fifth register electrically connected to the interrupt controller,

wherein the interrupt controller and the fifth register operate in the first mode, and do not operate in the second and third modes, and

wherein the fifth register comprises:

a second volatile memory; and

a second nonvolatile memory comprising a second transistor, wherein a channel formation region of the second transistor comprises a second oxide semiconductor layer.

15. The microcontroller according to claim 10, further comprising:

a RAM electrically connected to the CPU,

wherein the RAM comprising a third transistor, and

wherein a channel formation region of the third transistor comprises a third oxide semiconductor layer.

16. The microcontroller according to claim 10,

wherein the timer circuit is configured to output a signal at regular intervals, and

wherein the microcontroller is configured to shift from the second mode to the first mode by the controller in accordance with the signal supplied from the timer circuit.

17. The microcontroller according to claim 10,

wherein the first nonvolatile memory is configured to back up a data stored in the first volatile memory before power supply is stopped by the power gate, and

wherein the data backed up in the first nonvolatile memory is written into the first volatile memory in a case where power supply is started again by the power gate.

18. The microcontroller according to claim 10,

wherein the first oxide semiconductor layer comprises indium, gallium, and zinc.

Claims

1. A microcontroller comprising:

a timer circuit;

a first register electrically connected to the timer circuit;

a CPU comprising a second register;

a controller; and

a power gate configured to supply power to the timer circuit, the first register, the CPU, the second register, and the controller,

wherein the microcontroller is capable of being in:

a first mode, the first mode being a mode where the timer circuit, the first register, the CPU, the second register, and the controller operate;

a second mode, the second mode being a mode where the timer circuit, the first register, and the controller operate; and

a third mode, the third mode being a mode where the controller operates,

wherein the microcontroller is configured to shift from the first mode to one of the second and third modes by the CPU,

wherein the microcontroller is configured to shift from one of the second and third modes to the first mode by the controller, and

wherein the first register and the second register each comprises:

a first memory, wherein the first memory is a volatile memory; and

a second memory comprising a first transistor,

wherein a channel formation region of the first transistor comprises a first oxide semiconductor layer.

2. The microcontroller according to claim 1,

wherein the CPU and the second register do not operate in the second mode, and

wherein the timer circuit, the first register, the CPU, and the second register do

not operate in the third mode.

3. The microcontroller according to claim 1, further comprising:

an I/O port;

a third register electrically connected to the I/O port;

a comparator; and

a fourth register electrically connected to the comparator,

wherein the I/O port, the third register, the comparator, and the fourth register operate in the first mode, and do not operate in the second and third modes.

4. The microcontroller according to claim 1, further comprising:

an interrupt controller; and

a fifth register electrically connected to the interrupt controller,

wherein the interrupt controller and the fifth register operate in the first mode, and do not operate in the second and third modes.

5. The microcontroller according to claim 1, further comprising:

an interrupt controller; and

a fifth register electrically connected to the interrupt controller,

wherein the interrupt controller and the fifth register operate in the first mode, and do not operate in the second and third modes, and

wherein the fifth register comprises:

a third memory, wherein the third memory is a volatile memory; and

a fourth memory comprising a second transistor,

wherein a channel formation region of the second transistor comprises a second oxide semiconductor layer.

6. The microcontroller according to claim 1, further comprising:

a RAM electrically connected to the CPU,

wherein the RAM comprising a third transistor, and

wherein a channel formation region of the third transistor comprises a third oxide semiconductor layer.

7. The microcontroller according to claim 1,

wherein the timer circuit is configured to output a signal at regular intervals, and

wherein the microcontroller is configured to shift from the second mode to the first mode by the controller in accordance with the signal supplied from the timer circuit.

8. The microcontroller according to claim 1,

wherein the second memory is configured to back up a data stored in the first memory before power supply is stopped by the power gate, and

wherein the data backed up in the second memory is written into the first memory in a case where power supply is started again by the power gate.

9. The microcontroller according to claim 1,

wherein the first oxide semiconductor layer comprises indium, gallium, and zinc.

10. A microcontroller comprising:

a timer circuit;

a first register electrically connected to the timer circuit;

a CPU comprising a second register;

a controller; and

a power gate configured to supply power to the timer circuit, the first register, the CPU, the second register, and the controller,

wherein the microcontroller is capable of being in:

a first mode, the first mode being a mode where the timer circuit, the first register, the CPU, the second register, and the controller operate;

a second mode, the second mode being a mode where the timer circuit, the first register, and the controller operate; and

a third mode, the third mode being a mode where the controller operates,

wherein the microcontroller is configured to shift from the first mode to one of the second and third modes by the CPU,

wherein the microcontroller is configured to shift from one of the second and third modes to the first mode by the controller, and

wherein the first register and the second register each comprises:

a first memory, wherein the first memory is a volatile memory; and

a second memory comprising a first transistor and a fourth transistor,

wherein a channel formation region of the first transistor comprises a first oxide semiconductor layer, and

wherein a channel formation region of the fourth transistor comprises single crystal silicon.

11. The microcontroller according to claim 10,

wherein the CPU and the second register do not operate in the second mode, and

wherein the timer circuit, the first register, the CPU, and the second register do not operate in the third mode.

12. The microcontroller according to claim 10, further comprising:

an I/O port;

a third register electrically connected to the I/O port;

a comparator; and

a fourth register electrically connected to the comparator,

wherein the I/O port, the third register, the comparator, and the fourth register operate in the first mode, and do not operate in the second and third modes.

13. The microcontroller according to claim 10, further comprising:

an interrupt controller; and

a fifth register electrically connected to the interrupt controller,

wherein the interrupt controller and the fifth register operate in the first mode, and do not operate in the second and third modes.

14. The microcontroller according to claim 10, further comprising:

an interrupt controller; and

a fifth register electrically connected to the interrupt controller,

wherein the interrupt controller and the fifth register operate in the first mode, and do not operate in the second and third modes, and

wherein the fifth register comprises:

a third memory, wherein the third memory is a volatile memory; and

a fourth memory comprising a second transistor,

wherein a channel formation region of the second transistor comprises a second oxide semiconductor layer.

15. The microcontroller according to claim 10, further comprising:

a RAM electrically connected to the CPU,

wherein the RAM comprising a third transistor, and

wherein a channel formation region of the third transistor comprises a third oxide semiconductor layer.

16. The microcontroller according to claim 10,

wherein the timer circuit is configured to output a signal at regular intervals, and

wherein the microcontroller is configured to shift from the second mode to the first mode by the controller in accordance with the signal supplied from the timer circuit.

17. The microcontroller according to claim 10,

wherein the second memory is configured to back up a data stored in the first memory before power supply is stopped by the power gate, and

wherein the data backed up in the second memory is written into the first memory in a case where power supply is started again by the power gate.

18. The microcontroller according to claim 10, wherein the first oxide semiconductor layer comprises indium, gallium, and zinc.

19. The microcontroller according to claim 1, wherein the second memory is a nonvolatile memory.

20. The microcontroller according to claim 5, wherein the fourth memory is a nonvolatile memory.

21. The microcontroller according to claim 10, wherein the second memory is a nonvolatile memory.

22. The microcontroller according to claim 14, wherein the fourth memory is a nonvolatile memory.