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DESCRIPTION

POWER AMPLIFIER AND A TRANSMITTER INCLUDING THE POWER AMPLIFIER

5 The present invention relates to a power amplifier and to a transmitter and to a transceiver including such a power amplifier. The power amplifier is suitable for use in transmitters or transceivers operating in accordance with the ETSI interim standard for DCS 1800 (Personal Communications Network).

10 Time division duplex and time division multiple access protocols are frequently used in digital mobile and cordless communication systems in order to provide duplex channels on a single radio frequency carrier and in order to use a single rf carrier to provide many voice channels. One problem with such protocols is that as the radio frequency signal is switched on or off, the frequency spectrum of the signal momentarily widens which causes interference on adjacent radio frequency carriers. The momentary widening of the frequency spectrum is frequently known as "splatter".

15 In order to overcome or reduce this problem, the amplitude profile of the radio frequency carrier must be carefully shaped as the transmitter is switched on. This shaping is normally done in the power amplifier by coupling out a portion of the output signal, which after detection is compared with a reference signal and the difference is low pass filtered to form an "error" signal which is used to control the gain of the power amplifier. The reference signal which provides the shaping may be derived from a series of digital values which are read out from a ROM and which are applied to a digital to analogue converter. Such an arrangement is disclosed in Figure 5 of UK Patent Specification GB-A-2 220 808. Whilst such known arrangements function satisfactorily they are relatively costly and consume power which is a disadvantage with battery powered equipment.

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An object of the present invention is to simplify the amplitude profiling of the radio frequency carrier to avoid momentary widening of the frequency spectrum.

According to one aspect of the present invention there is provided a transceiver comprising transmitting means, receiving means and control means for controlling the operation of the transmitting and receiving means, the transmitting means comprising power amplifying means having an input for a signal to be amplified and an output for an output power signal and a control loop having means for sampling the output power signal, means for detecting the sampled output power signal, a reference control signal source, and means for comparing the detected sampled output power with the reference control signal, characterised in that the control loop further comprises means for integrating an output of the comparing means and low pass filtering means and in that there is provided multiplying means having first and second signal inputs and an output coupled to the input of the power amplifying means, a signal to be amplified being applied, in use, to the first signal input and the control loop being connected to the second input.

According to a second aspect of the present invention there is provided a transmitter comprising power amplifying means having an input for a signal to be amplified and an output for an output power signal and a control loop having means for sampling the output power signal, means for detecting the sampled output power signal, a reference control signal source, and means for comparing the detected sampled output power with the reference control signal, characterised in that the control loop further comprises means for integrating an output of the comparing means and low pass filtering means and in that there is provided multiplying means having first and second signal inputs and an output coupled to the input of the power amplifying means, a signal to be amplified being applied, in use, to the first signal input and the control loop being connected to the second input.

According to a third aspect of the present invention there

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is provided a power amplifier comprising power amplifying means having an input for a signal to be amplified and an output for an output power signal and a control loop having means for sampling the output power signal, means for detecting the sampled output power signal, a reference control signal source, and means for
5 comparing the detected sampled output power with the reference control signal, characterised in that the control loop further comprises means for integrating an output of the comparing means and low pass filtering means and in that there is provided multiplying means having first and second signal inputs and an
10 output coupled to the input of the power amplifying means, a signal to be amplified being applied, in use, to the first signal input and the control loop being connected to the second input.

By having a power control loop including a low pass filter, an integrator and a multiplier, the need for complex pulse
15 shaping circuitry to shape the reference waveform is avoided. The control loop used in conjunction with the power amplifying means is able to make use of a step-like reference waveform of a predetermined value. Shaping of the amplified waveform is partly
20 done in the integrating means which slows the output from the comparing means. The output from the integrating means is multiplied by the radio frequency input signal on the first input of the multiplying means which causes its output to rise slowly. The power amplifying means has sufficient linearity to assure
25 that the slowly rising waveform appears on its output.

The low pass filtering means may be coupled between an output of the integrating means and the second input to the multiplying means or between an output of the comparing means and the input to the integrating means. An advantage of locating the
30 low pass filtering means in either one of these positions is that it slows the integrated waveform so that the leading edge of the signal applied to the multiplying means rises gradually.

The present invention will now be described, by way of
35 example, with reference to the accompanying drawings, wherein:

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Figure 1 is a simplified block schematic diagram of a transceiver comprising the power amplifier in accordance with the first aspect of the present invention, and

Figure 2 shows waveforms occurring at different points in the circuit shown in Figure 1.

The transceiver shown in Figure 1 comprises a modulator 10 whose output is connected to a power amplifier circuit 12. An output of the power amplifier circuit 12 is connected to a duplexer 14 which is connected to an antenna 16 for transmitting the amplified signal.

A signal received at the antenna is coupled by way of the duplexer 14 to an r.f. section 18 of a receiver in which the signal is frequency down converted and applied to a demodulator 20.

The power amplifier circuit 12 comprises a linear power amplifier 22 having an input 24 and an output 26 coupled to the duplexer 14. A multiplier circuit 28 is provided having first and second inputs 30, 32 and an output 34. The first input 30 is connected to the modulator 10 and the output 34 is coupled to the amplifier input 24.

The amplifier circuit also includes a feedback control loop comprising a directional coupler 36 for coupling out a portion of the output from the power amplifier 22. A detector 38 is coupled to the directional coupler 36 for detecting the envelope of the output signal. A low pass filter 40 is connected to an output of the detector 38 and serves to remove wideband noise in the coupled out signal. The low pass filtered signal is applied to a non-inverting input of a comparator or differencing amplifier circuit 42. A reference or control signal source 44 is coupled to an inverting input of the differencing amplifier circuit 42. The control signal comprises a step function having a desired amplitude. An integrator 46 is coupled to an output of the amplifier circuit 42 for integrating the signal output of the amplifier circuit 42. An output of the integrator 46 is filtered

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in a low pass filter 48 and applied to the second input of the multiplier 28.

5 A controller 50 is provided for controlling the operation of the transceiver so that the transmitter and receiver sections are energised during the appropriate time slots of a TDMA frame and they are tuned to the required frequency if there are two or more channel frequencies available. The controller 50 is also responsible for setting dynamically the output power of the transmitter. Several methods are known per se. For example a
10 base station may send output power control messages to a portable/mobile unit and/or the transceiver may include means for obtaining a radio signal strength indication (RSSI) from a received signal and for adjusting its own output power in response. The reference or control signal source 44 may comprise
15 a store 52 for storing digitally a number of predetermined power levels and a digital to analogue converter 54 for converting the digital value read-out from the store 52 in response to a suitable signal from the controller 50 into a step-like control voltage. The control voltage supplied to the comparator 42 does
20 not have its leading and trailing edges shaped to conform to a predetermined envelope profile.

Referring to Figure 2, the waveform A comprises the power amplifier circuit output. It will be noted that the leading edge of the envelope rises gently somewhat like a raised cosine
25 waveform. Waveform B is the envelope of the coupled out signal after detection. Waveform C is the step-like control signal produced by the source 44. It should be noted that the duration of the control signal is less than that of the detected signal. Waveform D comprises the output of the difference amplifier
30 circuit 42. Finally waveform E comprises the output of the integrator 46. The step-like rising edge of the waveform D is slowed down by the integrator 46 and the low pass filter 48 thereby giving the desired profile to the leading edge of the waveform E without requiring special pulse shaping circuitry.

35 If desired the low pass filter 48 may be coupled between the

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output of the differencing amplifier circuit 42 and the input to the integrator 46, as shown in broken lines.

The multiplier 28 may comprise a four quadrant multiplier of a type described in the IEEE Journal of Solid State Circuits, Vol. SC-3, No. 4, December 1968, pages 365 to 372, "A Precise Four-Quadrant Multiplier with Subnanosecond Response" by Barrie Gilbert.

In the case of the power amplifier having to conform to the DCS 1800 specification, then in order for the control loop to meet section 05.05 of that specification, an integrator gain giving a loop time constant of $3.2\mu\text{s}$ could be used. Additionally the low pass filter 48 may comprise a second order Butterworth low pass filter with a cut off frequency of 200 kHz. Finally the multiplier 28 would require a 30 dB dynamic range.

From reading the present disclosure, other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the design, manufacture and use of transmitters, power amplifiers and component parts thereof and which may be used instead of or in addition to features already described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the disclosure of the present application also includes any novel feature or any novel combination of features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as does the present invention. The applicants hereby give notice that new claims may be formulated to such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

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CLAIMS

1. A transceiver comprising transmitting means, receiving means and control means for controlling the operation of the transmitting and receiving means, the transmitting means comprising power amplifying means having an input for a signal to be amplified and an output for an output power signal and a control loop having means for sampling the output power signal, means for detecting the sampled output power signal, a reference control signal source, and means for comparing the detected sampled output power with the reference control signal, characterised in that the control loop further comprises means for integrating an output of the comparing means and low pass filtering means and in that there is provided multiplying means having first and second signal inputs and an output coupled to the input of the power amplifying means, a signal to be amplified being applied, in use, to the first signal input and the control loop being connected to the second input.

2. A transceiver as claimed in claim 1, characterised in that the low pass filtering means is coupled between an output of the integrating means and the second signal input of the multiplying means.

3. A transceiver as claimed in claim 1, characterised in that the low pass filtering means is coupled between an output of the comparing means and an input to the integrating means.

4. A transceiver as claimed in any one of claims 1 to 3, characterised in that the reference control signal source comprises means for producing a step function of a predetermined amplitude.

5. A transceiver as claimed in any one of claims 1 to 4, characterised in that the multiplying means comprises a four-quadrant multiplier.

6. A transmitter comprising power amplifying means having an input for a signal to be amplified and an output for an output power signal and a control loop having means for sampling the output power signal, means for detecting the sampled output power signal, a reference control signal source, and means for comparing the detected sampled output power with the reference control



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signal, characterised in that the control loop further comprises means for integrating an output of the comparing means and low pass filtering means and in that there is provided multiplying means having first and second signal inputs and an output coupled to the input of the power amplifying means, a signal to be amplified being applied, in use, to the first signal input and the control loop being connected to the second input.

7. A transmitter as claimed in claim 6, characterised in that the low pass filtering means is coupled between an output of the integrating means and the second signal input of the multiplying means.

8. A transmitter as claimed in claim 6 or 7, characterised in that the reference control signal source comprises means for producing a step function of a predetermined amplitude.

9. A power amplifier comprising power amplifying means having an input for a signal to be amplified and an output for an output power signal and a control loop having means for sampling the output power signal, means for detecting the sampled output power signal, a reference control signal source, and means for comparing the detected sampled output power with the reference control signal, characterised in that the control loop further comprises means for integrating an output of the comparing means and low pass filtering means and in that there is provided multiplying means having first and second signal inputs and an output coupled to the input of the power amplifying means, a signal to be amplified being applied, in use, to the first signal input and the control loop being connected to the second input.

10. A power amplifier as claimed in claim 9, characterised in that the reference control signal source comprises means for producing a step function of a predetermined amplitude.



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