ABSTRACT

STRAINED SILICON MOS DEVICES

A structure to improve carrier mobility of a MOS device in an integrated circuit. The structure comprises a semiconductor substrate, containing a source region and a drain region; a conductive gate overlying a gate dielectric layer on the semiconductor substrate; a conformal stress film covering the source region, the drain region, and the conductive gate. In addition, the structure may comprise a semiconductor substrate, containing a source region and a drain region; a conductive gate overlying a gate dielectric layer on the semiconductor substrate; a plurality of stress films covering the source region, the drain region, and the conductive gate. Moreover, the structure may comprise a semiconductor substrate, containing a source region and a drain region; a conductive gate overlying a gate dielectric layer on the semiconductor substrate; a spacer disposed adjacent to the conductive gate, the spacer having a width less than 550 angstroms; a stress film covering the source region, the drain region, the conductive gate, and the spacer.

(FIG. 2)