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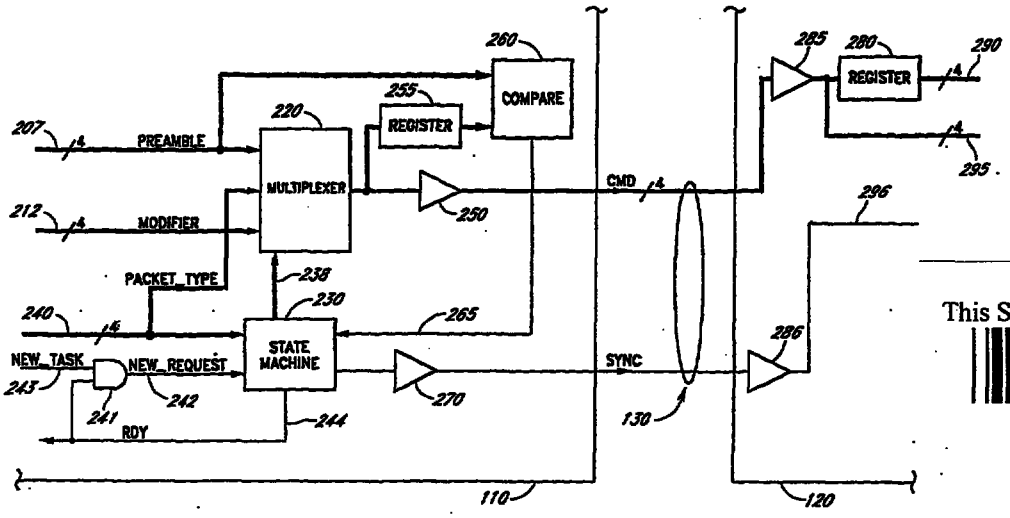

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(57) Abstract.

Customized circuitry implemented on the transmitting end of an interchip communication bus (130) reduces the number of clock cycles required to transmit control packets over the interchip communication bus (130). The packet transaction protocol is predicated upon the relationship between consecutive command words sent over the interchip bus (130) so that, if consecutive words at a packet boundary contain the same data, this data can be saved as separate command words by the receiving chip (120) within a single clock cycle. This is accomplished through the generation of a synchronization signal whenever a new packet is started. In a preferred embodiment, bit patterns for the first and/or last word of a packet which are found to be statistically more prevalent are intentionally juxtaposed to increase the probability of consecutive command words having the same information.