Capacitor with Improved Capacitance Density and Method of Manufacture

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application relates to the following co-pending and commonly assigned patent application: Serial No. _____, filed concurrently herewith and entitled "Capacitor with Enhanced Performance and Method of Manufacture" (TSM03-0556), which application is hereby incorporated herein by reference.

TECHNICAL FIELD

[0002] The present invention relates generally to semiconductor devices and more particularly to a capacitor with enhanced performance and method of manufacture.

BACKGROUND

[0003] Power supply lines in a semiconductor integrated circuit chip supply current to charge and discharge active and passive devices in the integrated circuit. For example, digital complementary metal-oxide-semiconductor (CMOS) circuits draw current when the clock makes a transition. During the operation of circuits, the power supply lines must supply transient currents with a relatively high intensity, and can result in voltage noise on the power supply lines. The voltage on the power supply line will fluctuate when the fluctuation time of the transient current is short or when its parasitic inductance or parasitic resistance is large.

[0004] In state-of-the-art circuits, the operational frequency of the integrated circuit is in the order of several hundreds of mega-hertz (MHz) to several giga-hertz (GHz). In such circuits, the rising time of clock signals is very short, so that voltage fluctuations in the supply line can be very large. Undesired voltage fluctuations in the power supply line powering a circuit can cause

noise on its internal signals and degrade noise margins. The degradation of noise margins can reduce circuit reliability or even cause circuit malfunction.

[0005] To reduce the magnitude of voltage fluctuations in the power supply lines, filtering or decoupling capacitors are usually used between the terminals of different power supply lines or between terminals of power supply line and the ground line. Decoupling capacitors act as charge reservoirs that additionally supply currents to circuits when required to prevent momentary drops in supply voltage.

[0006] Figure 1 shows a circuit diagram containing these decoupling capacitors. Capacitor C_1 is a decoupling capacitor that is inserted between a power supply line V_{DD} and the ground line *GND*. Most chips employ more than one power supply line, and may have a different power supply line OV_{DD} for the output circuits that interface with external circuits. Capacitor C_2 is a decoupling capacitor that is inserted between the output voltage supply line OV_{DD} and the ground line *GND*. Capacitor C_3 is a decoupling capacitor that is inserted between the supply line V_{DD} and the output voltage supply line OV_{DD}. These decoupling capacitors are usually placed as close as possible to the transient current source or sink.

[0007] Decoupling capacitors are used in integrated chips employing both bulk and silicon-on-insulator substrates. However, the role of decoupling capacitors is more important in a silicon-on-insulator chip than in a bulk silicon chip due to the following reason. Integrated chips fabricated on bulk substrates can naturally decouple the power supply potential and the ground potential due to the presence of inherent depletion capacitances between the doped wells and the bulk substrate. Compared to bulk substrates, silicon-on-insulator chips have very low on-chip decoupling capacitance between the power supply lines and ground.

[0008] U.S. Patent No. 6,558,998 entitled "SOI type integrated circuit with a decoupling capacity and process for embodiment of such a circuit" issued to Belleville *et al.* describes a decoupling capacitor that is formed with the formation of silicon-on-insulator substrates. While that capacitor may be formed with a large area or large capacitance, it is formed together with the substrate, which means that the substrate has to be customized for each different circuit design.

SUMMARY OF THE INVENTION

[0009] These and other problems are generally solved or circumvented, and technical advantages are generally achieved, by preferred embodiments of the present invention which teach an integrated circuit capacitor with improved capacitance density and method of manufacture a capacitor.

[0010] In accordance with a preferred embodiment of the present invention, a capacitor is formed in a capacitor includes an insulating layer overlying a substrate. A semiconductor layer overlies the insulator layer and a bottom electrode is formed in a portion of the semiconductor layer. A capacitor dielectric overlies the bottom electrode. Preferably, the capacitor dielectric comprising a high permittivity dielectric having a dielectric constant greater than about 5. A top electrode overlies the capacitor dielectric.

[0011] The preferred embodiment provides a decoupling capacitor that is formed on a semiconductor substrate that includes a silicon surface layer. A substantially flat bottom electrode is formed in a portion of the semiconductor surface layer. A capacitor dielectric overlies the bottom electrode and has a relative permittivity greater than about 5. A substantially flat top electrode overlies the capacitor dielectric. The top electrode is connected to a first reference voltage line and the bottom electrode is connected to a second reference voltage line.

[0012] The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiment disclosed may be readily

utilized as a basis for modifying or designing other structures or processes for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which:

[0014] Figure 1 shows an equivalent circuit of known decoupling capacitors;

[0015] Figure 2 provides a cross-sectional view of a preferred embodiment of this invention;

[0016] Figure 3 is a top view or layout view of a capacitor of the preferred embodiment;

[0017] Figures 4a and 4b show cross-sectional views of a capacitor of a preferred embodiment;

[0018] Figures 5a and 5b show other cross-sectional views of a capacitor of a preferred embodiment; and

[0019] Figures 6a-6f show cross-sectional views of a capacitor of the preferred embodiment during various stages of the fabrication process.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0020] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0021] In the preferred embodiment this invention, a capacitor structure with a high permittivity dielectric is formed on a silicon-on-insulator substrate. The following discussion provides further details on the various embodiments and methods of manufacture.

[0022] The preferred embodiment of the present invention relates to a capacitor, and more specifically, to capacitors formed with improved capacitance density. As an example, these capacitors can be used as decoupling capacitors. A number of examples and methods of fabrication will be discussed below.

[0023] In the preferred embodiment of this invention, capacitors with improved capacitance density are taught. Such capacitors are useful as decoupling capacitors that help reduce voltage fluctuations in voltage supply lines in integrated circuit chips. The decoupling capacitors taught in this invention can be used on bulk substrates comprising an elemental semiconductor such as silicon, bulk substrates comprising of an alloy semiconductor such as silicon-germanium, or bulk substrates comprising of a compound semiconductor such as indium phosphide. More preferably, the decoupling capacitors may be formed on semiconductor-on-insulator substrates such as silicon-on-insulator substrates.

[0024] Figure 2 provides a cross-sectional view of a preferred embodiment of this invention. In this embodiment, a decoupling capacitor 102 is formed on a semiconductor-on-insulator substrate that includes a semiconductor layer 104 on an insulator layer 106, which in turn overlies a substrate 108, preferably a silicon substrate. The capacitor 102 includes a bottom electrode 110, a capacitor dielectric 112 overlying the bottom electrode 110, and a top electrode 114 overlying the capacitor dielectric 112.

[0025] The bottom electrode 110 is preferably formed within the semiconductor layer 104. The bottom electrode 110 may be lightly-doped and electrically contacted by a highly-doped region (not shown in Figure 2, see e.g., Figure 4b). Alternatively, the bottom electrode 110 may be a highly-doped region. In various embodiments, the bottom electrode may be doped with n-type (e.g., arsenic or phosphorus) or p-type (e.g., boron) dopants.

[0026] The capacitor dielectric 112 is preferably a high permittivity (high-k) dielectric. By using a high-k dielectric as the capacitor dielectric 112, the capacitance density $\frac{\varepsilon_0 \varepsilon_r}{t_{phys}}$ is significantly higher than that of a capacitor employing a conventional silicon oxide dielectric; where ε_0 is the permittivity of free space, ε_r is the relative permittivity, and t_{phys} is the physical thickness of the capacitor dielectric. If the decoupling capacitor 102 maintains the same size (i.e., length x width of bottom and top electrodes 110 and 112), the use of a high-k capacitor dielectric improves the total capacitance and therefore reduces the voltage fluctuations in the voltage supply lines to which it decouples.

[0027] The high-k dielectric preferably has a relative permittivity of larger than 5, and more preferably has a relative permittivity of larger than 10, and even more preferably has a relative permittivity of larger than 20. The high permittivity dielectric may be selected from a group

comprising of aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), hafnium oxynitride (HfON), hafnium silicate ($HfSiO_4$), zirconium oxide (ZrO_2), zirconium oxynitride (ZrON), zirconium silicate ($ZrSiO_4$), or combinations thereof. In the preferred embodiment, the high-k dielectric is hafnium oxide.

[0028] The silicon oxide equivalent thickness (EOT) of the capacitor dielectric 112 is preferably smaller than about 100 angstroms, more preferably smaller than about 50 angstroms, and even more preferably smaller than about 10 angstroms. The physical thickness of the capacitor dielectric may be smaller than about 100 angstroms, more preferably smaller than about 50 angstroms, and even more preferably smaller than about 10 angstroms. In other embodiments, the physical thickness of the capacitor dielectric may be smaller than about 100 angstroms, more preferably smaller than about 50 angstroms, and even more preferably smaller than about 10 angstroms.

[0029] The top electrode 114 is formed from a conductive material such as poly-crystalline silicon, poly-crystalline silicon-germanium, a metal, a metallic nitride, a metallic silicide, or a metallic oxide, or combinations thereof. Metals such as molybdenum, tungsten, titanium, tantalum, platinum, and hafnium may be used as the portion of the top electrode. Metallic nitrides may include, but will not be restricted to, molybdenum nitride, tungsten nitride, titanium nitride, tantalum nitride. Metallic silicides may include, but will not be restricted to, nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, erbium silicide. Metallic oxides may include, but will not be restricted to, ruthenium oxide and indium tin oxide.

[0030] As shown in Figure 2, the decoupling capacitor may be formed in an active region in the vicinity of an active device such as a transistor 116. The transistor 116 includes source and

drain regions 118 and 120 in silicon layer 104, a gate dielectric 122, and a gate electrode 124. In the preferred embodiment, the gate dielectric 122 is formed from the same layer as the capacitor dielectric 112 and the gate electrode 124 is formed from the same layer as the top electrode 114. In fact, as will be discussed below, the transistor 116 and capacitor 102 are preferably formed at the same time.

[0031] Figure 2 also illustrates a third active region 126. While no device is shown in active region 126, it is understood that a capacitor, a transistor or another device such as a diode or a resistor can be formed. In fact a typical semiconductor chip will include many different device components formed. In some cases, a number of devices will be formed in a single active region while in other cases a single active region will include only one element.

[0032] Active region 126 is isolated from the active region that includes capacitor 102 and the active region that includes transistor 116 by isolation regions 128. In the illustrated embodiment, shallow trench isolation (STI) is used. In this case, an insulator, such as silicon oxide, is formed within a trench between active areas. In the preferred embodiment, the STI dielectric fill material is chemical vapor deposited silicon oxide. The shallow trench isolation structure may also comprise trench liner oxide (not shown for simplicity) on the boundaries of the trench. The trench liner oxide may or may not contain nitrogen. In other embodiments, other isolation techniques such as mesa isolation can be used. In those cases, the trenches are left unfilled during formation of the devices in the active regions.

[0033] Figure 3 is a top view or layout view of the capacitor 102 of the preferred embodiment. The capacitor 102 has a width W and a length L. In the preferred embodiment, the width W may have a dimension of greater than about 5 microns, and preferably greater than about 10 microns. In the preferred embodiment, the length L may have a dimension of greater

than about 1 micron, and preferably greater than about 5 microns. The detailed structure of the capacitor may be seen in cross-sectional views along the lines A-A' and B-B', which are shown in Figures 4a and 4b. The contacts 130 are shown in the cross-sectional views of Figures 5a and 5b, for example.

[0034] The cross-sectional view along line A-A' is shown in Figure 4a. The top electrode 114 extends laterally over the isolation regions 128. The top electrode in Figure 4a is shown to have a thickness t, preferably in the range of about 200 angstroms to about 2000 angstroms. The capacitor structure 102 may additionally have spacers 132 formed on the sides of the top electrode 114. In a typical embodiment, these spacers 132 are formed during formation of transistor 116 (Figure 2) and therefore also included with the capacitor 102. The spacers 132, however, are optional.

[0035] The cross-sectional view along line B-B' is shown in Figure 4b. Figure 4b shows that the bottom electrode 110 can be electrically connected via adjacent doped regions 134 and 136. One or more doped regions 134 (136) can be included. In the case where the bottom electrode 110 is not heavily doped, the bottom electrode 110 may include an inversion layer. An inversion layer may be formed by a supply of mobile carriers from the adjacent doped regions, and when there is a substantial bias between the top and bottom electrodes 110 and 114. The substantial bias can be the potential between V_{DD} and GND, between OV_{DD} and GND, or between OV_{DD} and V_{DD}.

[0036] In one embodiment, the bottom electrode 110 is doped to the same conductivity type as the contact regions 134 and 136. That is, the impurities added to the silicon layer 104 are the same conductivity type (n or p) for bottom electrode 110 and contact regions 134 and 136.

[0037] In another embodiment, the bottom electrode 110 is doped to a different conductivity type. In this case, the inversion region creates the contact between regions 110, 134 and 136. For example, in one embodiment the contact regions 134 and 136 are physically doped with n-type dopants (e.g., arsenic and/or phosphorus) and the electrode region 110 is physically doped with p-type dopants (e.g., boron). When the top electrode 114 is connected to a high enough voltage level, an inversion region will be formed in bottom electrode 110, which will appear to be n-doped. In this manner, the bottom electrode contact regions 134 and/or 136 are doped to a given conductivity type (n-type in this example) and the bottom electrode 110 is operationally doped the given conductivity type. In this context, "operationally doped" means being at that doping level whenever the chip is operational. This definition excludes a transistor, which is at that doping level only when that transistor itself, rather than the chip, is turned on.

[0038] An embodiment showing the contacts 130 and 131 to the bottom and top electrodes 110 and 114 is shown in Figures 5a and 5b (collectively Figure 5). Figure 5a shows a cross-sectional view along line A-A' of Figure 3 and Figure 5b shows a cross-sectional view along line B-B' of Figure 3.

[0039] The views of Figure 5 include an inter-layer dielectric 138. The inter-layer dielectric (ILD) 138 can be a chemical vapor deposited dielectric such as silicon oxide. The ILD 138 can also be a low permittivity (low-k) dielectric employed in interconnect technology. By using a low-k ILD to cover the capacitor 102, parasitic capacitances between the top electrode 114 and metal lines 140 in the vicinity of the top electrode 114 can be reduced.

[0040] In the preferred embodiment, the relative-permittivity of the low-k dielectric 138 is less than about 3.5, and more preferably less than about 3.0. For example, the low-k dielectric material can be an organic material, such as benzocyclobutene (BCB), SILK, FLARE, or others.

Alternatively, the low-k dielectric material can be an inorganic dielectric material, such as methyl silsesquioxane (MSQ), hydrogen silsesquioxane (HSQ), SiOF, for example. These materials are exemplary only as other embodiments may include different low-k dielectric materials.

[0041] A contact etch-stop layer 144 can overlie the top electrode 114 and the spacer 132, as shown in Figure 5. The contact etch-stop layer 144 is preferably silicon nitride, but it is understood that other materials with a different etch rate from the ILD 138 can be used. The silicon nitride etch-stop layer 144 can have an inherent stress in the range of –2 giga-pascals (GPa) to +2 GPa, where negative stress implies compressive stress and positive stress implies tensile stress.

[0042] A contact plug 131 electrically couples the top electrode 114 to interconnect metal lines 140 as shown in Figure 5a. As shown in Figure 5b, a contact plug 130 electrically couples the doped region 134 (135) in the semiconductor layer 104 with the bottom electrode 110. The contact plugs are made of a conductive material such as tungsten and may include barrier layers (not shown), e.g., titanium and titanium nitride.

[0043] A inter-metal dielectric (IMD) 142 is formed over metal layer 140 and ILD 138. The IMD 142 can be formed from any of the materials listed above. The IMD 142 can be the same material or a different material than ILD 138. While not shown, contacts can be formed through the IMD 142 to contact metal layer 140.

[0044] It is understood that the capacitor 102 can be used in a semiconductor-on-insulator technology employing trench isolation, or may be used in a semiconductor-on-insulator technology employing mesa isolation. In mesa isolation, trenches are not filled with a dielectric filling material prior to the formation of transistors or capacitors. In a semiconductor chip

employing mesa isolation, trenches between active regions are not filled with dielectric prior to the formation of active devices.

[0045] Next, a method of manufacturing a capacitor will be described with respect to Figures 6a-6f. As will be discussed, the capacitor can be formed at the same time as a transistor (see e.g., transistor 116 in Figure 2).

[0046] Referring now to Figure 6a, a semiconductor-on-insulator substrate including substrate 108, insulator 106 and semiconductor layer 104 is provided. An active region mask 148 is used to define trenches 150 in the semiconductor layer 104. The semiconductor layer 104 preferably has a thickness of about 1000 angstroms or thinner. The insulator 106 thickness is preferably about 1200 angstroms or thinner. The mask 148 preferably comprises silicon nitride, and more preferably comprises silicon nitride on a silicon oxide layer.

[0047] Trench filling dielectric material is deposited by chemical vapor deposition to fill the trenches 150, followed by a chemical mechanical planarization process step. The mask 148 is then removed to give the cross-section as shown in Figure 6b. The bottom electrode 110 may or may not be heavily doped at this point. If an ion implantation step with a high dose is introduced into the active region at this point to dope the semiconductor layer 104, a heavily-doped bottom electrode 110 can be formed. For example, the heavily-doped active region or bottom electrode 110 may have a doping concentration of greater than about $10^{19}cm^{-3}$.

[0048] The capacitor dielectric 112 is then formed, as shown in Figure 6c. The physical thickness of the dielectric 112 may be larger than 5 angstroms, more preferably larger than 20 angstroms, and even more preferably larger than 40 angstroms. The capacitor dielectric 112 may be formed together with the formation of a transistor gate dielectric in a different portion of the semiconductor chip (not shown here, see Figure 2). By forming the high-k capacitor dielectric

together with the gate dielectric of a transistor in a different portion of the chip, no additional process steps are introduced.

[0049] High-k dielectric materials as previously described may be used. The high-k dielectric may be formed by chemical vapor deposition, sputter deposition, or other known techniques of forming high-k dielectric materials. An interfacial layer (not shown) can be formed on the bottom electrode 110 prior to the formation of the high-k dielectric material 112. The interfacial layer may be a silicon oxide layer or a silicon oxynitride layer. The active region may additionally be treated in a hydrogen-containing or nitrogen-containing ambient prior to the formation of the interfacial layer.

[0050] The top electrode 114 material can then be deposited over the capacitor dielectric layer 112. The top electrode material can be comprised of conventional poly-crystalline silicon, poly-crystalline silicon germanium, metals, metallic silicides, or metallic nitrides, as previously described. The top electrode material may be deposited by conventional techniques such as chemical vapor deposition. The top electrode may also be formed by the deposition of silicon and metal, followed by an anneal to form a metal silicide gate electrode material. The top electrode material is then patterned using photolithography techniques, and etched using plasma etch processes to form the gate electrodes.

[0051] The deposition of the top electrode 114 material may be the same process step as the deposition of gate electrode material of a transistor to be formed in a different portion of the semiconductor chip, and the etching of the top electrode may similarly be accomplished together with the etching of the gate electrode of the transistor. The completed top electrode 114 is shown in Figure 6d. The capacitor dielectric 112 is retained at least in the portion of the capacitor covered by the top electrode 114.

[0052] Doping may be introduced in regions adjacent to the bottom electrode to make electrical contacts with the bottom electrode 110. The electrical contact regions 134 and 136 are shown in the cross-sectional views of Figure 4b and Figure 5b (and are above and below the plane of the page in the view of Figure 6d. The doping of contact regions 134 and 136 is formed at the same time that source and drain regions of the transistor (116 in Figure 2) are doped. For example, the doping step performed in Figure 6d can form the lightly doped extensions of the source and drain.

[0053] As shown in Figure 6e, spacers 132 may be additionally formed on the sides of the top electrode 114. This may be followed by another implant to doped the regions (134 and 136 in Figure 4b) of the active region not covered by the top electrode 114 and spacers 132. This step will simultaneously form the heavily doped source and drain regions of transistors on the chip.

[0054] A contact etch-stop layer 144 can be formed on the top electrode 114 and spacers 132. An inter-layer dielectric (ILD) 142 can be formed over the capacitor and contact holes 131 (and 130 in Figure 5b) can be etched through the ILD 142 to reach the top and bottom electrodes 110 and 114. Conductive materials, such as tungsten, are then used to fill the contact holes to electrically contact the top and bottom electrodes to metal layers (see e.g., metal layer 140 in Figure 5b).

[0055] Although the capacitor described in this invention has been illustrated for use as a decoupling capacitance, it is understood that the capacitor thus formed according to this invention may be used for other purposes. For example, the capacitor may be used as a coupling capacitor.

[0056] In the foregoing specification, the invention has been described with reference to specific embodiments. However, various modifications and changes can be made by one skilled in the art without departing from the scope of the present invention. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of the present invention.

[0057] While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.

WHAT IS CLAIMED IS:

1. A capacitor comprising:

an insulating layer overlying a substrate;

a semiconductor layer overlying the insulator layer;

a bottom electrode formed in a portion of the semiconductor layer;

a capacitor dielectric overlying the bottom electrode, the capacitor dielectric comprising a high permittivity dielectric having a dielectric constant greater than about 5; and

a top electrode overlying the capacitor dielectric.

2. The capacitor of claim 1 wherein the capacitor is a decoupling capacitor.

3. The capacitor of claim 2 wherein the top electrode is connected to a power supply line and the bottom electrode is connected to a ground line.

4. The capacitor of claim 2 wherein the top electrode is connected to a first power supply line and the bottom electrode is connected to a second power supply line.

5. The capacitor of claim 1 wherein the bottom electrode or the top electrode is substantially flat.

6. The capacitor of claim 1 wherein the top electrode comprises poly-crystalline silicon.

7. The capacitor of claim 1 wherein the top electrode comprises a metal selected from the group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

8. The capacitor of claim 1 wherein the top electrode comprises a metal nitride selected from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, tantalum nitride, or combinations thereof.

9. The capacitor of claim 1 wherein the top electrode comprises a metal silicide selected from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, erbium silicide, or combinations thereof.

10. The capacitor of claim 1 wherein the top electrode comprises a metal oxide selected from the group consisting of ruthenium oxide, indium tin oxide, or combinations thereof.

11. The capacitor of claim 1 wherein the high permittivity dielectric comprises hafnium oxide.

12. The capacitor of claim 1 wherein the high permittivity dielectric comprises a material is selected from the group consisting of aluminum oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, or combinations thereof.

13. The capacitor of claim 1 wherein the high permittivity dielectric has a relative permittivity of greater than about 10.

14. The capacitor of claim 1 wherein the high permittivity dielectric has a relative permittivity of greater than about 20.

15. The capacitor of claim 1 wherein the capacitor dielectric has a physical thickness of less than about 100 angstroms.

16. The capacitor of claim 1 wherein the capacitor dielectric has a physical thickness of less than about 20 angstroms.

17. The capacitor of claim 1 wherein the capacitor has a width of larger than about 5 microns.

18. The capacitor of claim 1 wherein the capacitor has a width of larger than about 10 microns.

19. The capacitor of claim 1 wherein the capacitor has a length of larger than about 1 micron.

20. The capacitor of claim 1 wherein the capacitor has a length of larger than about 5 microns.

21. The capacitor of claim 1 wherein the bottom electrode contact region is doped to the first conductivity type and wherein the bottom electrode is doped to a second conductivity type and coupled to a supply voltage that creates an inversion region of the first conductivity type.

22. The capacitor of claim 1 wherein the bottom electrode and the bottom electrode contact region are doped to the first conductivity type.

23. A decoupling capacitor comprising:

a semiconductor substrate comprising a silicon surface layer;

a substantially flat bottom electrode formed in a portion of the semiconductor surface layer;

a capacitor dielectric overlying the bottom electrode, the capacitor dielectric comprising a high permittivity dielectric with a relative permittivity greater than about 5;

a substantially flat top electrode overlying the capacitor dielectric; and

wherein the top electrode is electrically coupled to a first reference voltage line and the bottom electrode is electrically coupled to a second reference voltage line.

24. The capacitor of claim 23 wherein the top electrode is connected to a power supply line and the bottom electrode is connected to a ground line.

25. The capacitor of claim 23 wherein the top electrode is connected to a first power supply line and the bottom electrode is connected to a second power supply line.

26. The capacitor of claim 23 wherein the semiconductor substrate is a bulk silicon substrate.

27. The capacitor of claim 23 wherein the semiconductor substrate is a silicon-on-insulator substrate.

28. The capacitor of claim 23 wherein the top electrode comprises silicon.

29. The capacitor of claim 23 wherein the top electrode comprises a metal selected from the group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

30. The capacitor of claim 23 wherein the top electrode comprises a metal nitride selected from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, tantalum nitride, or combinations thereof.

31. The capacitor of claim 23 wherein the top electrode comprises a metal silicide selected from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, erbium silicide, or combinations thereof.

32. The capacitor of claim 23 wherein the high permittivity dielectric comprises hafnium oxide.

33. The capacitor of claim 23 wherein the high permittivity dielectric comprises a material selected from the group consisting of hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, and combinations thereof.

34. The capacitor of claim 23 wherein the high permittivity dielectric has a relative permittivity of greater than 10.

35. The capacitor of claim 23 wherein the high permittivity dielectric has a relative permittivity of greater than 20.

36. The capacitor of claim 23 wherein the capacitor dielectric has a physical thickness of less than about 100 angstroms.

37. The capacitor of claim 23 wherein the capacitor dielectric has a physical thickness of less than about 50 angstroms.

38. The capacitor of claim 23 wherein the capacitor dielectric has a physical thickness of less than about 10 angstroms.

39. The capacitor of claim 23 wherein the capacitor has a width of larger than about 5 microns.

40. The capacitor of claim 23 wherein the capacitor has a width of larger than about 10 microns.

41. The capacitor of claim 23 wherein the capacitor has a length of larger than about 1 micron.

42. The capacitor of claim 23 wherein the capacitor has a length of larger than about 5 microns.

43. The capacitor of claim 23 wherein the bottom electrode is doped to a first conductivity type, the capacitor further comprising adjacent doped regions doped to a second conductivity type.

44. The capacitor of claim 43 wherein the first conductivity type is n-type and the second conductivity type is p-type.

45. The capacitor of claim 43 wherein the first conductivity type is p-type and the second conductivity type is n-type.

46. The capacitor of claim 23 wherein the bottom electrode is doped to a first conductivity type, the capacitor further comprising adjacent doped regions with the first conductivity type.

47. The capacitor of claim 23 and further comprising spacers formed on sides of the top electrode.

48. The capacitor of claim 47 and further comprising an etch-stop layer overlying the top electrode and the spacers.

49. The capacitor of claim 48 wherein the etch-stop layer comprises silicon nitride.

50. The capacitor of claim 48 and further comprising an inter-layer dielectric overlying the etch-stop layer.

51. The capacitor of claim 50 wherein the inter-layer dielectric comprises silicon oxide.

52. The capacitor of claim 50 wherein the inter-layer dielectric comprises a dielectric with a relative permittivity less than about 3.5.

53. The capacitor of claim 50 wherein the inter-layer dielectric comprises a dielectric with a relative permittivity less than about 3.0.

54. The capacitor of claim 50 wherein the inter-layer dielectric is selected from the group consisting of benzocyclobutene (BCB), SILK, FLARE, methyl silsesquioxane (MSQ), hydrogen silsesquioxane (HSQ), and SiOF.

55. The capacitor of claim 50 and further comprising a first contact plug in electrical contact with the bottom electrode and a second contact plug in electrical contact with the top electrode.

56. The capacitor of claim 23 further comprising a shallow trench isolation region adjacent to the bottom electrode.

57. The capacitor of claim 23 wherein semiconductor substrate comprises a semiconductor on insulator substrate including a plurality of islands, wherein the islands are isolated from one another by mesa isolation.

58. A method of forming a capacitor, the method comprising:

providing a silicon-on-insulator substrate including a silicon layer overlying an insulator layer;

forming a bottom electrode in the silicon layer;

forming a capacitor dielectric on bottom electrode, the capacitor dielectric comprising a high permittivity dielectric with a relative permittivity greater than about 5;

forming a top electrode on capacitor dielectric;

forming a bottom electrode contact region within the strained silicon layer adjacent the bottom electrode; and

electrically connecting the bottom electrode and the bottom electrode contact region.

59. The method of claim 58 wherein the capacitor is a decoupling capacitor.

60. The method of claim 58 wherein the step of forming the bottom electrode comprises:

forming an active region;

forming isolation regions surrounding the active region; and

doping the active region.

61. The method of claim 60 wherein the active region has a doping concentration of greater than about $10^{19}cm^{-3}$.

62. The method of claim 58 wherein forming the capacitor dielectric comprises a chemical vapor deposition step.

63. The method of claim 58 wherein forming the capacitor dielectric comprises a sputtering deposition step.

64. The method of claim 58 wherein the step of forming the capacitor dielectric comprises:

forming an interfacial oxide layer; and

forming a high permittivity dielectric layer.

65. The method of claim 58 and further comprising:

doping a portion of the silicon layer not covered by top electrode;

forming spacers on sides of the top electrode; and

doping a portion of the silicon layer not covered by the top electrode and spacers.

66. The method of claim 65 wherein the spacers comprise silicon nitride.

67. The method of claim 65 further comprising:

depositing an etch-stop layer over top electrode and spacers;

forming an inter-layer dielectric over etch-stop layer;

forming contact holes in inter-layer dielectric; and

filling the contact holes with a conductive material to form contact plugs.

68. The method of claim 67 wherein the etch-stop layer comprises silicon nitride.

69. The method of claim 67 wherein the inter-layer dielectric comprises silicon oxide.

70. The method of claim 67 wherein the inter-layer dielectric comprises a dielectric with a relative permittivity less than about 3.5.

71. The method of claim 67 wherein the inter-layer dielectric comprises a dielectric with a relative permittivity less than about 3.0.

72. The method of claim 67 wherein the inter-layer dielectric is selected from the group consisting of benzocyclobutene (BCB), SILK, FLARE, methyl silsesquioxane (MSQ), hydrogen silsesquioxane (HSQ), and SiOF.

73. The method of claim 67 wherein the contact plugs comprise a first contact plug that electrically contacts the bottom electrode and a second contact plug that electrically contacts the top electrode.

74. The method of claim 73 wherein the top electrode is electrically coupled to a power supply line and the bottom electrode is electrically coupled to a ground line.

75. The method of claim 73 wherein the top electrode is electrically coupled to a first power supply line and the bottom electrode is electrically coupled to a second power supply line.

76. The method of claim 58 wherein the insulator layer comprise silicon oxide.

77. The method of claim 58 wherein the insulator layer has a thickness of less than about 1200 angstroms.

78. The method of claim 58 wherein the silicon layer has a thickness of less than about 1000 angstroms.

79. The method of claim 58 wherein the top electrode comprises silicon.

80. The method of claim 58 wherein the top electrode comprises a metal selected from the group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

81. The method of claim 58 wherein the top electrode comprises a metallic nitride selected from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, tantalum nitride, or combinations thereof.

82. The method of claim 58 wherein the top electrode comprises a metallic silicide selected from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, erbium silicide, or combinations thereof.

83. The method of claim 58 wherein the high permittivity comprises hafnium oxide.

84. The method of claim 58 wherein the high permittivity dielectric is selected from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, or combinations thereof.

85. The method of claim 58 wherein the high permittivity dielectric has a relative permittivity of greater than about 10.

86. The method of claim 58 wherein the high permittivity dielectric has a relative permittivity of greater than about 20.

87. The method of claim 58 wherein the capacitor dielectric has a physical thickness of less than about 100 angstroms.

88. The method of claim 58 wherein the capacitor dielectric has a physical thickness of less than about 50 angstroms.

89. The method of claim 58 wherein the capacitor dielectric has a physical thickness of less than about 10 angstroms.

90. The method of claim 58 wherein the capacitor has a width of greater than about 5 microns.

91. The method of claim 58 wherein the capacitor has a width of greater than about 10 microns.

92. The method of claim 58 wherein the capacitor has a length of greater than about 1 micron.

93. The method of claim 58 wherein the capacitor has a length of greater than about 5 microns.