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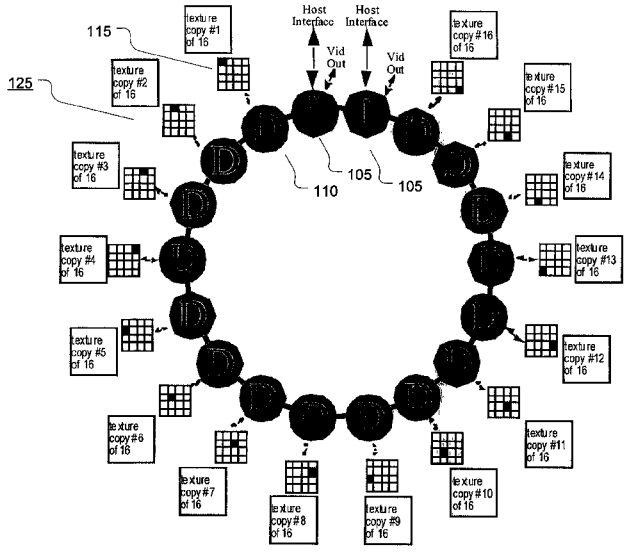
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(54) Title: SCALABLE HIGH PERFORMANCE 3D GRAPHICS



Texture and Frame Buffer Memory Allocation and Partitioning

(57) Abstract: A high-speed ring topology. In one embodiment, two base chip types are required: a "drawing" chip, LoopDraw (110), and an "interface" chip, LoopInterface (105). Each of these chips have a set of pins that supports an identical high speed point to point unidirectional input and output ring interconnect interface: the LoopLink (125). The LoopDraw chip (110) uses additional pins to connect to several standard memories (115) that form a high bandwidth local memory sub-system. The LoopInterface chip (105) uses additional pins to support a high speed host computer host interface, at least one video output interface, and possibly also additional non-local interconnects to other LoopInterface chip(s) (105).

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