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COMPUTER SYSTEM HAVING APPARATUS FOR ASYNCHRONOUSLY DELIVERING CONTROL ELEMENTS WITH A PIPE INTERFACE

ABSTRACT

A microprocessor system which includes a processor unit with system memory and a separate buffer memory, one or more subsystem adapter units with memory, optional I/O devices which may attach to the adapters, and a bus interface. The memory in the processor and the memory in the adapters are used by the system as a shared memory (106,112) which is configured as a distributed FIFO circular queue (a pipe). Unit to unit asynchronous communication is accomplished by placing control elements (104,116) on the pipe which represent requests, replies, and status information. The units (622,624) send and receive control elements (104,116) independent of the other units which allows free flowing asynchronous delivery of control information and data between units (622,624). The shared memory (106,112) can be organised as pipe pairs between each pair of units to allow full duplex operation by using one pipe for outbound control elements (104,116) and the other pipe for inbound control elements (104,116). The control elements (104,116) have standard fixed header fields with variable fields following the fixed header. The fixed header allows a common interface protocol to be used by different hardware adapters. The combination of the pipe and the common interface protocol allows many different types of hardware adapters to asynchronously communicate, resulting in higher overall throughput due to lower interrupt overhead.

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