CLAIMS

What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate having a diffusion region;

a transistor formed within said diffusion region and comprising a source, a drain, and a gate;

a power rail disposed outside said diffusion region;

a contact layer disposed above said substrate and below said power rail; and

a via disposed between said contact layer and said power rail to electrically connect said contact layer to said power rail; and wherein

said contact layer includes a first length disposed outside said diffusion region and a second length extending from said first length into said diffusion region and electrically connected to said transistor.

2. A semiconductor device as set forth in claim 1 wherein said second length of said contact layer is electrically connected to at least one of a source and a drain of said transistor.

3. A semiconductor device as set forth in claim 1 wherein said via is further defined as a plurality of vias disposed between said power rail and said first length of said contact layer and spaced from one another.

4. A semiconductor device as set forth in claim 1 wherein said transistor is further defined as a plurality of transistors formed within said diffusion region.

5. A semiconductor device as set forth in claim 4 wherein said second length of said contact layer is electrically connected to one of said transistors and wherein said contact layer further includes a third length extending from said first length into said diffusion region and electrically connected to another of said transistors.

6. A semiconductor device as set forth in claim 5 wherein said second length and said third length are generally perpendicular to said first length.

7. A semiconductor device as set forth in claim 1 wherein said second length is generally perpendicular to said first length.

8. A semiconductor device as set forth in claim 1 wherein said gate of said transistor extends linearly and said power rail extends linearly and said gate of said transistor and said power rail are generally perpendicular to one another.

9. A semiconductor device as set forth in claim 1 further comprising a metal pin layer extending from said diffusion region to outside of said diffusion region.

10. A semiconductor device as set forth in claim 1 wherein said contact layer comprises a semiconductor material.

11. A semiconductor device comprising:

a semiconductor substrate having a first diffusion region and a second diffusion region;

at least one transistor formed within each of said diffusion regions wherein each transistor comprises a source, a drain, and a gate;

a first power rail disposed outside and adjacent to said first diffusion region;

a second power rail disposed outside and adjacent to said second diffusion region;

a first contact layer disposed above said substrate and below said first power rail;

a second contact layer disposed above said substrate and below said second power rail; and

a plurality of vias disposed between said contact layers and said power rails to respectively electrically connect said contact layers to said power rails; wherein

said first contact layer including a first length running generally congruent with said first power rail and a second length extending from said first length into said first diffusion region and electrically connected to said at least one transistor; and wherein

said second contact layer including a first length disposed outside said diffusion region and a second length extending from said first length into said second diffusion region and electrically connected to said at least one transistor.

12. A semiconductor device as set forth in claim 11 wherein said second length of said contact layer is electrically connected to at least one of a source and a drain of said at least one transistor.

13. A semiconductor device as set forth in claim 11 wherein said at least one transistor is further defined as a plurality of transistors formed within each of said diffusion regions.

14. A semiconductor device as set forth in claim 13 wherein said second length of said first contact layer is electrically connected to one of said transistors and wherein said first contact layer further includes a third length extending from said first length into said diffusion region and electrically connected to another of said transistors.

15. A semiconductor device as set forth in claim 14 wherein said second length and said third length of said first contact layer are generally perpendicular to said first length of said first contact layer.

16. A semiconductor device as set forth in claim 11 wherein said second length of said first contact layer is generally perpendicular to said first length of said first contact layer.

17. A semiconductor device as set forth in claim 11 wherein said gates of said transistors extend linearly and said power rails extend linearly and said gates of said transistors are generally perpendicular to power rails.

18. A semiconductor device as set forth in claim 10 further comprising a metal pin layer extending from said first diffusion region to said second diffusion region.

19. A semiconductor device as set forth in claim 10 wherein said second length of said contact layer is electrically connected to at least one of a source and a drain of said at least one transistor.

20. A semiconductor device as set forth in claim 11 further comprising

a metal pin layer extending from said first diffusion region to said second diffusion region; and wherein

said contact layers each comprise a semiconductor material;

said at least one transistor is further defined as a plurality of transistors formed within each of said diffusion regions;

said second length of said first contact layer is electrically connected to one of said transistors and wherein said first contact layer further includes a third length extending from said first length into said diffusion region and electrically connected to another of said transistors;

said second length and said third length of said first contact layer are generally perpendicular to said first length of said first contact layer;

said second length of said first contact layer is generally perpendicular to said first length of said first contact layer; and

said gates of said transistors extend linearly and said power rails extend linearly and said gates of said transistors are generally perpendicular to power rails.

CLAIMS

1. A semiconductor device comprising:

a semiconductor substrate having a diffusion region;

a transistor formed within said diffusion region and comprising a source, a drain, and a gate;

a metal layer including

a power rail disposed outside said diffusion region and

a pin layer extending from said diffusion region to outside said diffusion region;

a contact layer disposed above said substrate and below said metal layer; and

a via disposed between said contact layer and said power rail to electrically connect said contact layer to said power rail; and wherein

said contact layer includes a first length disposed outside said diffusion region and a second length extending from said first length into said diffusion region and electrically connected to said transistor.

2. A semiconductor device as set forth in claim 1 wherein said second length of said contact layer is electrically connected to at least one of a source and a drain of said transistor.

3. A semiconductor device as set forth in claim 1 wherein said via is further defined as a plurality of vias disposed between said power rail and said first length of said contact layer and spaced from one another.

4. A semiconductor device as set forth in claim 1 wherein said transistor is further defined as a plurality of transistors formed within said diffusion region.

5. A semiconductor device as set forth in claim 4 wherein said second length of said contact layer is electrically connected to one of said transistors and wherein said contact layer further includes a third length extending from said first length into said diffusion region and electrically connected to another of said transistors.

6. A semiconductor device as set forth in claim 5 wherein said second length and said third length are generally perpendicular to said first length.

7. A semiconductor device as set forth in claim 1 wherein said second length is generally perpendicular to said first length.

8. A semiconductor device as set forth in claim 1 wherein said gate of said transistor extends linearly and said power rail extends linearly and said gate of said transistor and said power rail are generally perpendicular to one another.

9. A semiconductor device as set forth in claim 1 wherein said contact layer comprises a semiconductor material.

10. A semiconductor device comprising:

a semiconductor substrate having a first diffusion region and a second diffusion region;

at least one transistor formed within each of said diffusion regions wherein each transistor comprises a source, a drain, and a gate;

a first power rail disposed outside and adjacent to said first diffusion region;

a second power rail disposed outside and adjacent to said second diffusion region;

a first contact layer disposed above said substrate and below said first power rail;

a second contact layer disposed above said substrate and below said second power rail; and

a plurality of vias disposed between said contact layers and said power rails to respectively electrically connect said contact layers to said power rails; wherein

said first contact layer including a first length running generally congruent with said first power rail and a second length extending from said first length into said first diffusion region and electrically connected to said at least one transistor; and wherein

said second contact layer including a first length disposed outside said diffusion region and a second length extending from said first length into said second diffusion region and electrically connected to said at least one transistor.

11. A semiconductor device as set forth in claim 11 wherein said second length of said contact layer is electrically connected to at least one of a source and a drain of said at least one transistor.

12. A semiconductor device as set forth in claim 11 wherein said at least one transistor is further defined as a plurality of transistors formed within each of said diffusion regions.

13. A semiconductor device as set forth in claim 13 wherein said second length of said first contact layer is electrically connected to one of said transistors and wherein said first contact layer further includes a third length extending from said first length into said diffusion region and electrically connected to another of said transistors.

14. A semiconductor device as set forth in claim 14 wherein said second length and said third length of said first contact layer are generally perpendicular to said first length of said first contact layer.

15. A semiconductor device as set forth in claim 11 wherein said second length of said first contact layer is generally perpendicular to said first length of said first contact layer.

16. A semiconductor device as set forth in claim 11 wherein said gates of said transistors extend linearly and said power rails extend linearly and said gates of said transistors are generally perpendicular to power rails.

17. A semiconductor device as set forth in claim 10 further comprising a metal pin layer extending from said first diffusion region to said second diffusion region.

18. A semiconductor device as set forth in claim 10 wherein said second length of said contact layer is electrically connected to at least one of a source and a drain of said at least one transistor.

19. A semiconductor device as set forth in claim 11 further comprising

a metal pin layer extending from said first diffusion region to said second diffusion region; and wherein

said contact layers each comprise a semiconductor material;

said at least one transistor is further defined as a plurality of transistors formed within each of said diffusion regions;

said second length of said first contact layer is electrically connected to one of said transistors and wherein said first contact layer further includes a third length extending from said first length into said diffusion region and electrically connected to another of said transistors;

said second length and said third length of said first contact layer are generally perpendicular to said first length of said first contact layer;

said second length of said first contact layer is generally perpendicular to said first length of said first contact layer; and

said gates of said transistors extend linearly and said power rails extend linearly and said gates of said transistors are generally perpendicular to power rails.