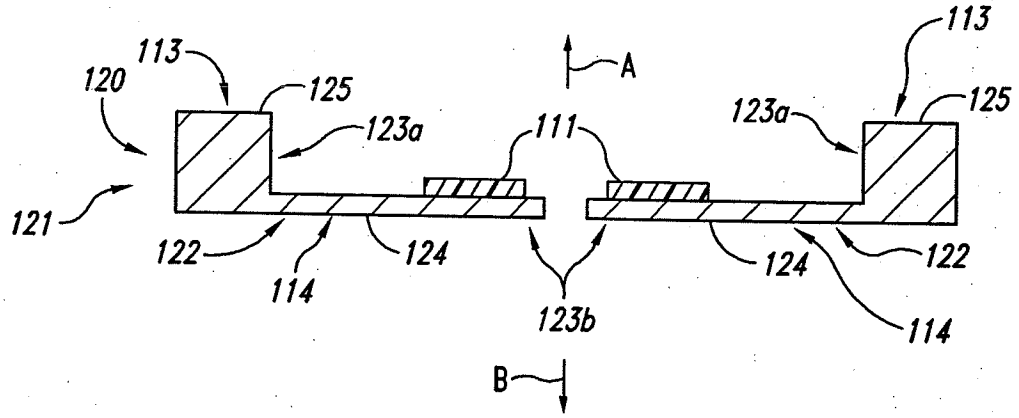


Fig. 1A

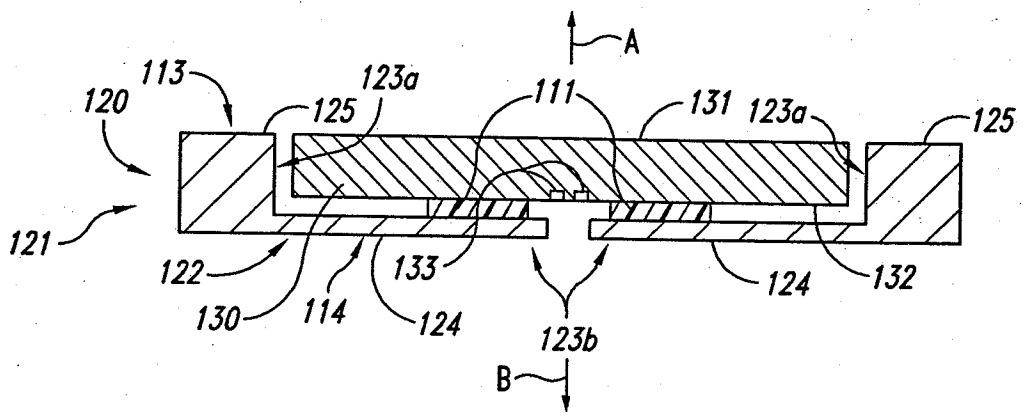


Fig. 1B

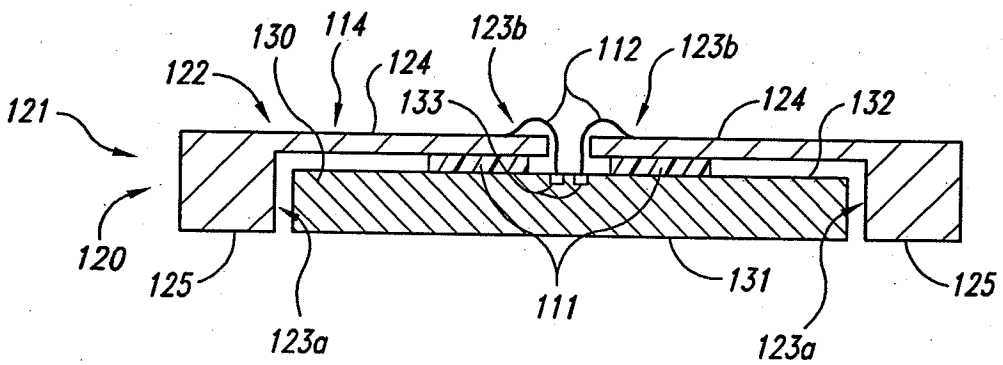


Fig. 1C

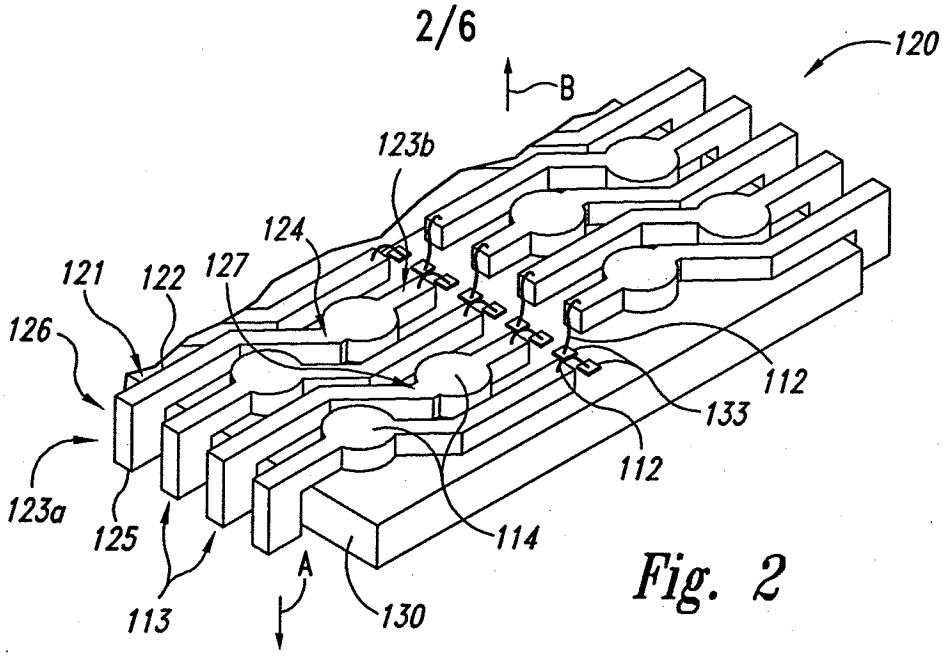


Fig. 2

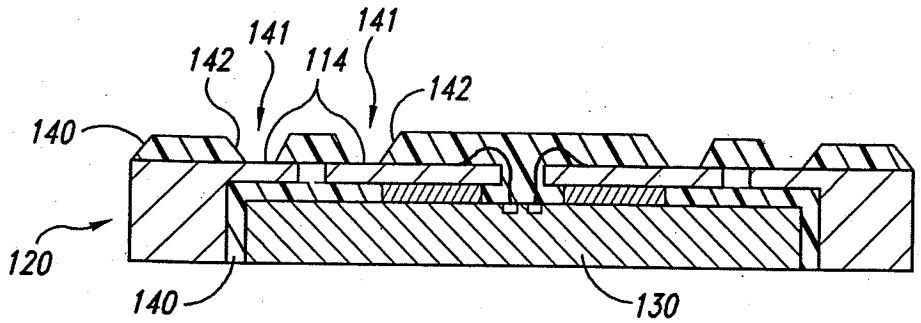


Fig. 3A

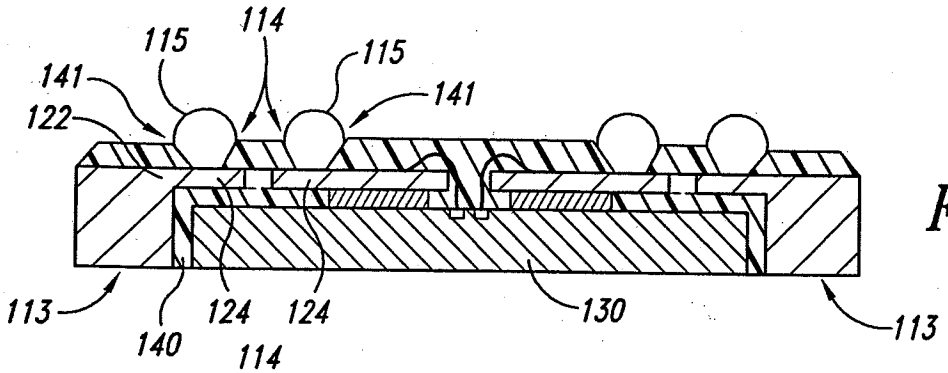


Fig. 3B

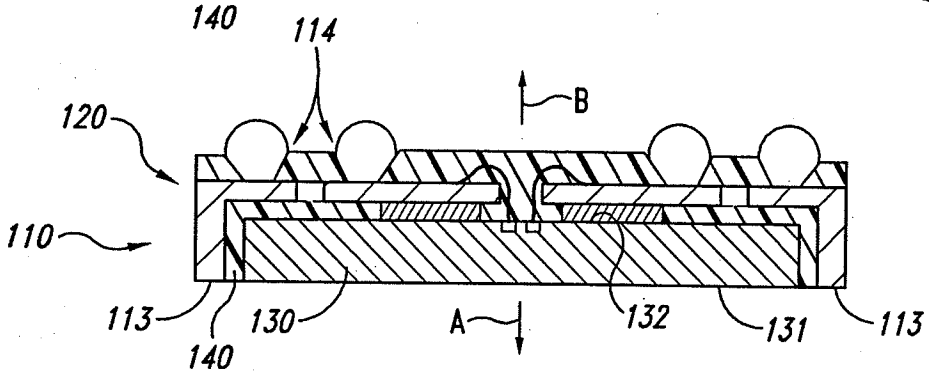


Fig. 3C

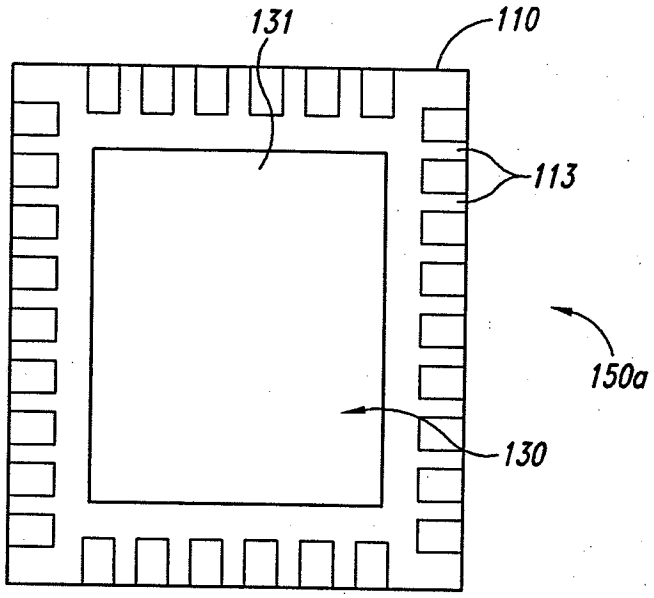


Fig. 4A

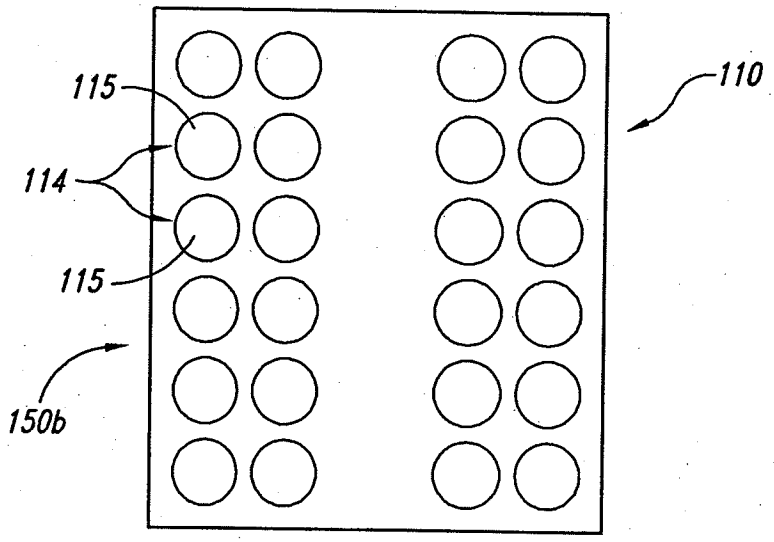


Fig. 4B

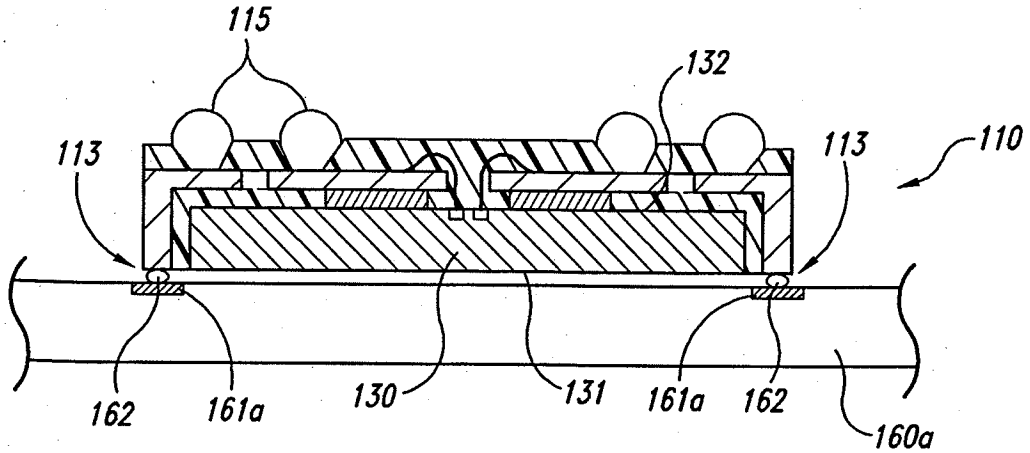

115
132
113
113
110
162
161a
130
131
161a
162
160a

Fig. 5A

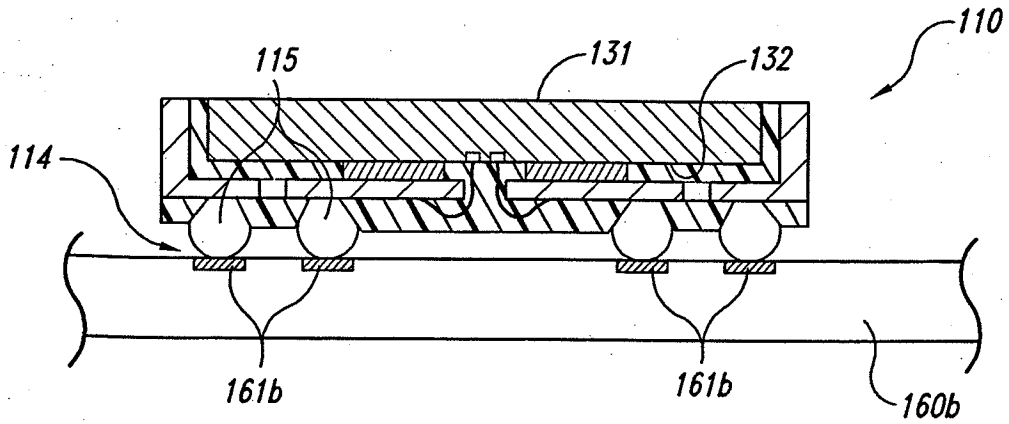

110
115
131
132
114
161b
161b
160b

Fig. 5B

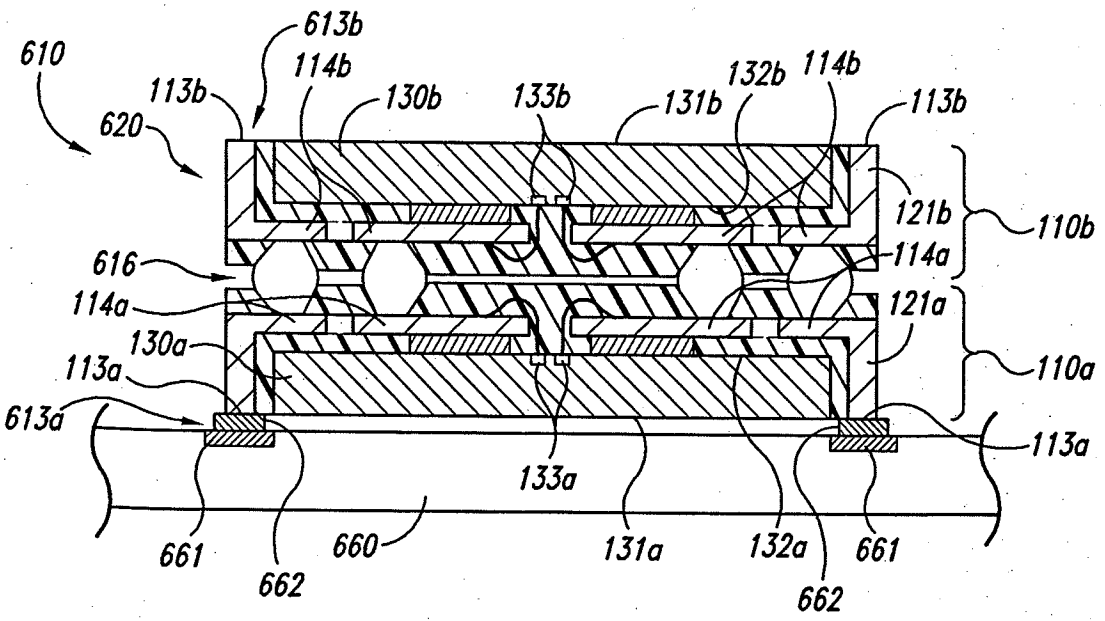

610
613b
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113b
130b
133b
131b
132b
114b
113b
620
121b
110b
616
114a
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121a
130a
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661
662
660
131a
132a
661
662

Fig. 6

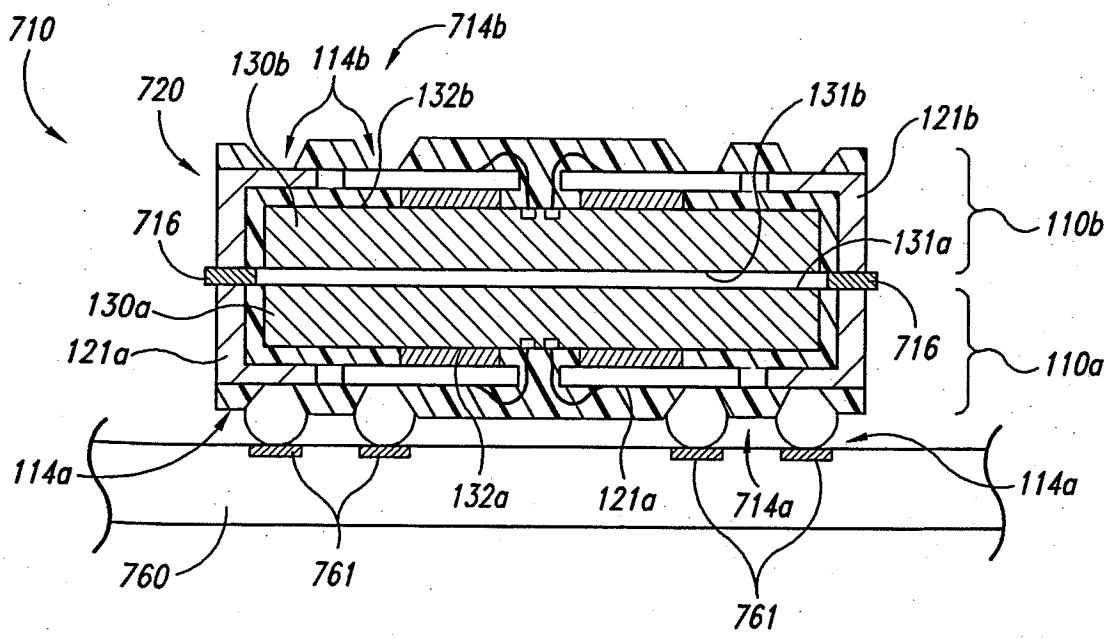

710
714b
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114b
720
132b
131b
121b
716
131a
110b
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716
121a
110a
114a
132a
121a
714a
114a
760
761
761

Fig. 7

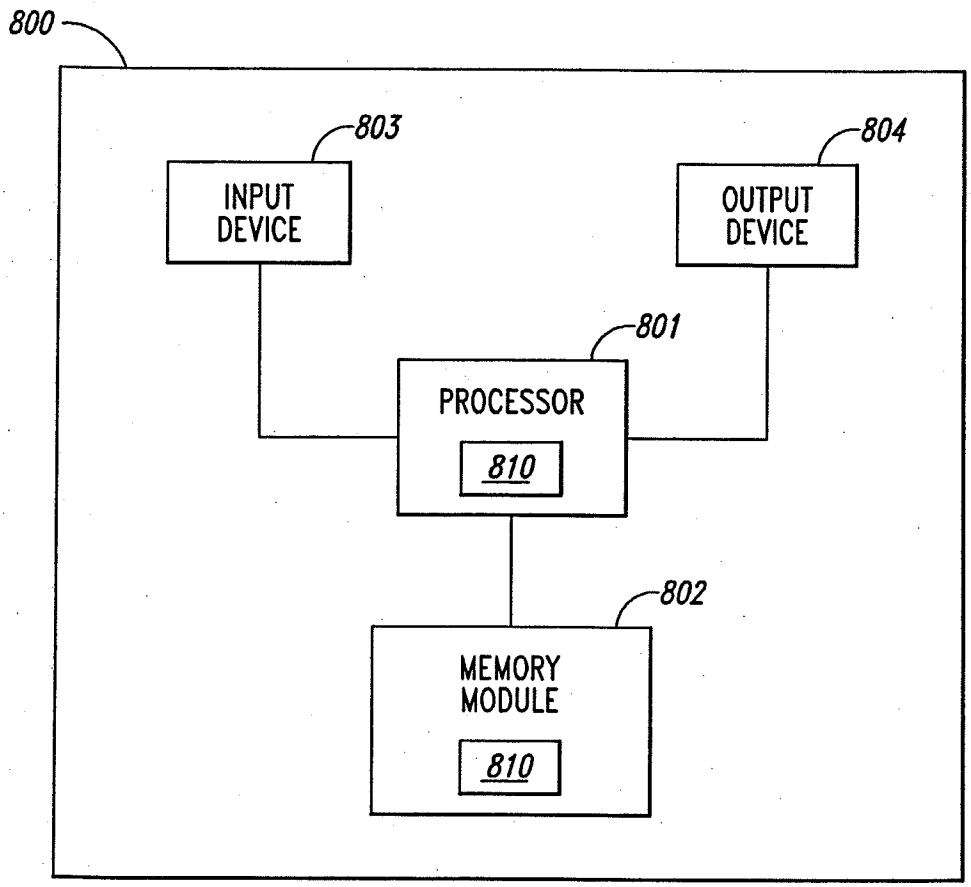

800
803
INPUT DEVICE
804
OUTPUT DEVICE
801
PROCESSOR
810
802
MEMORY MODULE
810

Fig. 8