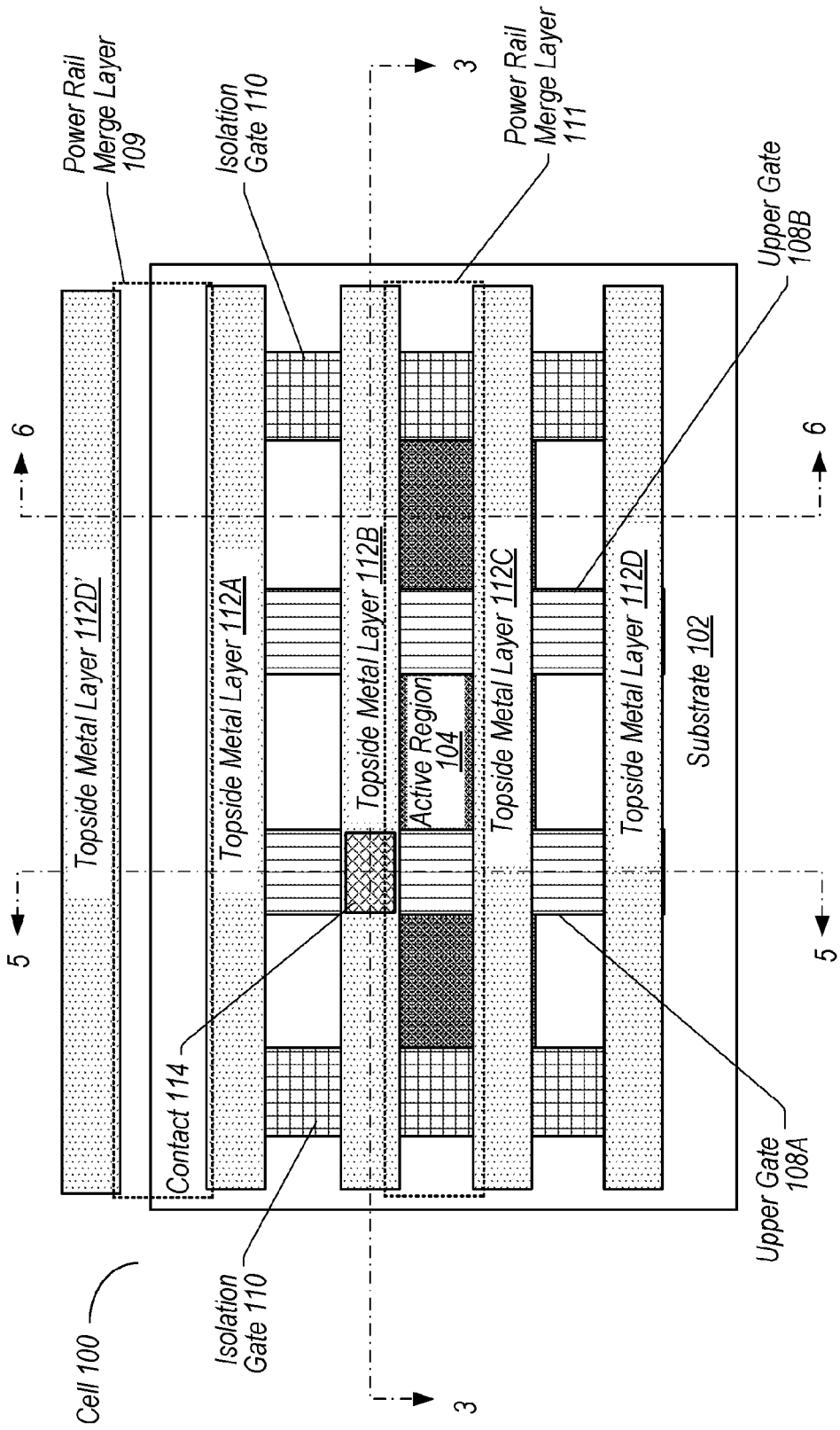

Power Rail Merge Layer 109
Isolation Gate 110
Power Rail Merge Layer 111
Upper Gate 108B
3
6
5
Topside Metal Layer 112D'
Topside Metal Layer 112A
Topside Metal Layer 112B
Active Region 104
Topside Metal Layer 112C
Topside Metal Layer 112D
Substrate 102
Contact 114
Isolation Gate 110
Upper Gate 108A
Cell 100

FIG. 1

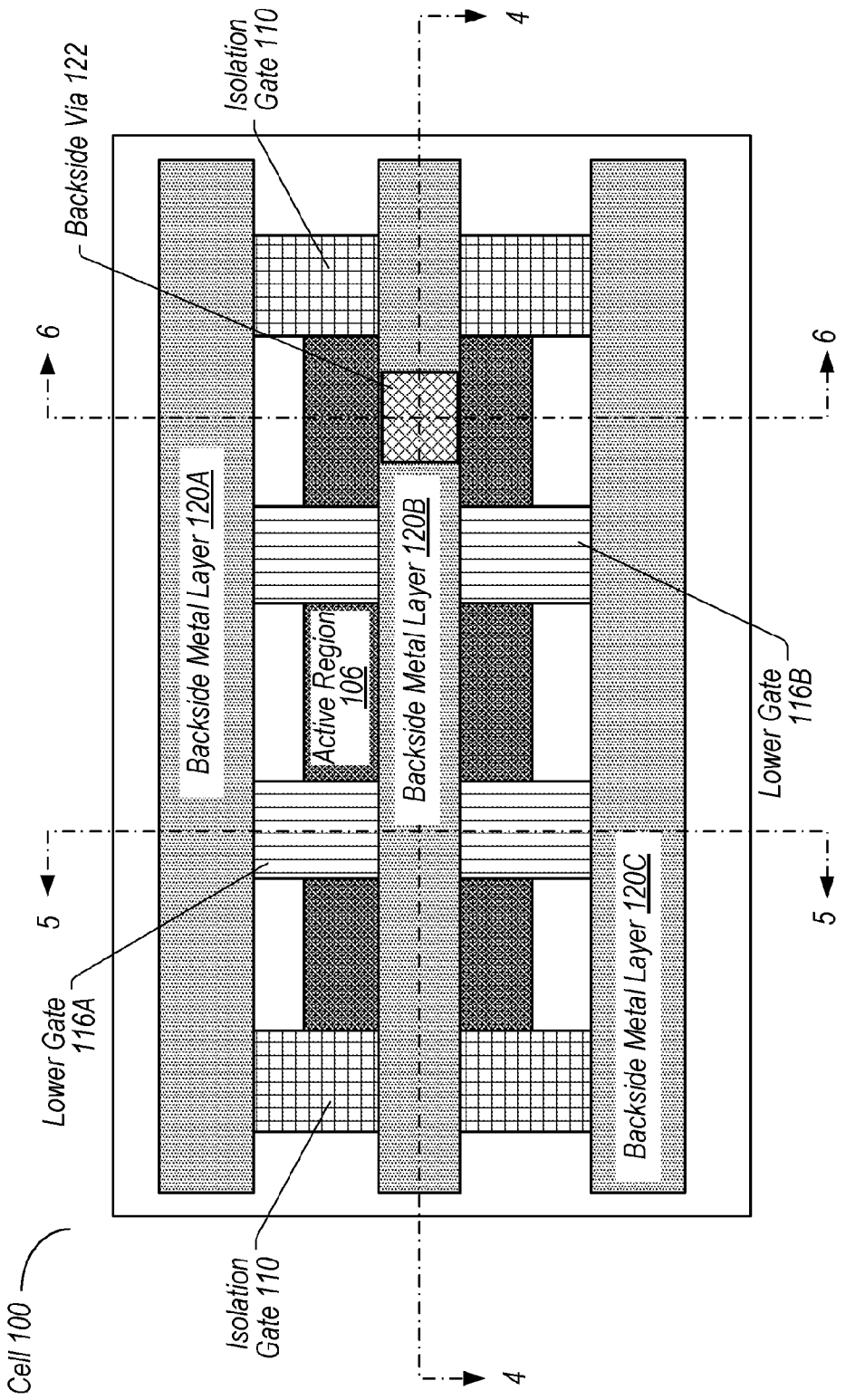

Backside Via 122
Isolation Gate 110
4
6
6
Backside Metal Layer 120A
Active Region 106
Backside Metal Layer 120B
Backside Metal Layer 120C
Lower Gate 116B
Lower Gate 116A
5
5
Isolation Gate 110
Cell 100
4

FIG. 2

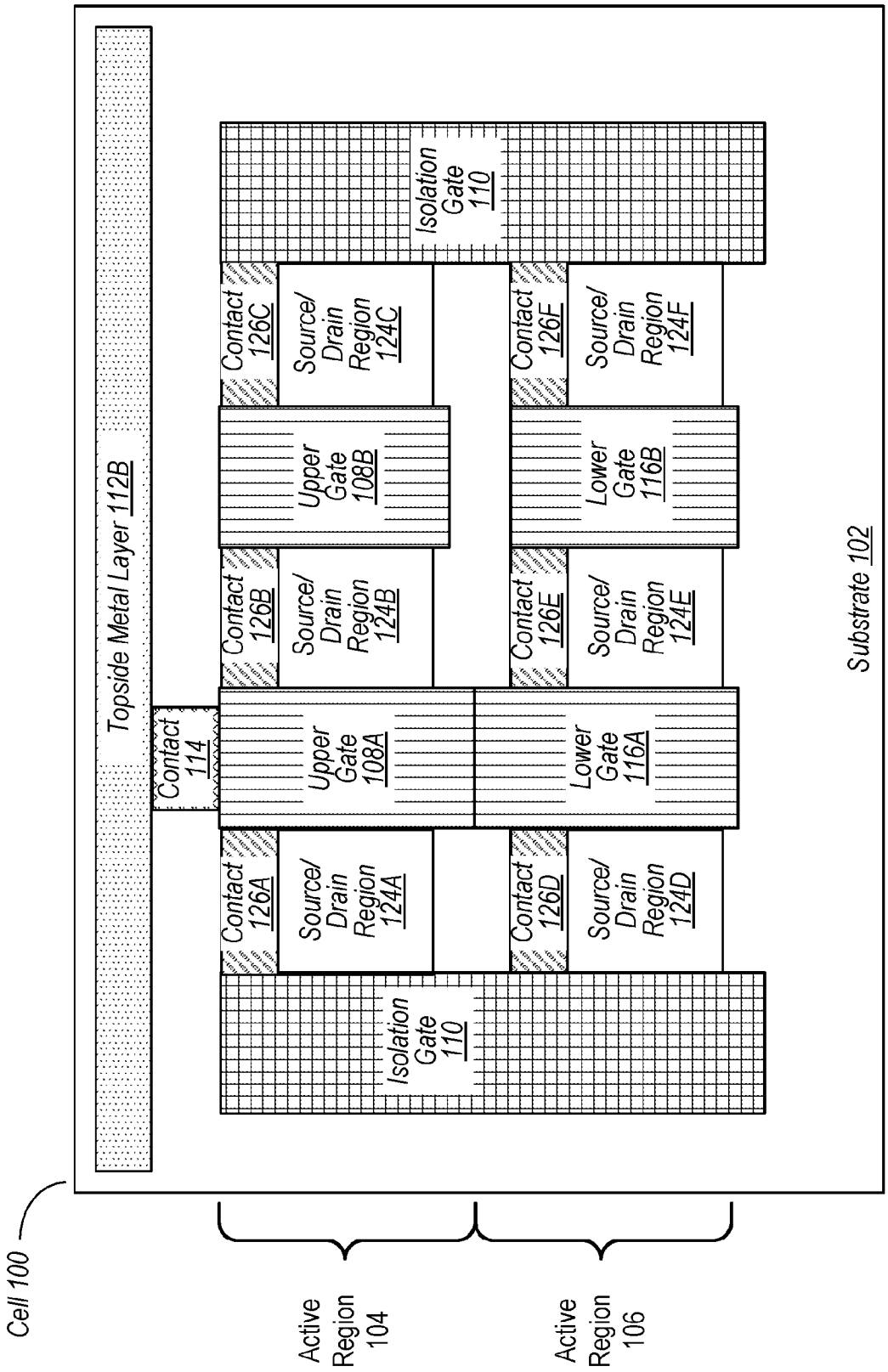

Cell 100
Topside Metal Layer 112B
Substrate 102
Isolation Gate 110
Contact 126C
Source/ Drain Region 124C
Contact 126F
Source/ Drain Region 124F
Upper Gate 108B
Lower Gate 116B
Contact 126B
Source/ Drain Region 124B
Contact 126E
Source/ Drain Region 124E
Contact 114
Upper Gate 108A
Lower Gate 116A
Contact 126A
Source/ Drain Region 124A
Contact 126D
Source/ Drain Region 124D
Isolation Gate 110
Active Region 104
Active Region 106

FIG. 3

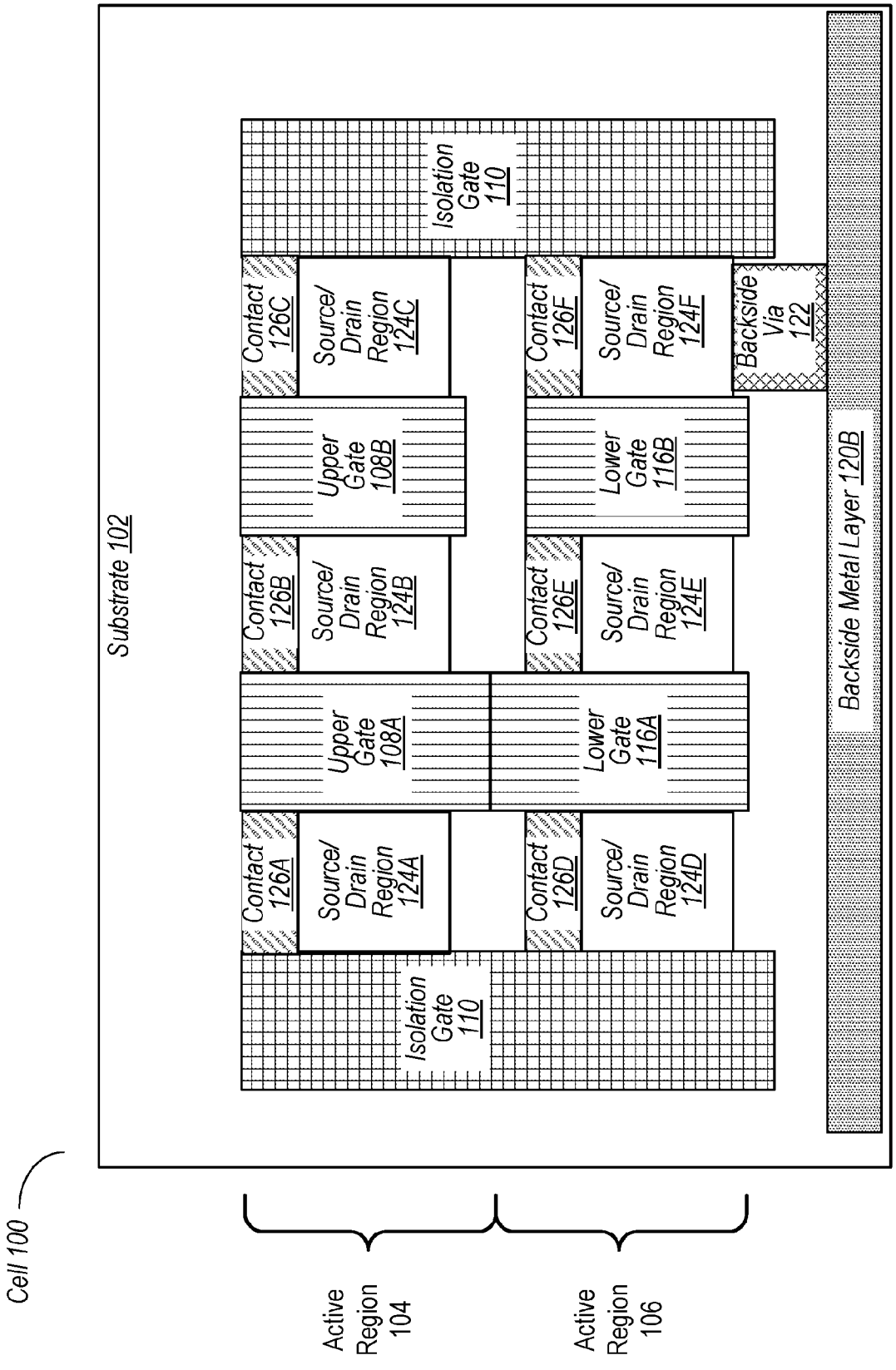

Cell 100
Substrate 102
Isolation Gate 110
Contact 126C
Source/ Drain Region 124C
Contact 126F
Source/ Drain Region 124F
Backside Via 122
Upper Gate 108B
Lower Gate 116B
Contact 126B
Source/ Drain Region 124B
Contact 126E
Source/ Drain Region 124E
Upper Gate 108A
Lower Gate 116A
Contact 126A
Source/ Drain Region 124A
Contact 126D
Source/ Drain Region 124D
Isolation Gate 110
Backside Metal Layer 120B
Active Region 104
Active Region 106

FIG. 4

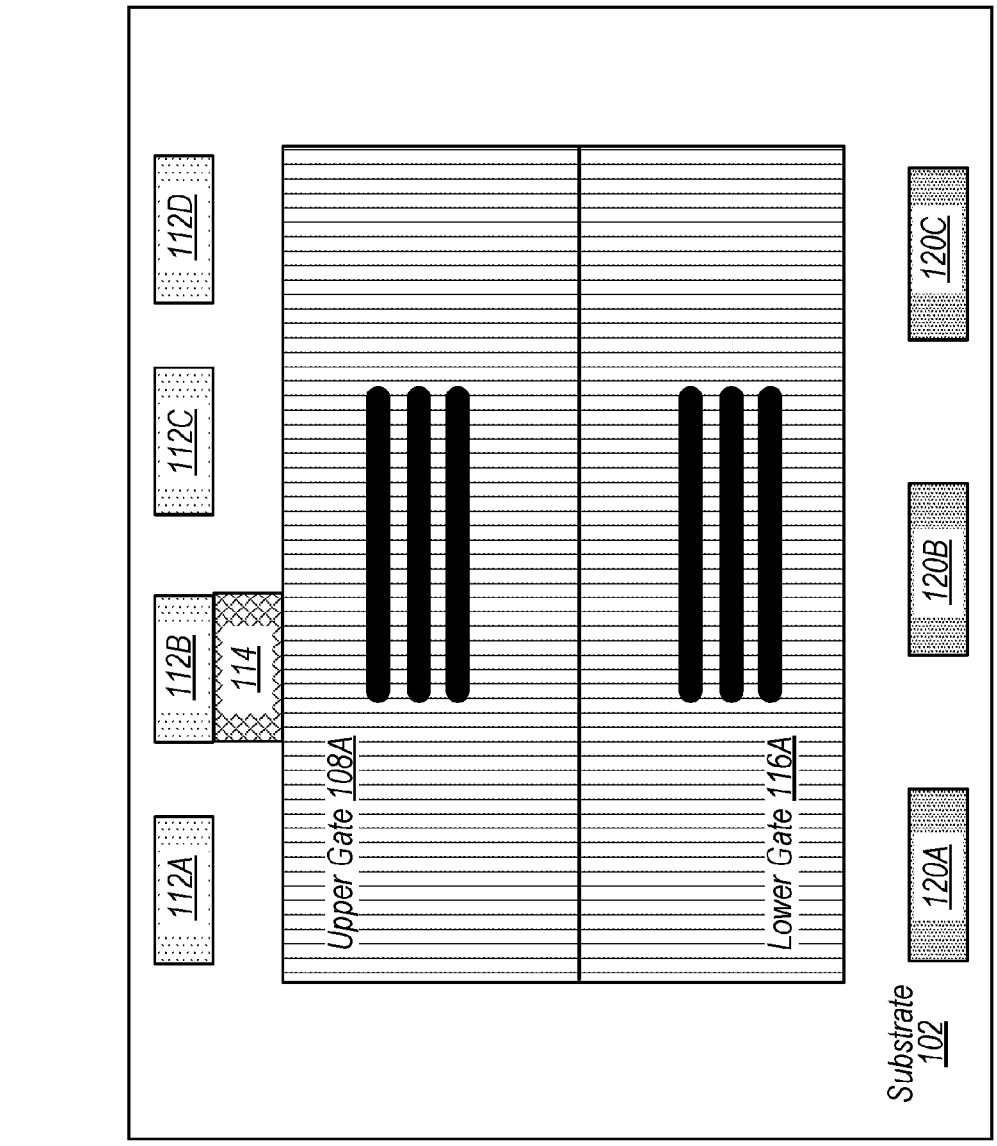

Cell 100
112A
112B
114
112C
112D
Upper Gate 108A
Lower Gate 116A
120A
120B
120C
Substrate 102

FIG. 5

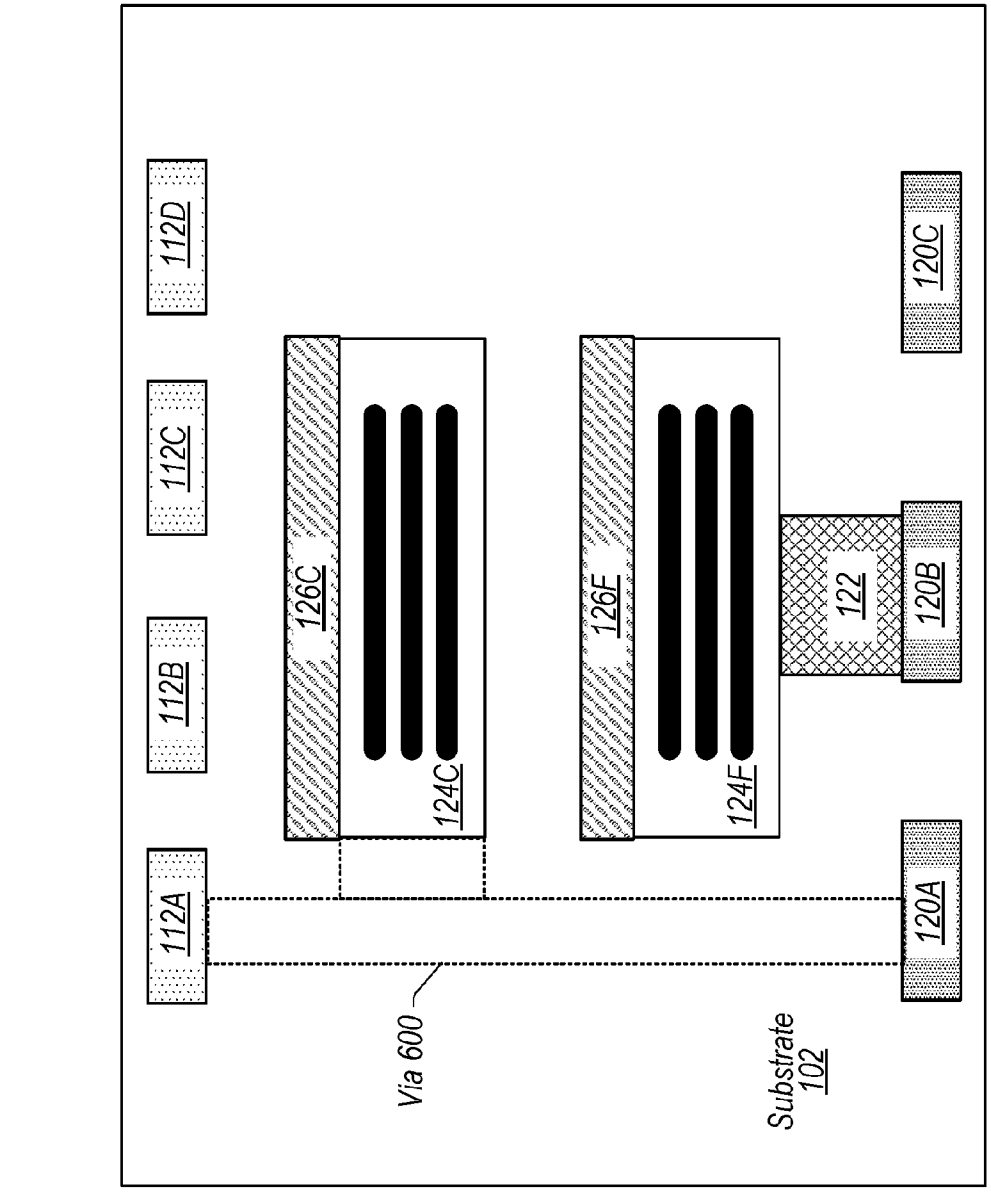

Cell 100
112A
112B
112C
112D
126C
124C
126F
124F
122
120A
120B
120C
Via 600
Substrate
102

FIG. 6

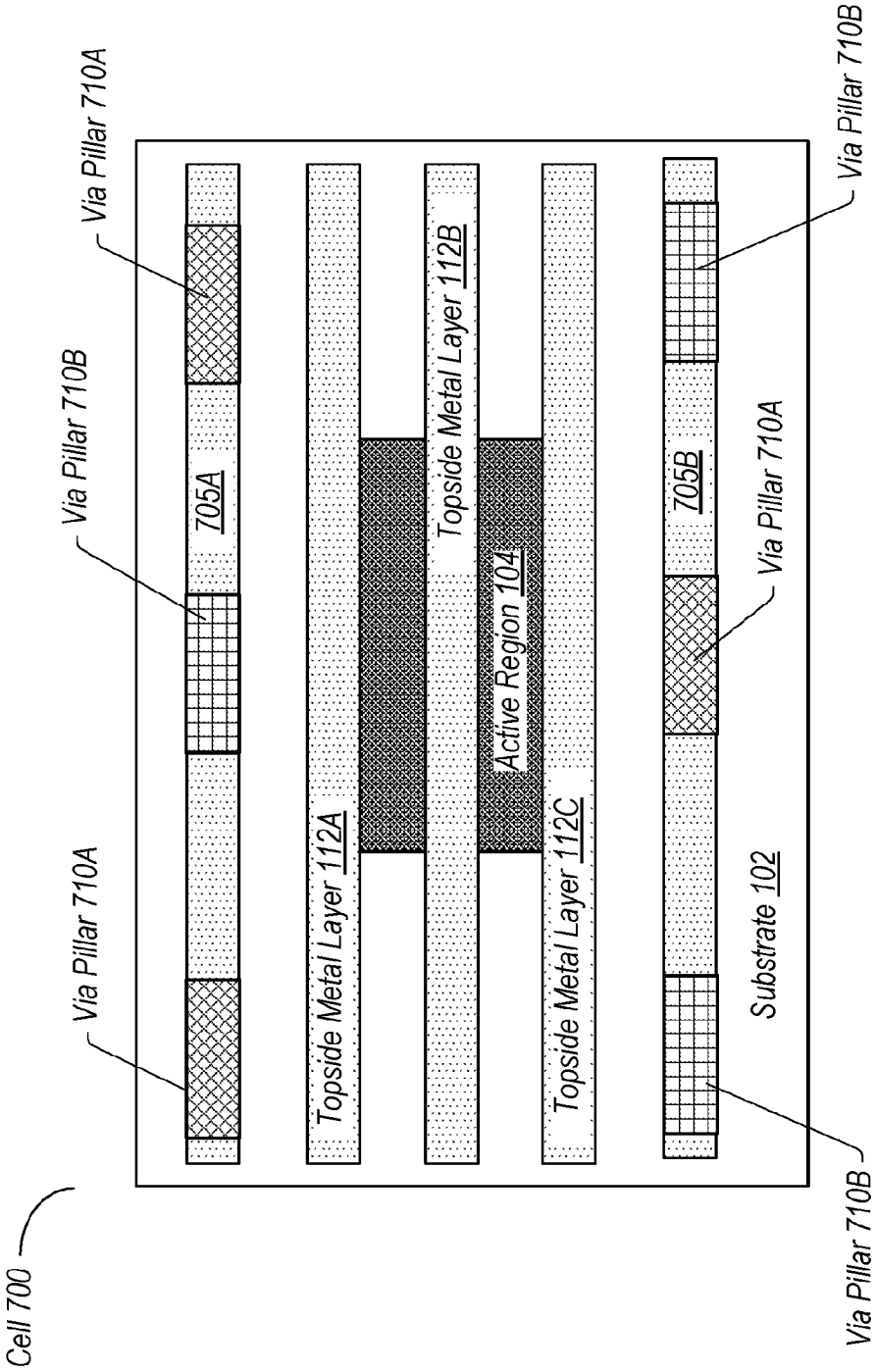

Cell 700
Via Pillar 710A
Via Pillar 710B
Via Pillar 710A
Via Pillar 710B
705A
Topside Metal Layer 112A
Topside Metal Layer 112B
Active Region 104
Topside Metal Layer 112C
705B
Via Pillar 710A
Via Pillar 710B
Substrate 102

FIG. 7

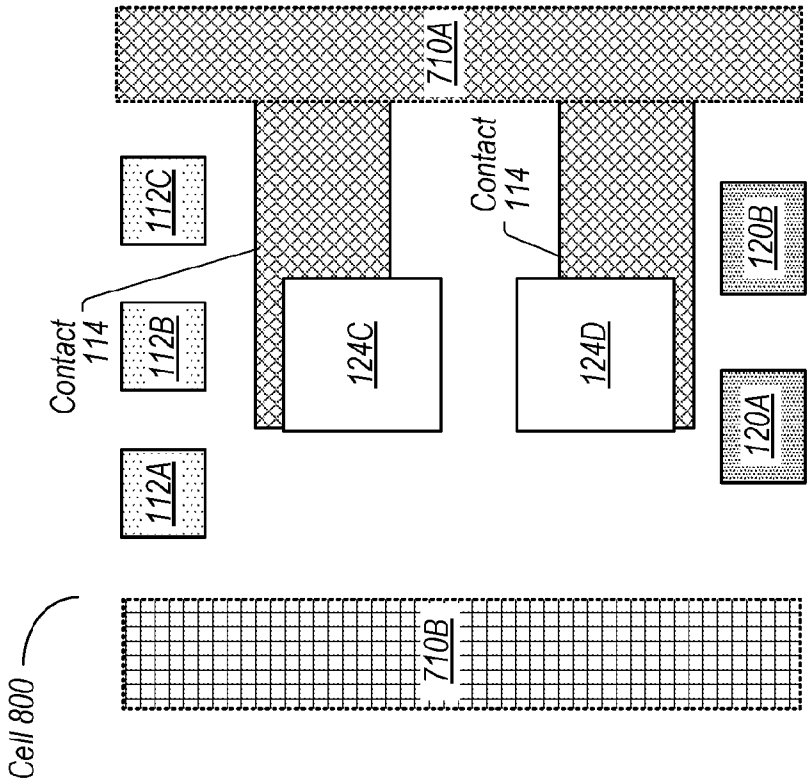

Cell 800
710B
710A
112A
112B
112C
Contact 114
124C
124D
120A
120B

FIG. 9

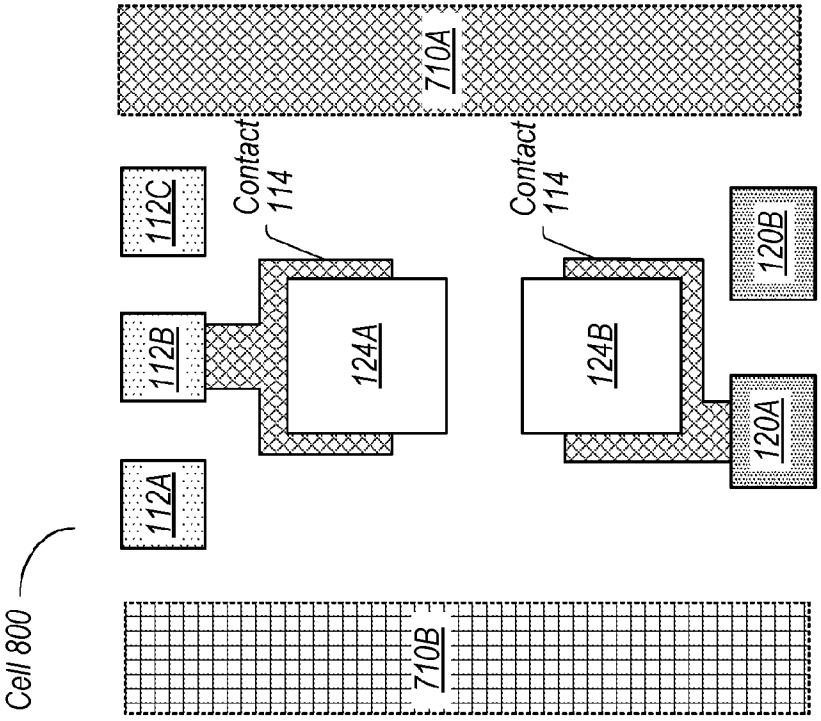

Cell 800
710B
710A
112A
112B
112C
Contact 114
Contact 114
124A
124B
120A
120B

FIG. 8

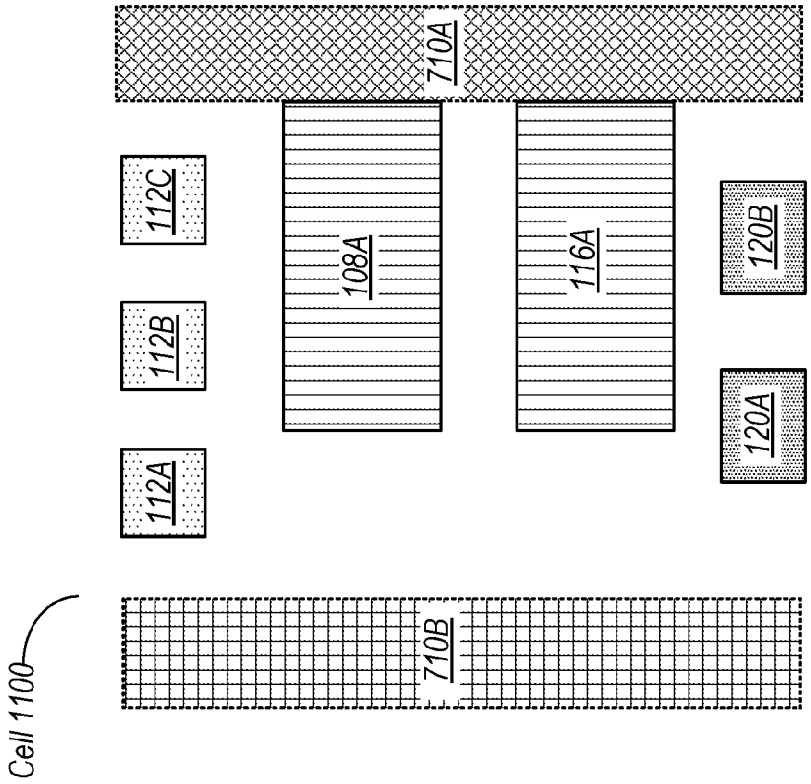

Cell 1100
710B
710A
112A
112B
112C
108A
116A
120A
120B

FIG. 11

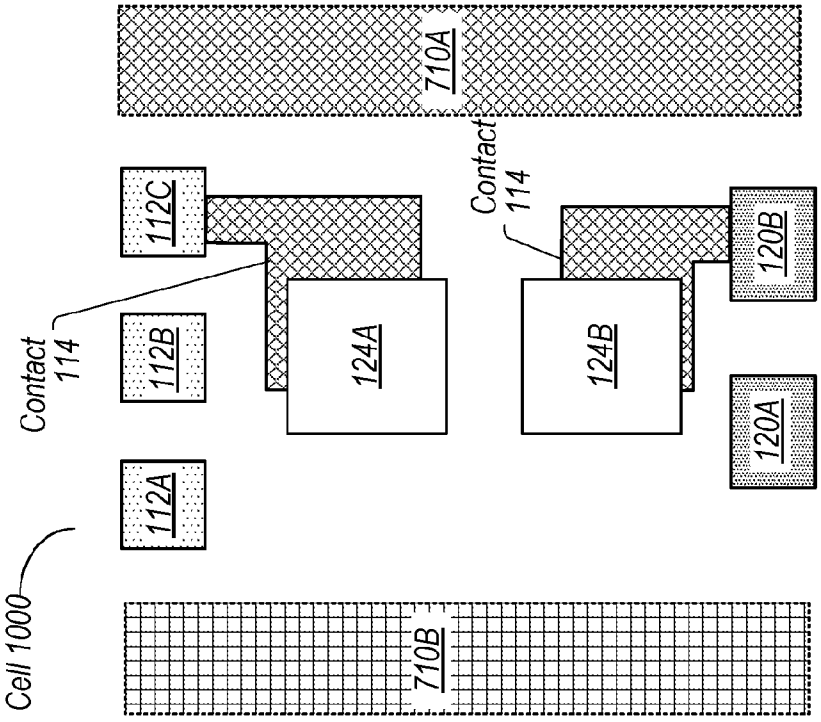

Cell 1000
710B
710A
112A
112B
112C
Contact 114
Contact 114
124A
124B
120A
120B

FIG. 10

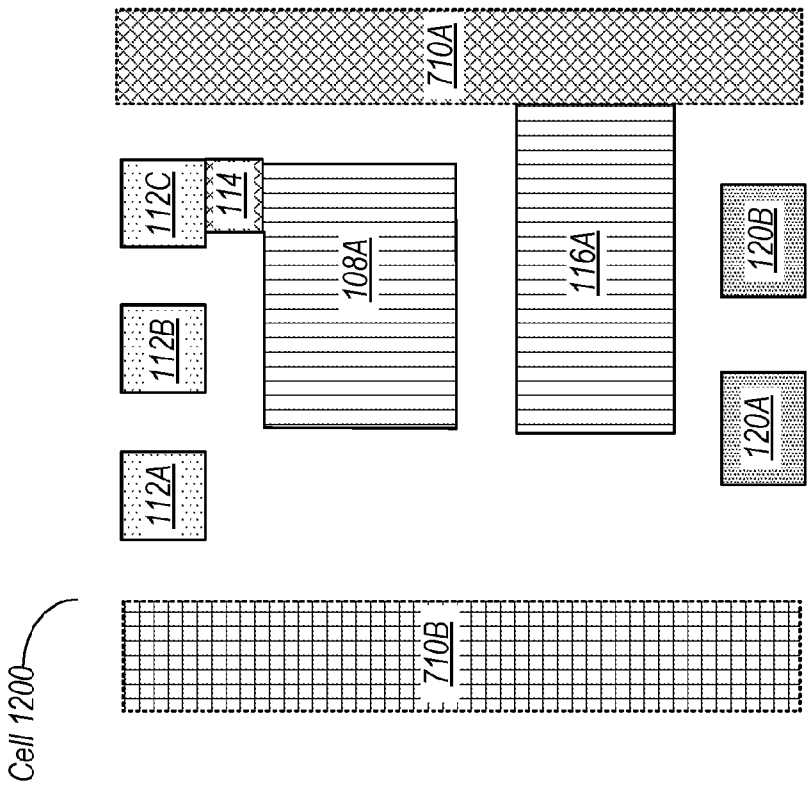


FIG. 12

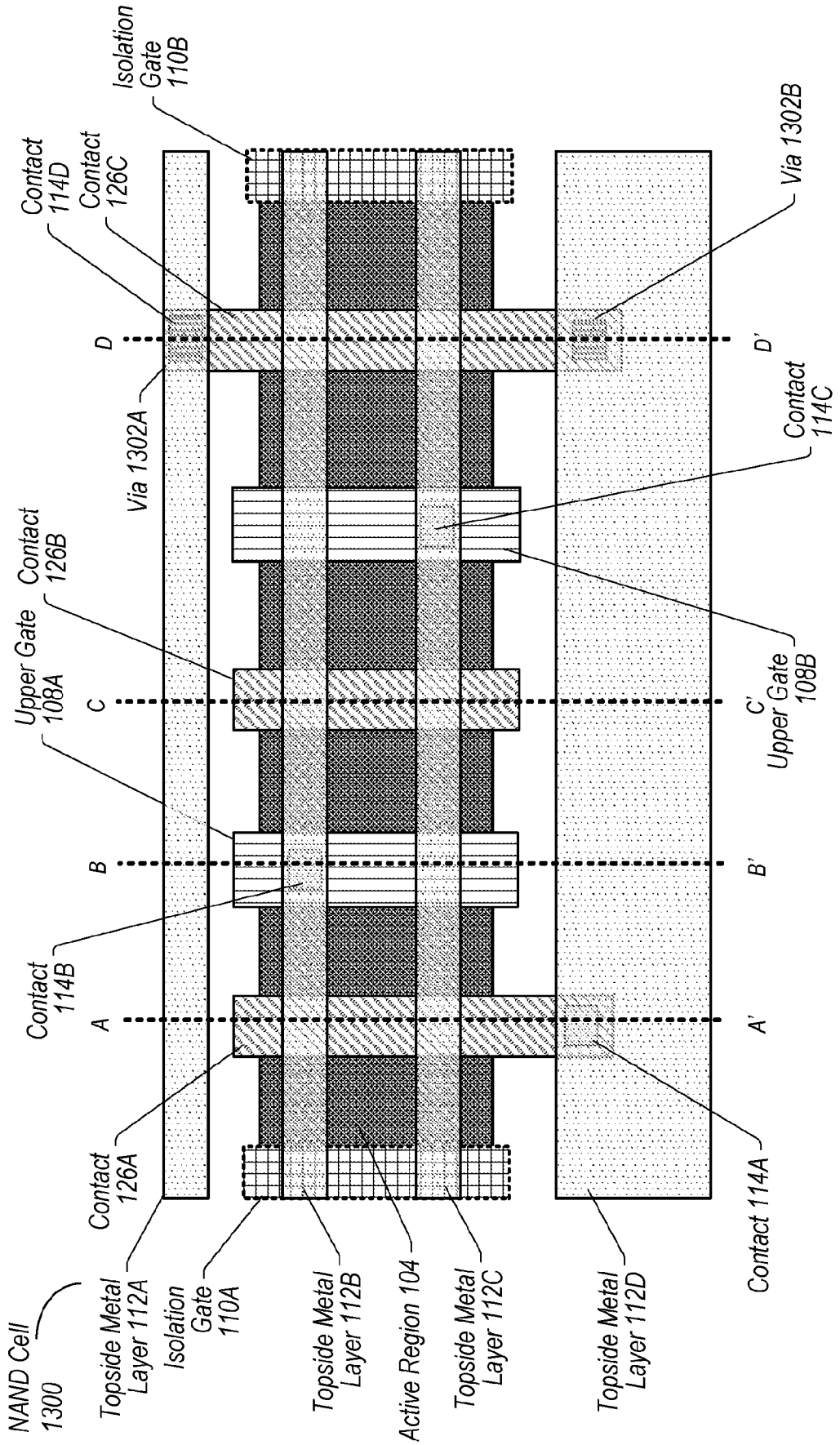

NAND Cell 1300
Topside Metal Layer 112A
Isolation Gate 110A
Topside Metal Layer 112B
Active Region 104
Topside Metal Layer 112C
Topside Metal Layer 112D
Contact 126A
Contact 114B
Upper Gate 108A
Contact 126B
Contact 114D
Contact 126C
Isolation Gate 110B
Via 1302A
Via 1302B
Contact 114C
Upper Gate 108B
Contact 114A
A
A'
B
B'
C
C'
D
D'

FIG. 13

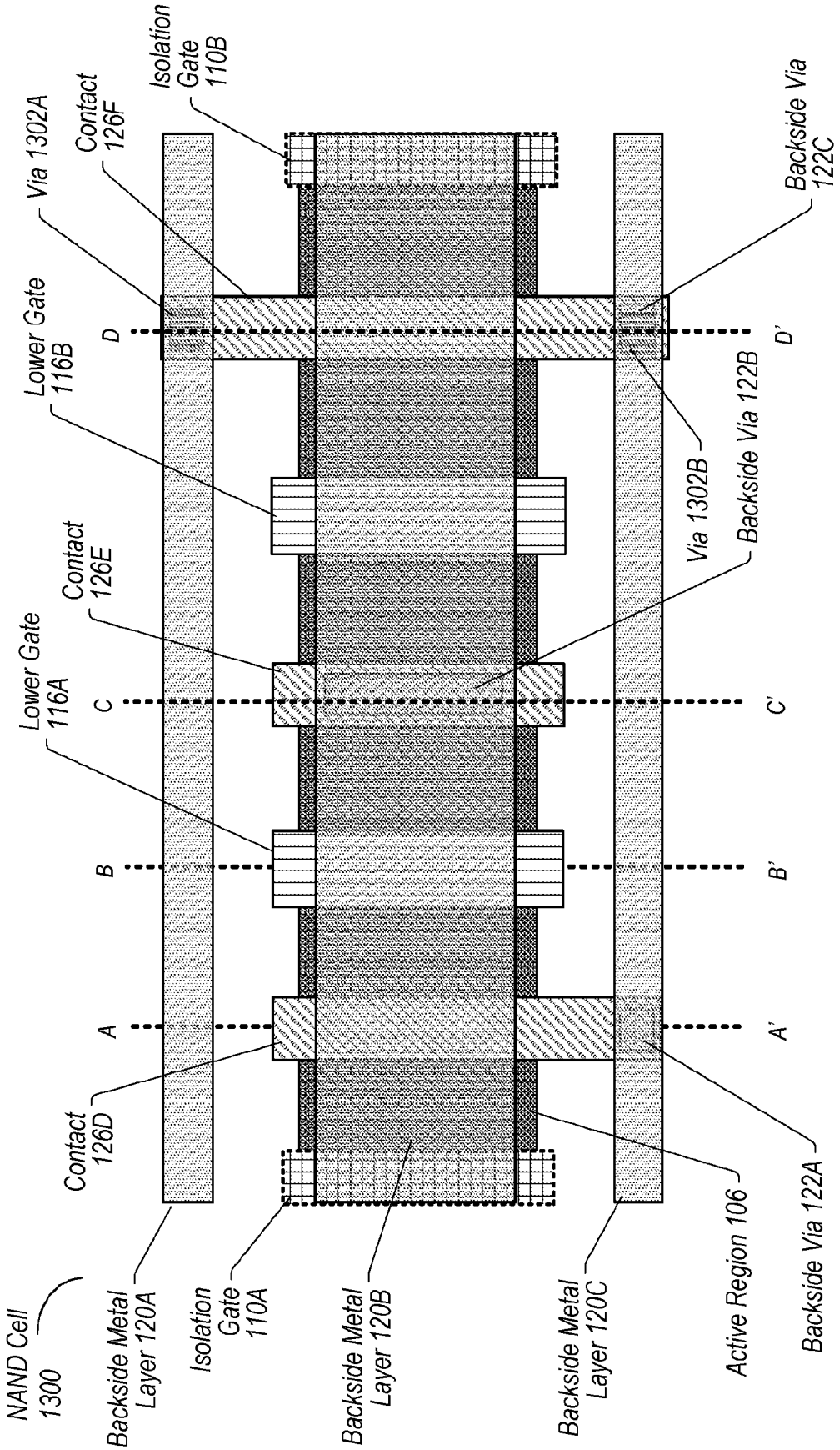

NAND Cell 1300
Backside Metal Layer 120A
Isolation Gate 110A
Backside Metal Layer 120B
Backside Metal Layer 120C
Active Region 106
Backside Via 122A
Contact 126D
Lower Gate 116A
Contact 126E
Lower Gate 116B
Via 1302A
Contact 126F
Isolation Gate 110B
Backside Via 122C
Via 1302B
Backside Via 122B
A
A'
B
B'
C
C'
D
D'

FIG. 14

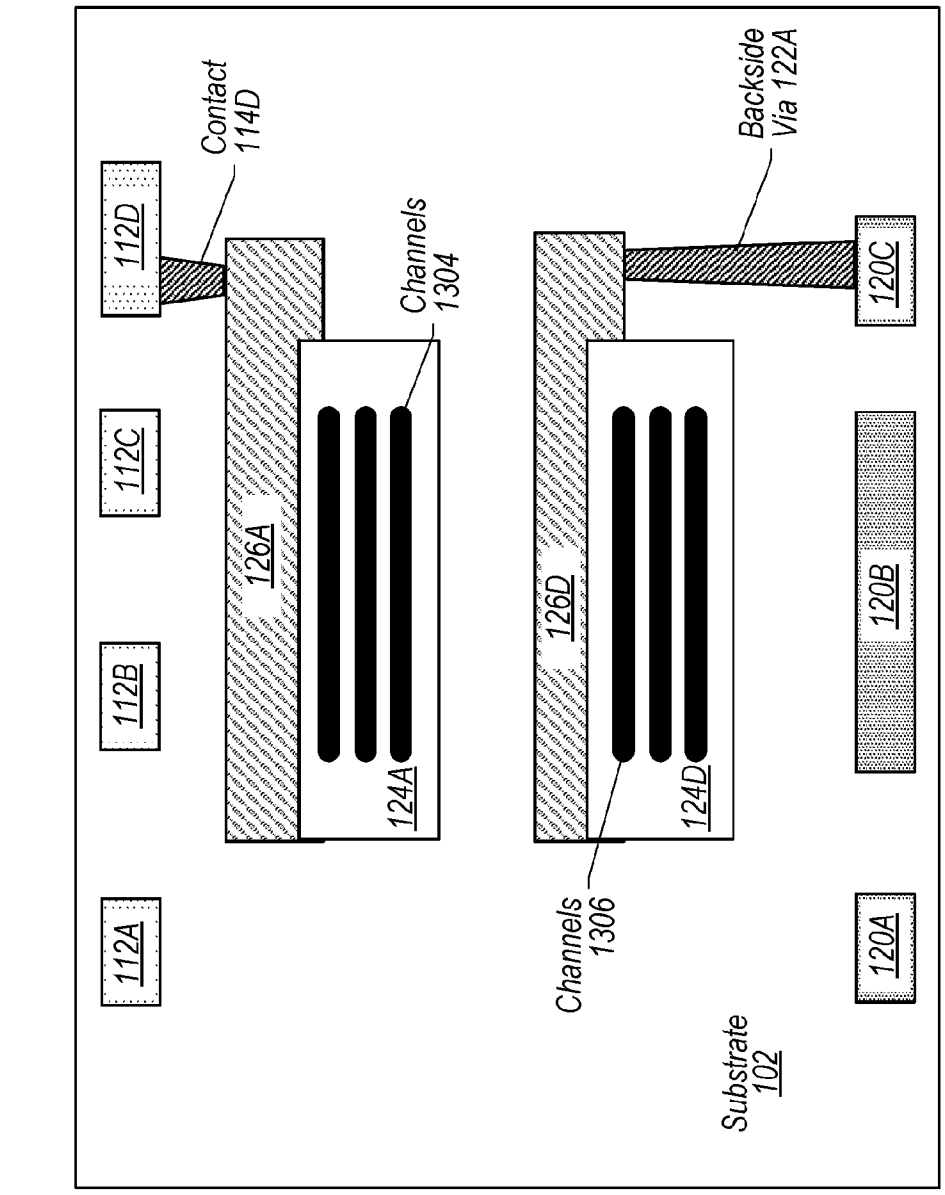

NAND Cell
1300
Substrate
102
112A
112B
112C
112D
120A
120B
120C
124A
124D
126A
126D
Contact
114D
Channels
1304
Channels
1306
Backside
Via 122A

FIG. 15

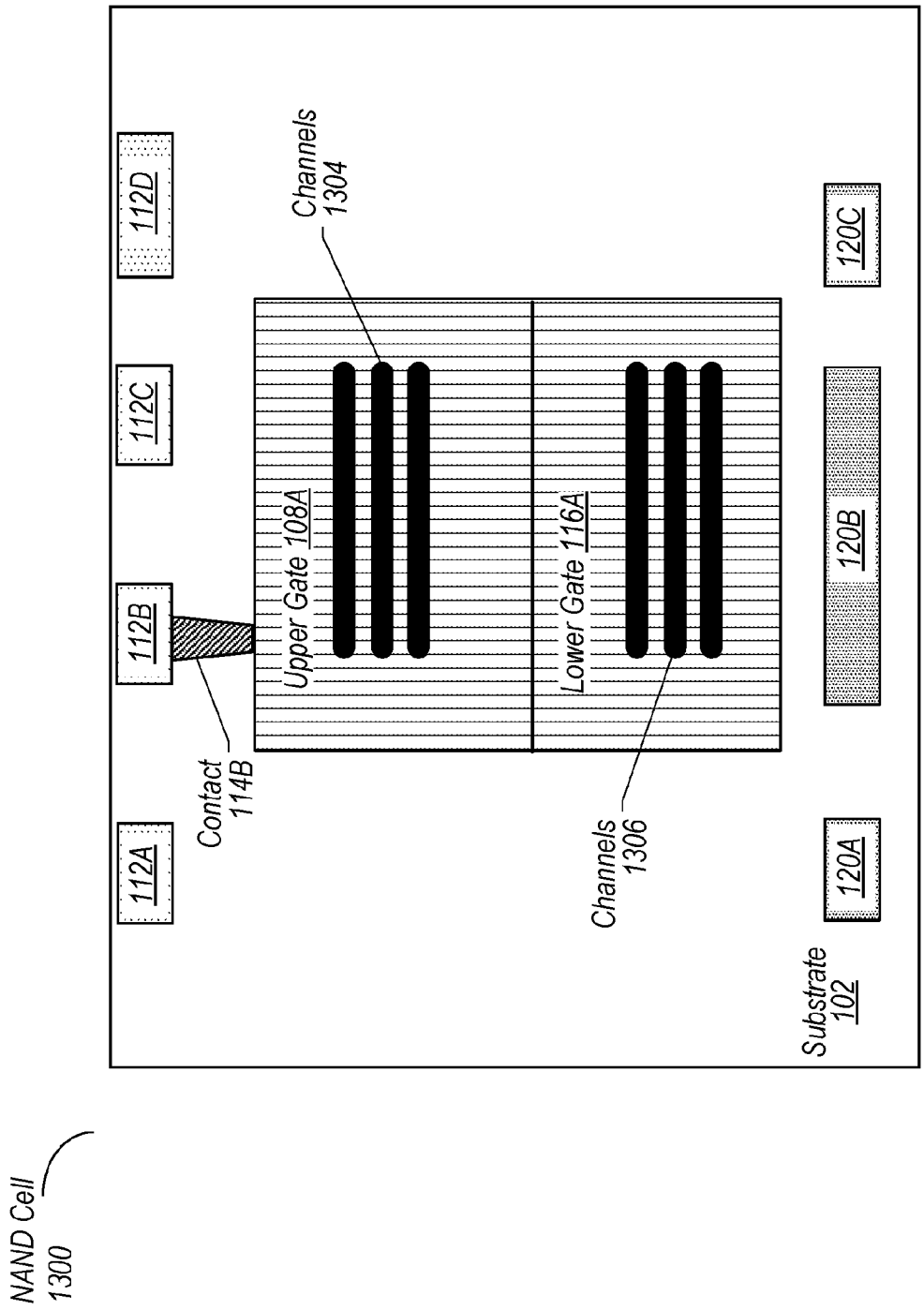

NAND Cell
1300
Substrate
102
112A
112B
112C
112D
120A
120B
120C
Contact
114B
Upper Gate 108A
Lower Gate 116A
Channels
1304
Channels
1306

FIG. 16

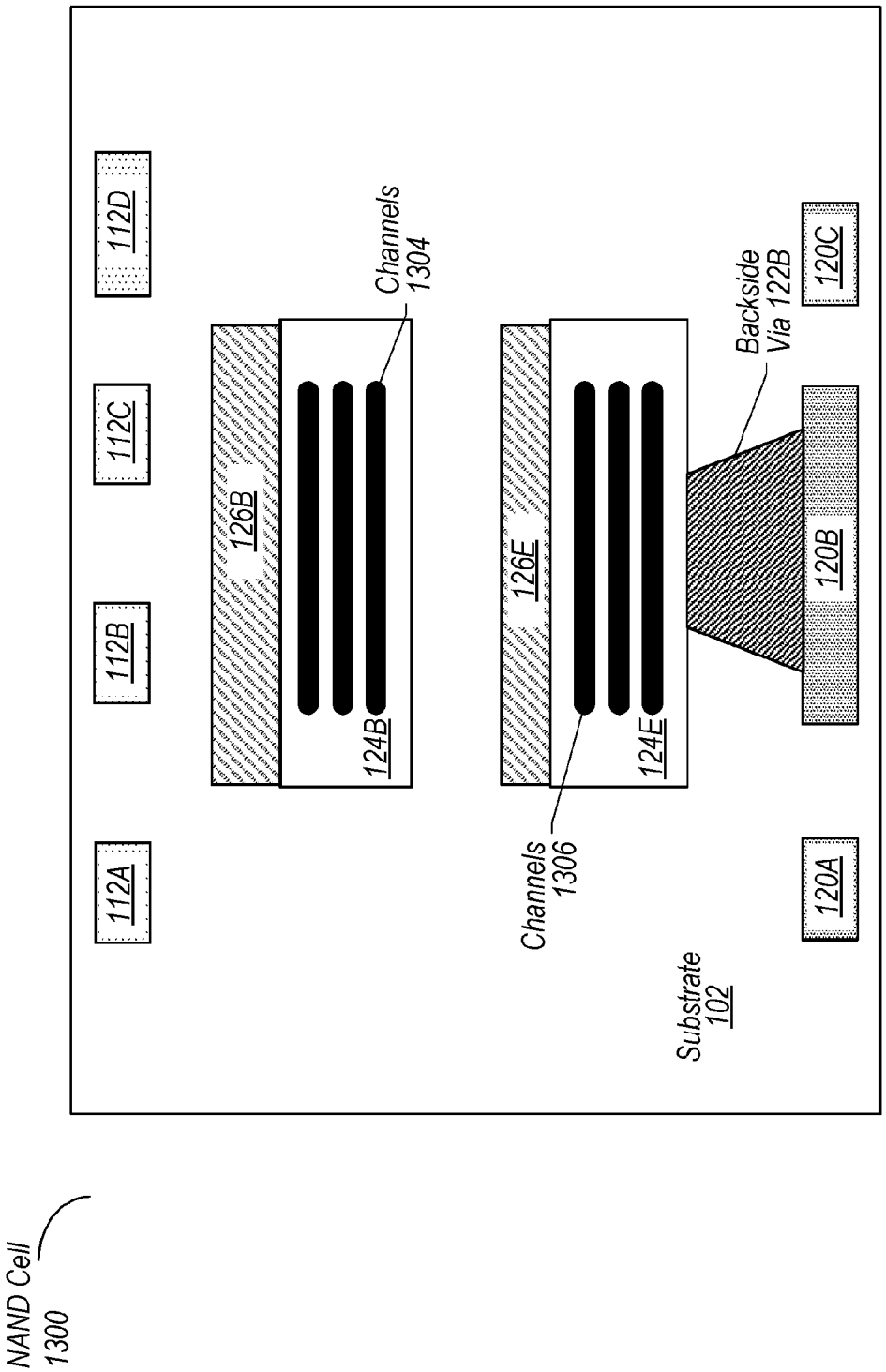

NAND Cell
1300
112A
112B
112C
112D
126B
124B
Channels
1304
126E
124E
Channels
1306
Backside
Via 122B
120A
120B
120C
Substrate
102

FIG. 17

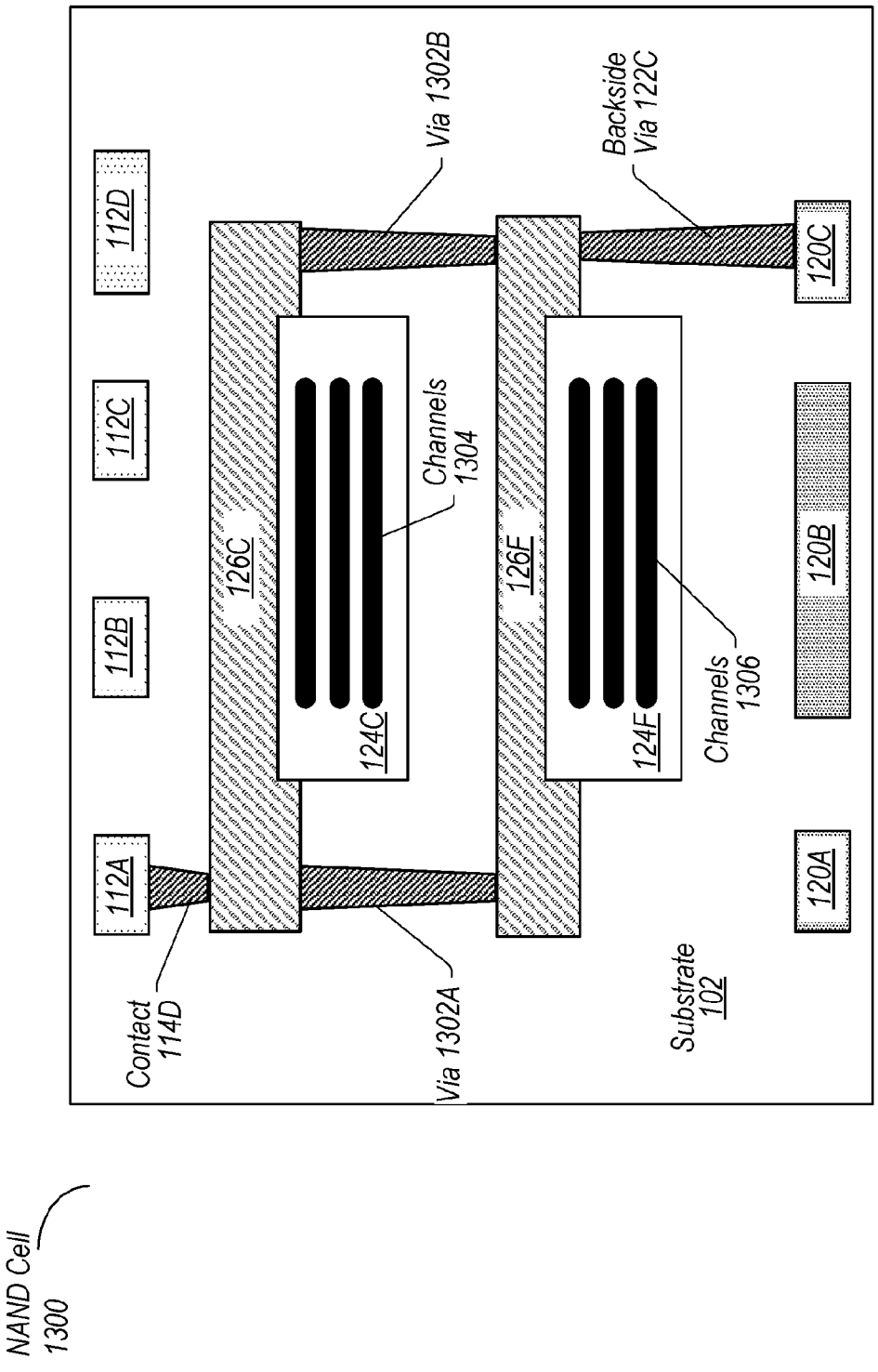

NAND Cell
1300
Contact
114D
Via 1302A
Via 1302B
Backside
Via 122C
Channels
1304
Channels
1306
Substrate
102
112A
112B
112C
112D
120A
120B
120C
124C
124F
126C
126F

FIG. 18

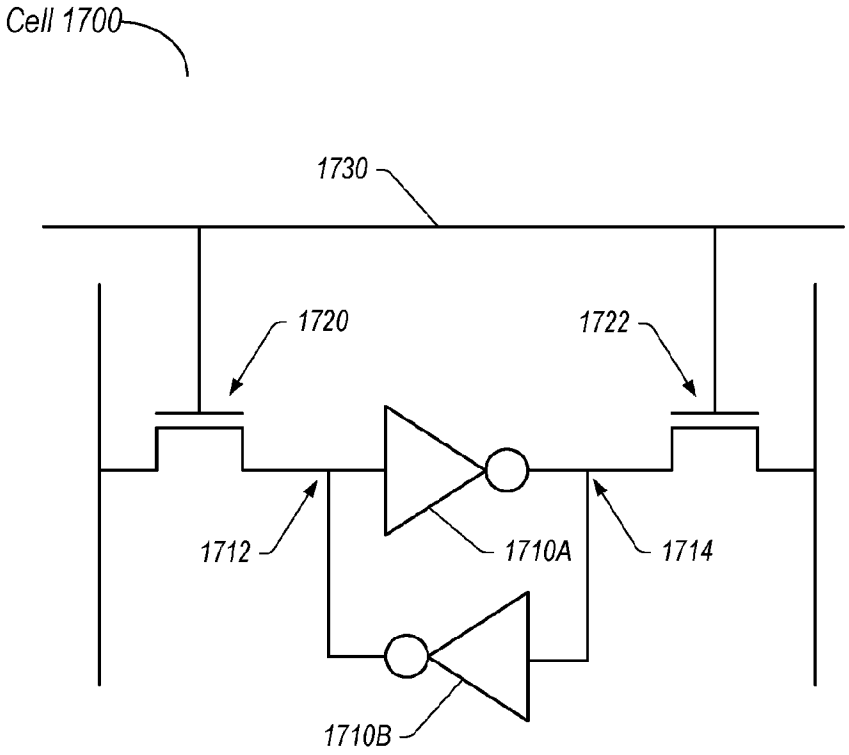


FIG. 19

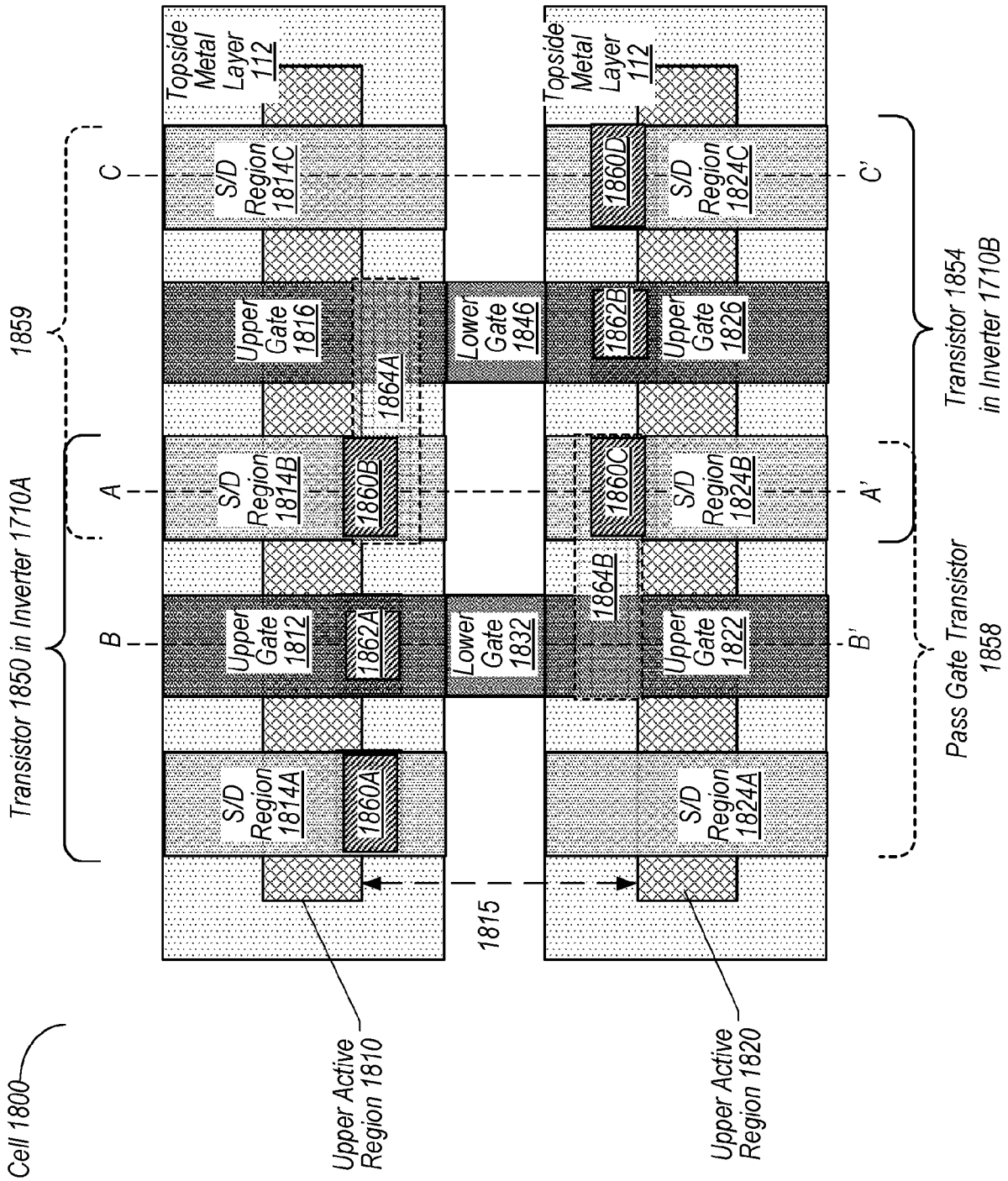

Cell 1800
Transistor 1850 in Inverter 1710A
Pass Gate Transistor 1859
Pass Gate Transistor 1858
Transistor 1854 in Inverter 1710B
Topside Metal Layer 112
Topside Metal Layer 112
S/D Region 1814A
S/D Region 1814B
S/D Region 1814C
S/D Region 1824A
S/D Region 1824B
S/D Region 1824C
Upper Gate 1812
Upper Gate 1816
Upper Gate 1822
Upper Gate 1826
Lower Gate 1832
Lower Gate 1846
1860A
1860B
1860C
1860D
1862A
1862B
1864A
1864B
1815
Upper Active Region 1810
Upper Active Region 1820
A
A'
B
B'
C
C'

FIG. 20

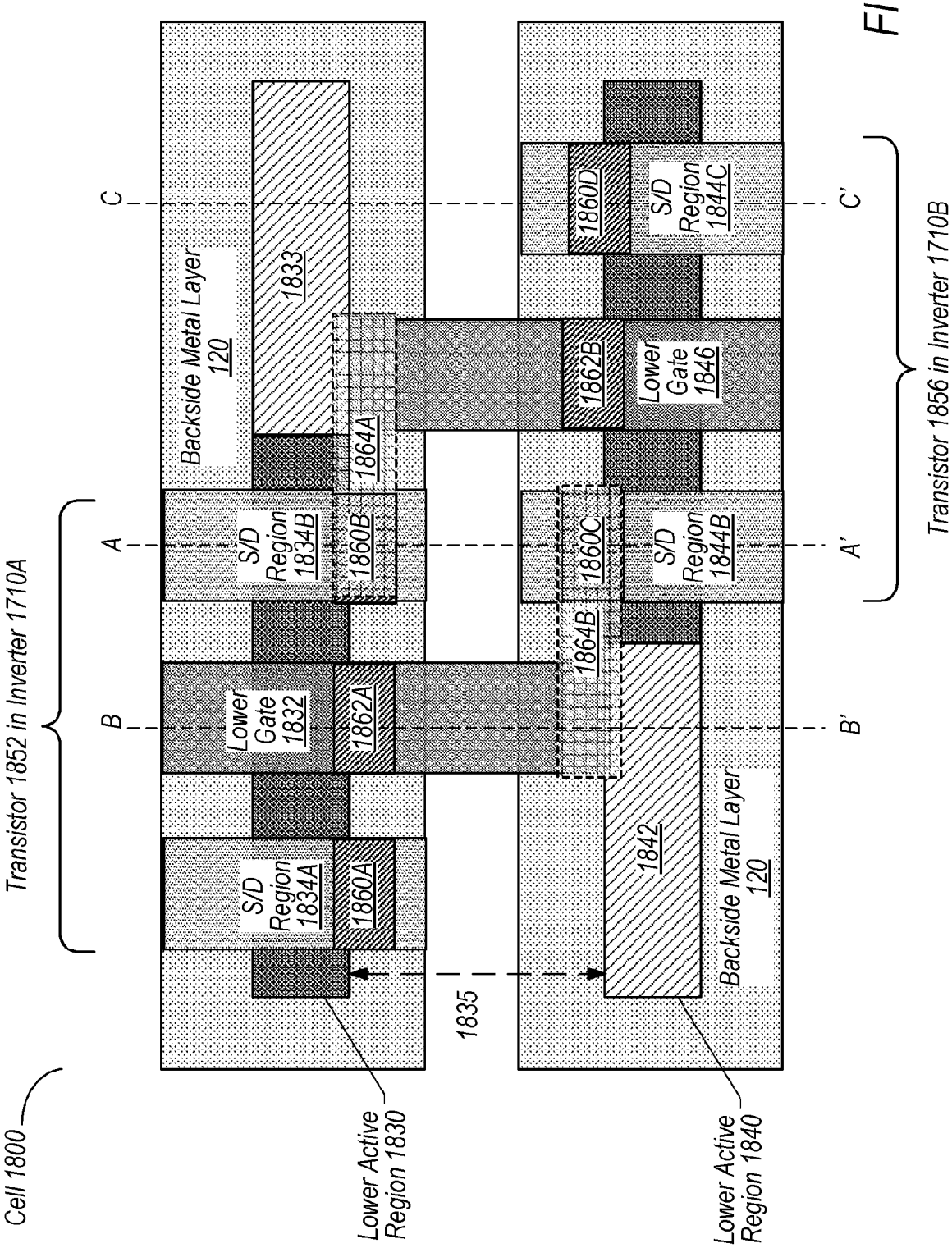

Cell 1800
Transistor 1852 in Inverter 1710A
Transistor 1856 in Inverter 1710B
Backside Metal Layer 120
Backside Metal Layer 120
A
A'
B
B'
C
C'
S/D Region 1834A
S/D Region 1834B
Lower Gate 1832
1833
1860A
1860B
1862A
1864A
1835
1842
1860C
1860D
1862B
1864B
S/D Region 1844B
S/D Region 1844C
Lower Gate 1846
Lower Active Region 1830
Lower Active Region 1840

FIG. 21

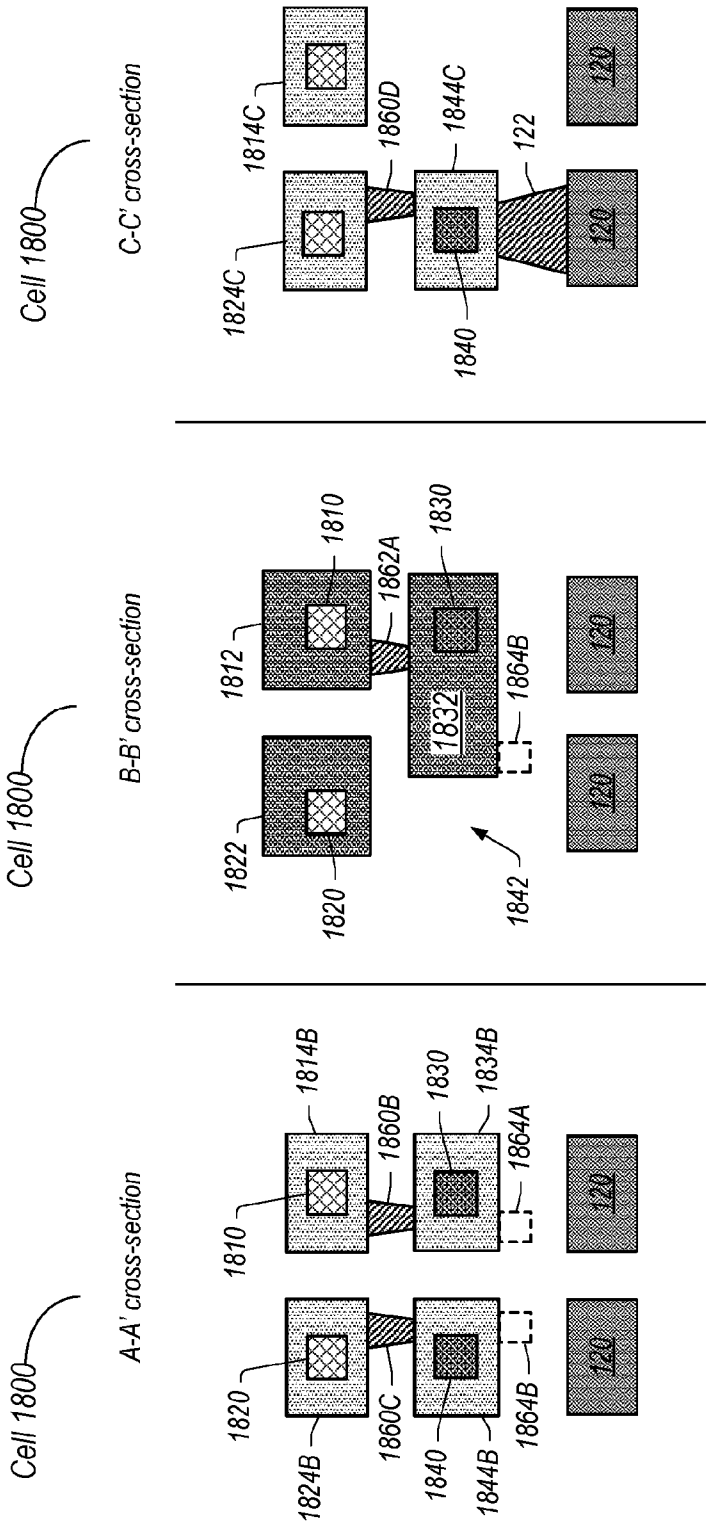


FIG. 22

FIG. 23

FIG. 24

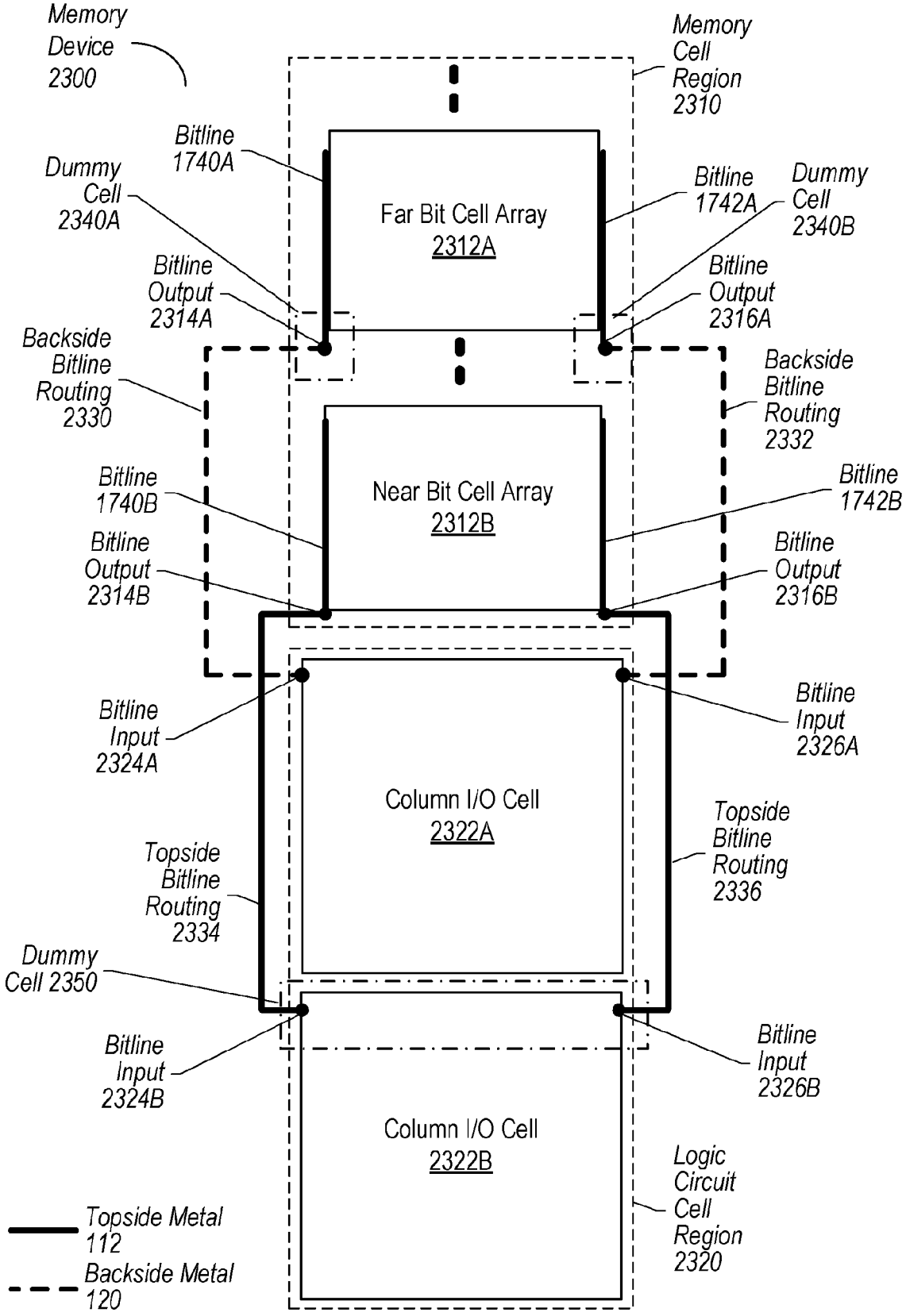

Memory Device 2300
Memory Cell Region 2310
Bitline 1740A
Dummy Cell 2340A
Bitline 1742A
Dummy Cell 2340B
Far Bit Cell Array 2312A
Bitline Output 2314A
Bitline Output 2316A
Backside Bitline Routing 2330
Backside Bitline Routing 2332
Near Bit Cell Array 2312B
Bitline 1740B
Bitline 1742B
Bitline Output 2314B
Bitline Output 2316B
Bitline Input 2324A
Bitline Input 2326A
Column I/O Cell 2322A
Topside Bitline Routing 2336
Topside Bitline Routing 2334
Dummy Cell 2350
Bitline Input 2324B
Bitline Input 2326B
Column I/O Cell 2322B
Logic Circuit Cell Region 2320
Topside Metal 112
Backside Metal 120

FIG. 25

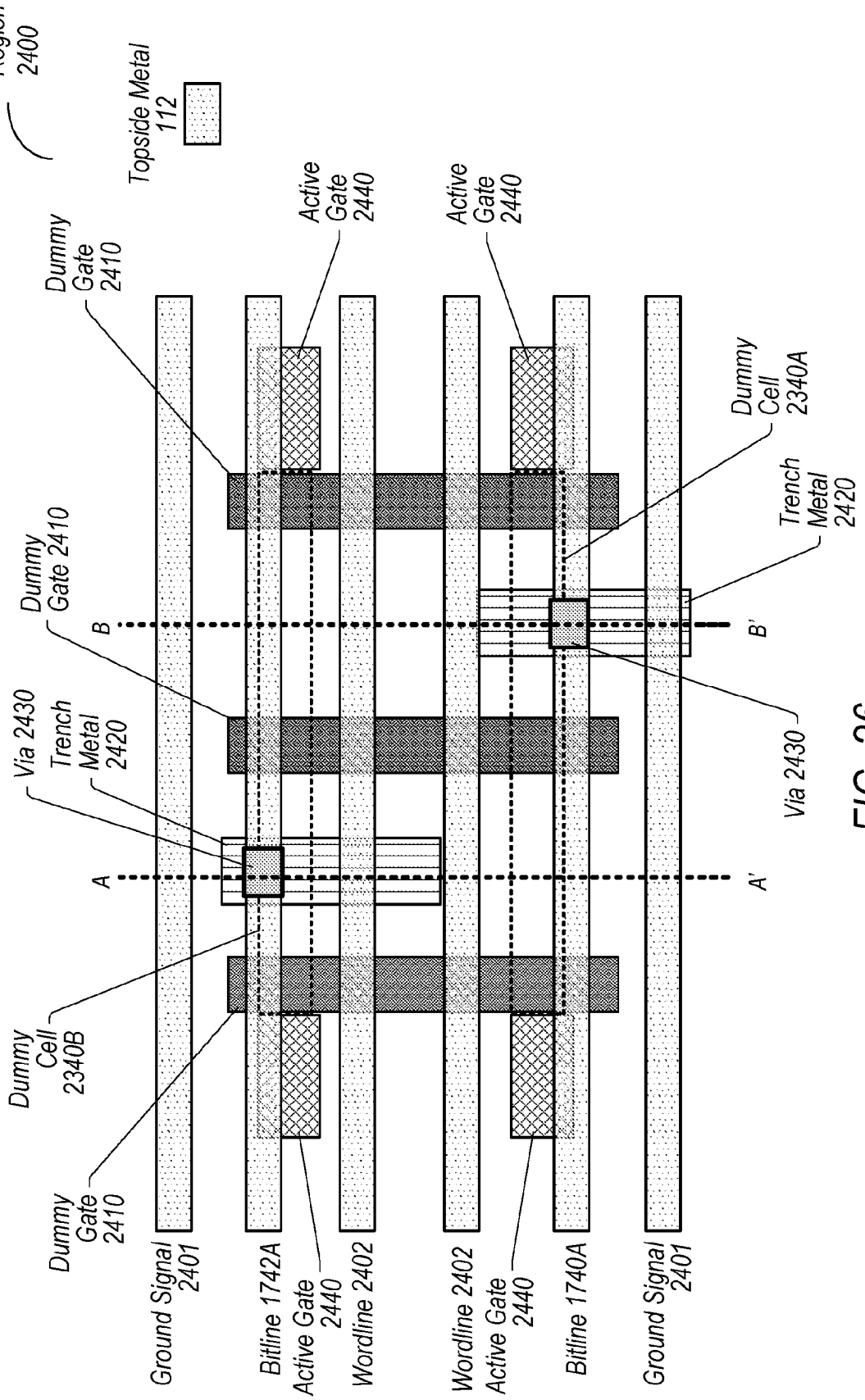

Region 2400
Topside Metal 112
Dummy Gate 2410
Active Gate 2440
Active Gate 2440
Dummy Gate 2410
Dummy Cell 2340A
Trench Metal 2420
B
B'
Via 2430
Trench Metal 2420
Via 2430
A
A'
Dummy Cell 2340B
Dummy Gate 2410
Ground Signal 2401
Bitline 1742A
Active Gate 2440
Wordline 2402
Wordline 2402
Active Gate 2440
Bitline 1740A
Ground Signal 2401

FIG. 26

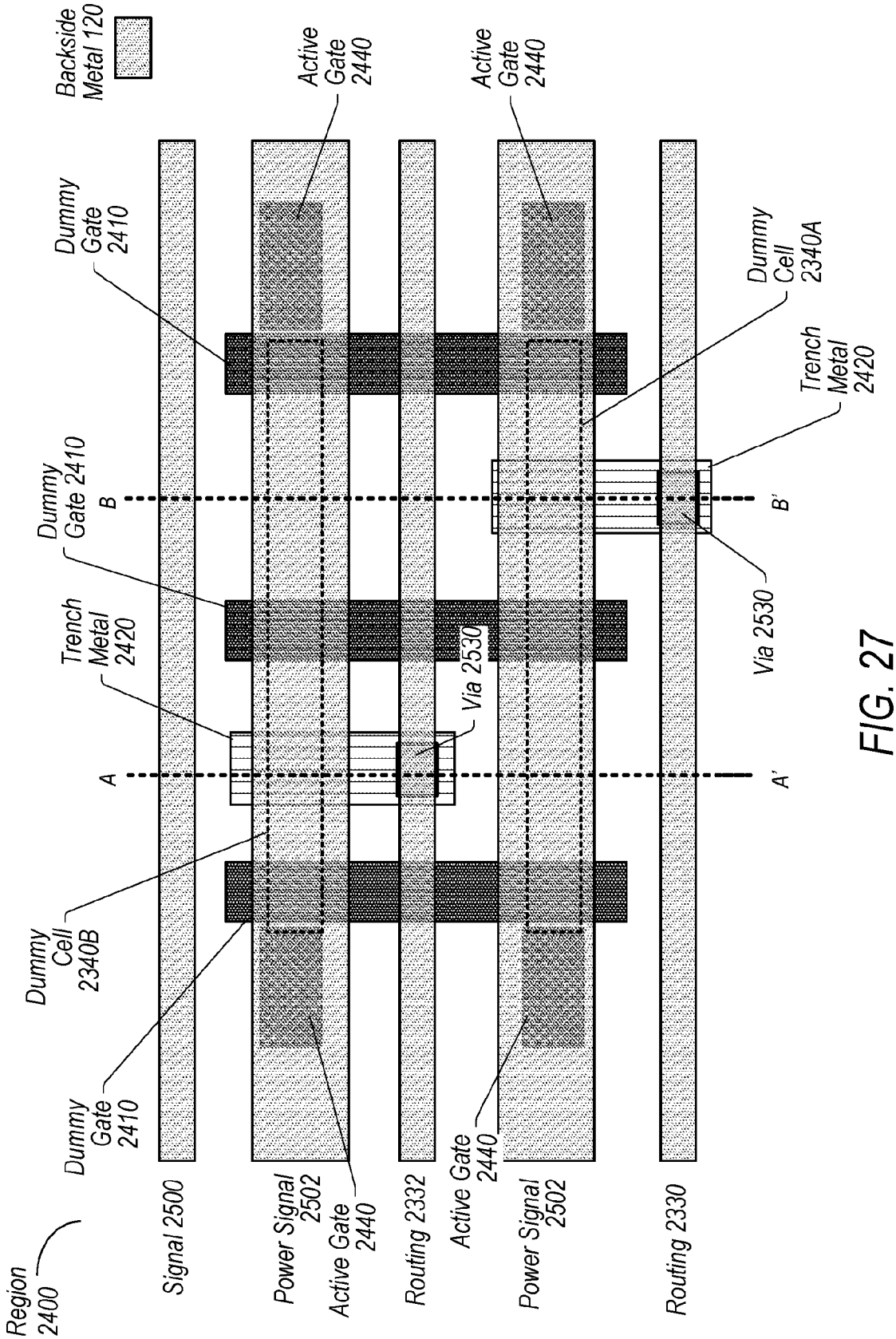

Backside Metal 120
Active Gate 2440
Active Gate 2440
Dummy Gate 2410
Dummy Cell 2340A
Dummy Gate 2410
B
B'
Trench Metal 2420
Trench Metal 2420
Via 2530
Via 2530
A
A'
Dummy Cell 2340B
Dummy Gate 2410
Region 2400
Signal 2500
Power Signal 2502
Active Gate 2440
Routing 2332
Active Gate 2440
Power Signal 2502
Routing 2330

FIG. 27

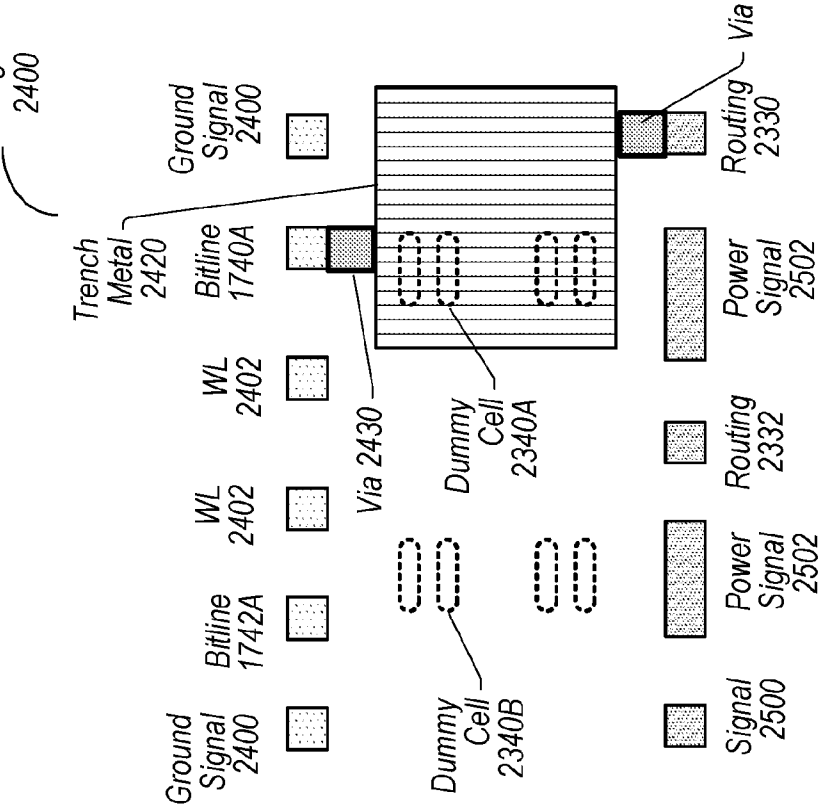

Region 2400
Trench Metal 2420
Ground Signal 2400
Bitline 1740A
WL 2402
WL 2402
Bitline 1742A
Ground Signal 2400
Via 2430
Dummy Cell 2340A
Dummy Cell 2340B
Via 2530
Routing 2330
Power Signal 2502
Routing 2332
Power Signal 2502
Signal 2500
B-B' x-section

FIG. 29

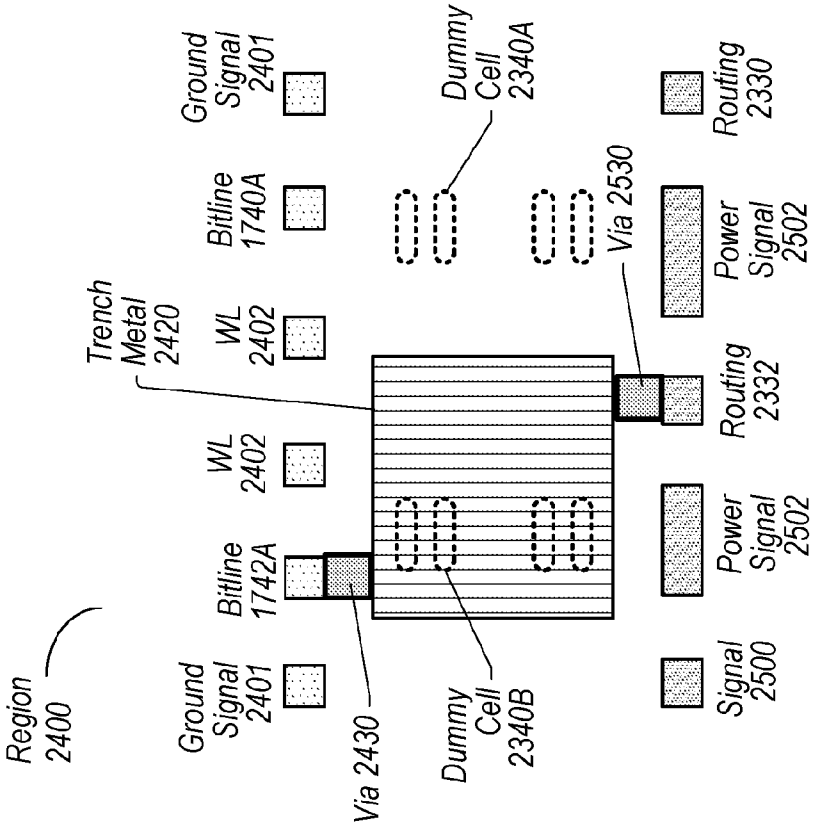

Region 2400
Trench Metal 2420
Ground Signal 2401
Bitline 1740A
WL 2402
WL 2402
Bitline 1742A
Ground Signal 2401
Via 2430
Dummy Cell 2340A
Dummy Cell 2340B
Via 2530
Routing 2330
Power Signal 2502
Routing 2332
Power Signal 2502
Signal 2500
A-A' x-section

FIG. 28

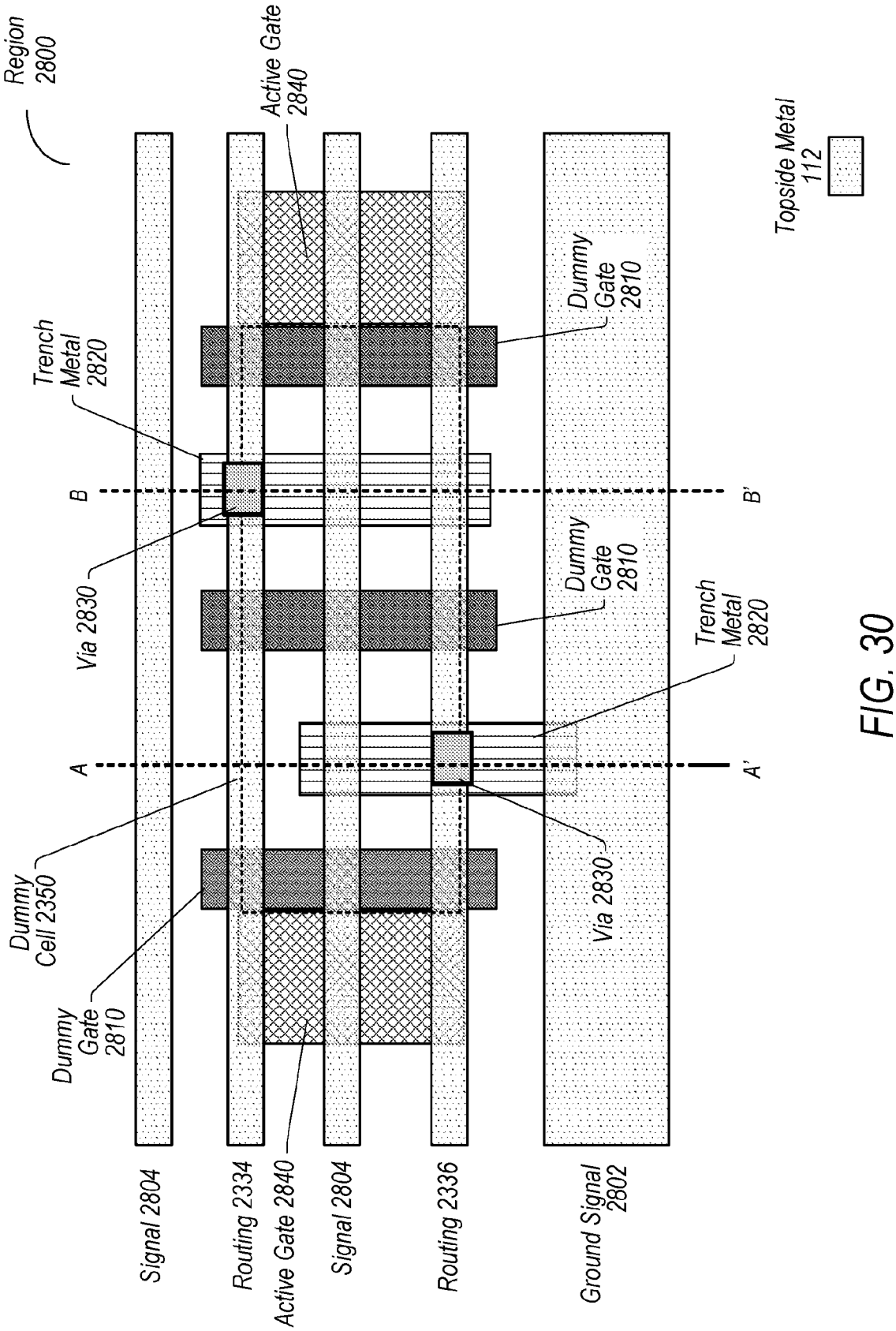

Region 2800
Active Gate 2840
Topside Metal 112
Trench Metal 2820
Dummy Gate 2810
B
B'
Via 2830
Dummy Gate 2810
Trench Metal 2820
A
A'
Dummy Cell 2350
Via 2830
Dummy Gate 2810
Signal 2804
Routing 2334
Active Gate 2840
Signal 2804
Routing 2336
Ground Signal 2802

FIG. 30

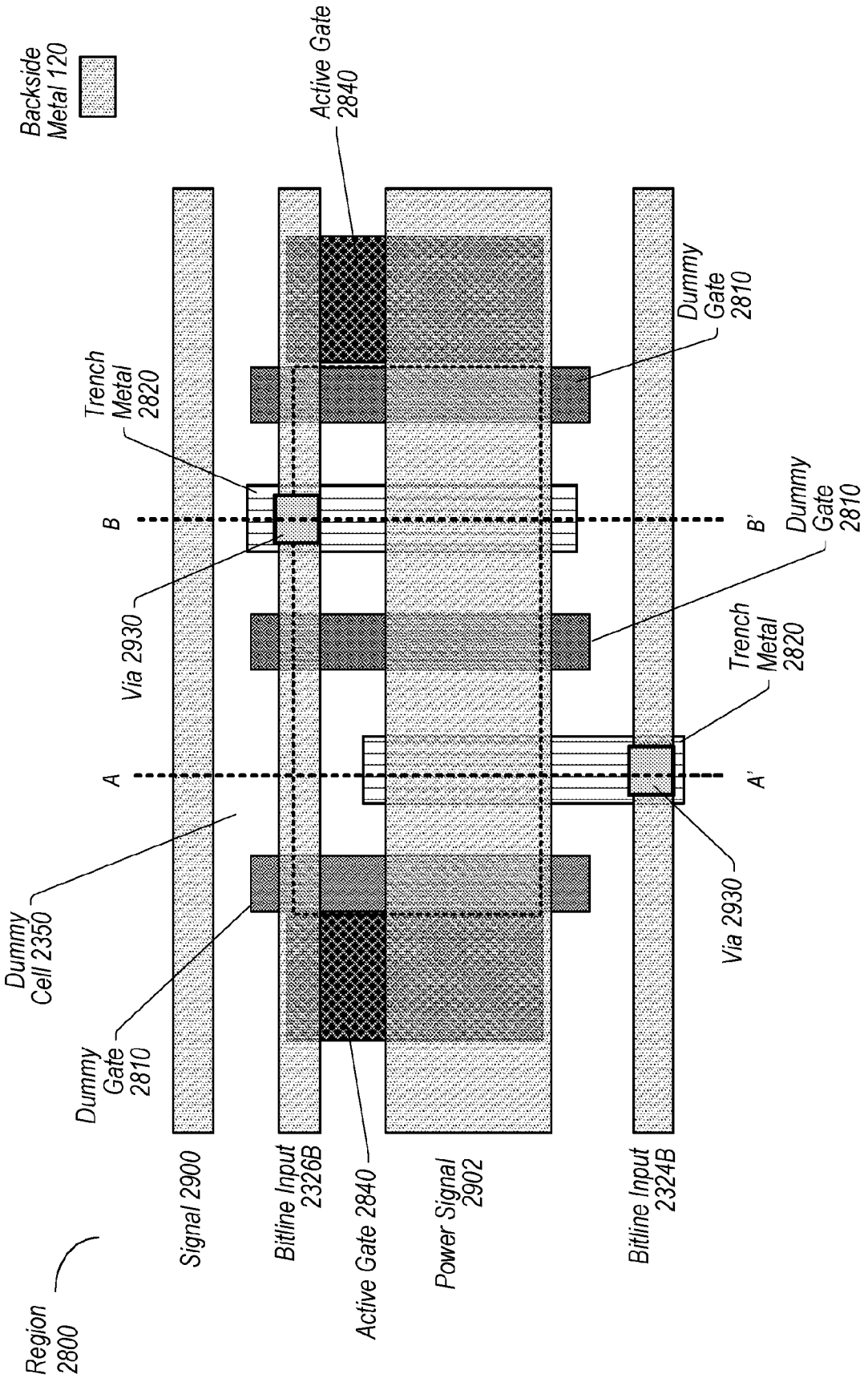

Backside Metal 120
Active Gate 2840
Dummy Gate 2810
Trench Metal 2820
B
B'
Via 2930
Dummy Gate 2810
Trench Metal 2820
A
A'
Dummy Cell 2350
Via 2930
Dummy Gate 2810
Region 2800
Signal 2900
Bitline Input 2326B
Active Gate 2840
Power Signal 2902
Bitline Input 2324B

FIG. 31

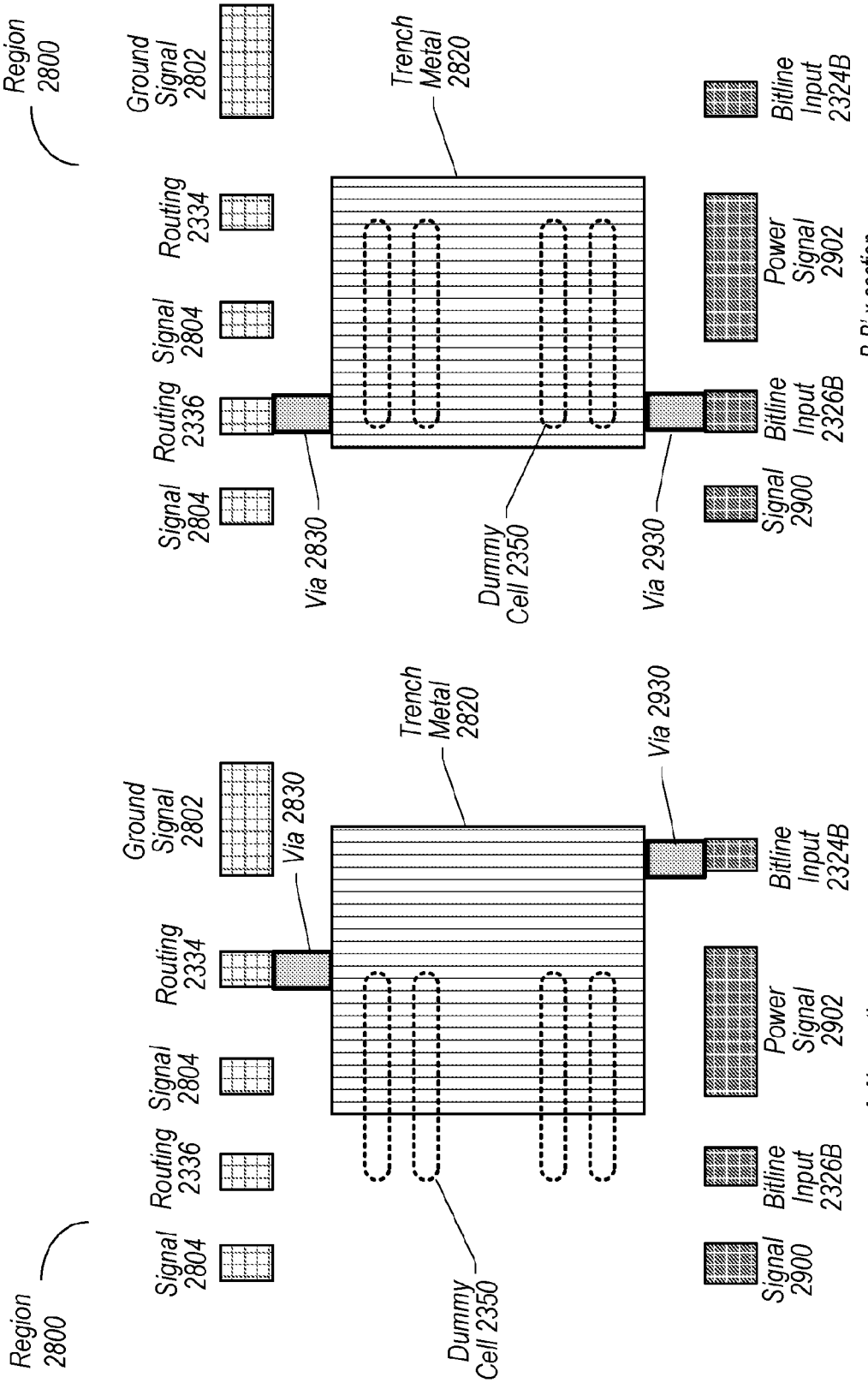

Region 2800
Ground Signal 2802
Routing 2334
Signal 2804
Routing 2336
Signal 2804
Trench Metal 2820
Via 2830
Dummy Cell 2350
Via 2930
Bitline Input 2324B
Power Signal 2902
Bitline Input 2326B
Signal 2900
A-A' x-section
B-B' x-section

FIG. 32

FIG. 33

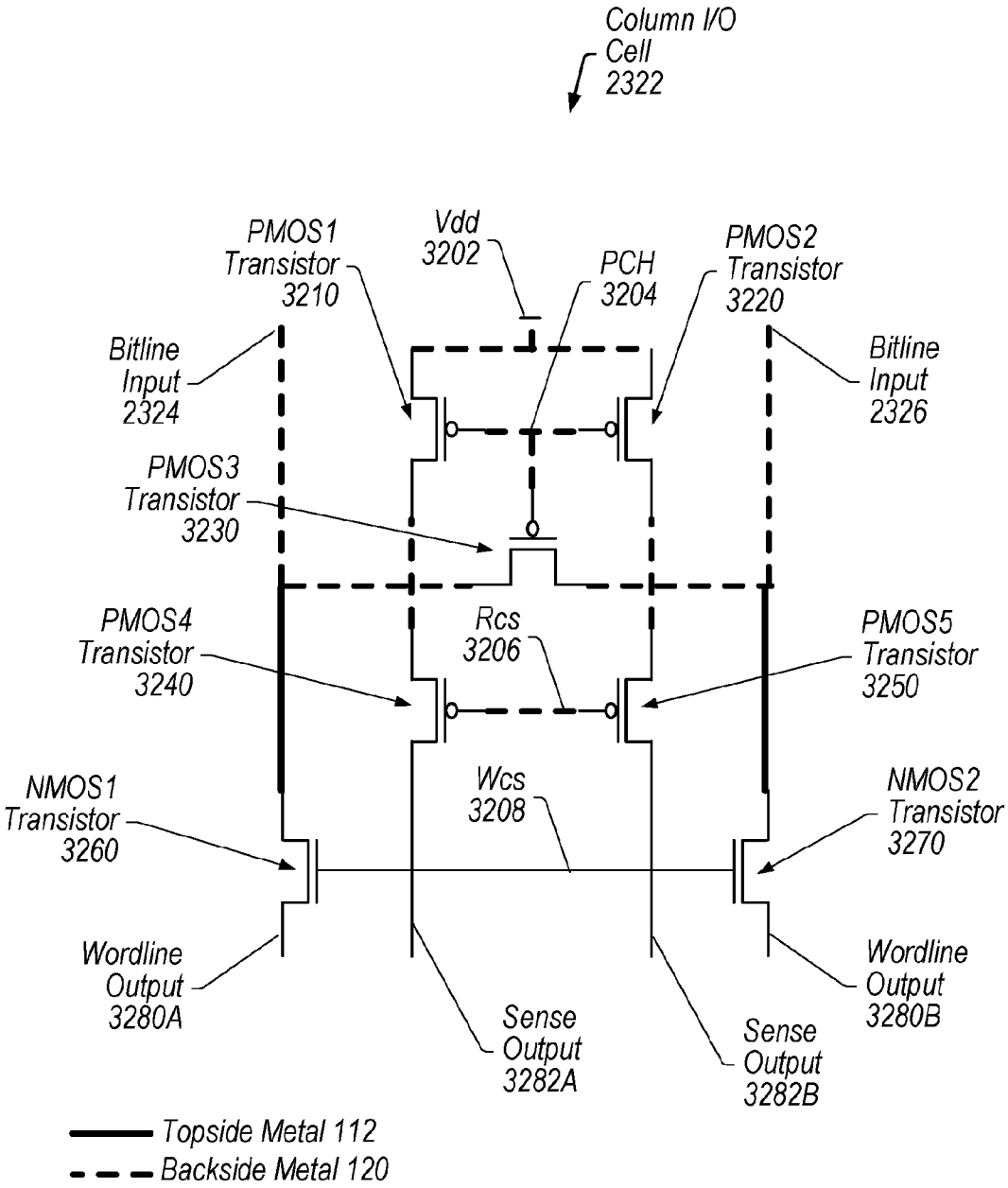

Column I/O Cell 2322
PMOS1 Transistor 3210
Vdd 3202
PCH 3204
PMOS2 Transistor 3220
Bitline Input 2324
Bitline Input 2326
PMOS3 Transistor 3230
PMOS4 Transistor 3240
Rcs 3206
PMOS5 Transistor 3250
NMOS1 Transistor 3260
Wcs 3208
NMOS2 Transistor 3270
Wordline Output 3280A
Sense Output 3282A
Sense Output 3282B
Wordline Output 3280B
Topside Metal 112
Backside Metal 120

FIG. 34

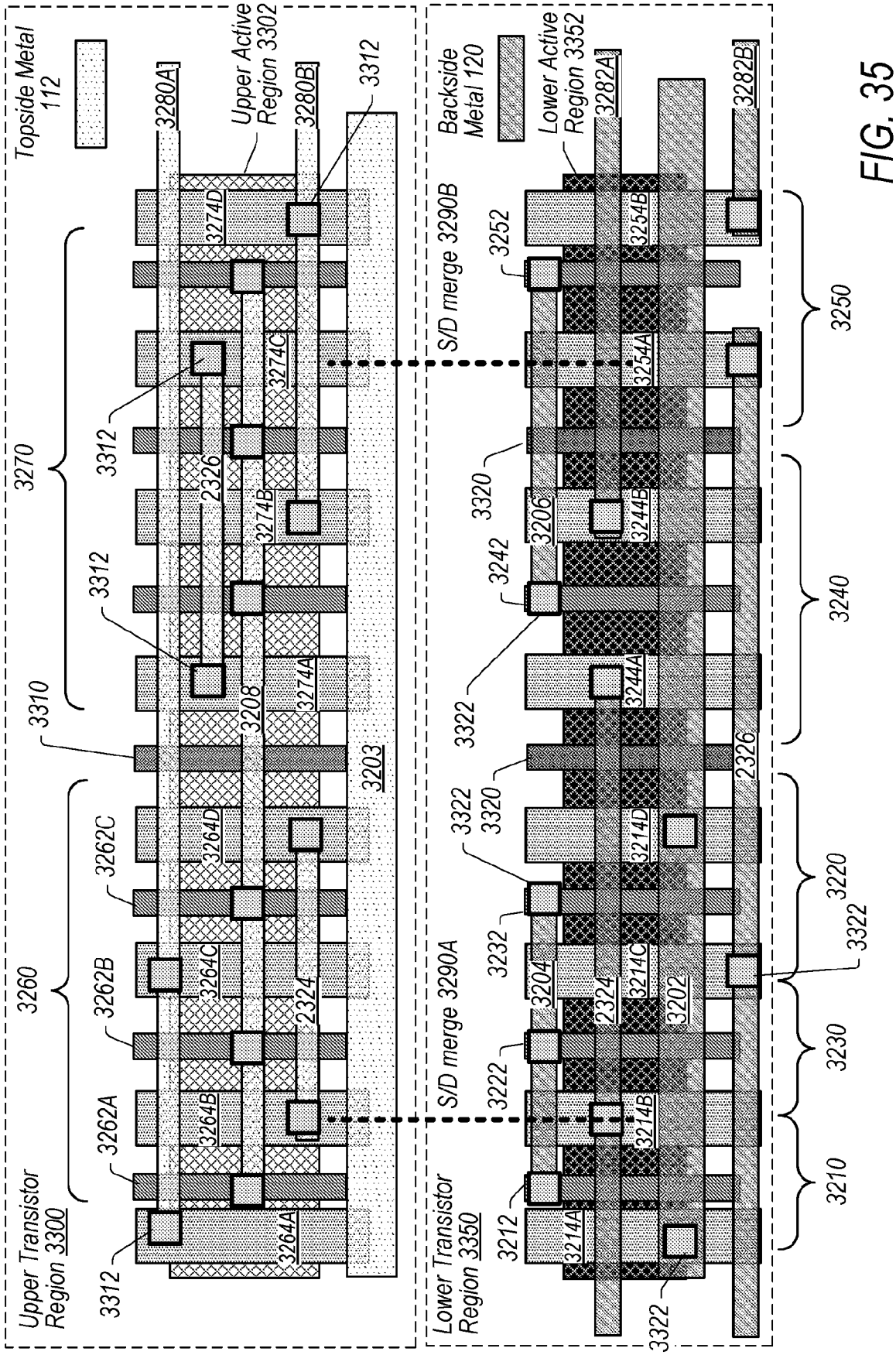

Topside Metal 112
Backside Metal 120
Upper Active Region 3302
Lower Active Region 3352
Upper Transistor Region 3300
Lower Transistor Region 3350
S/D merge 3290B
S/D merge 3290A
3270
3260
3250
3240
3230
3220
3210
3280A
3280B
3282A
3282B
3312
3310
3322
3320
3242
3252
3222
3232
3212
3202
3203
3208
2326
2324
3274A
3274B
3274C
3274D
3264A
3264B
3264C
3264D
3262A
3262B
3262C
3254A
3254B
3244A
3244B
3206
3204
3214A
3214B
3214C
3214D

FIG. 35

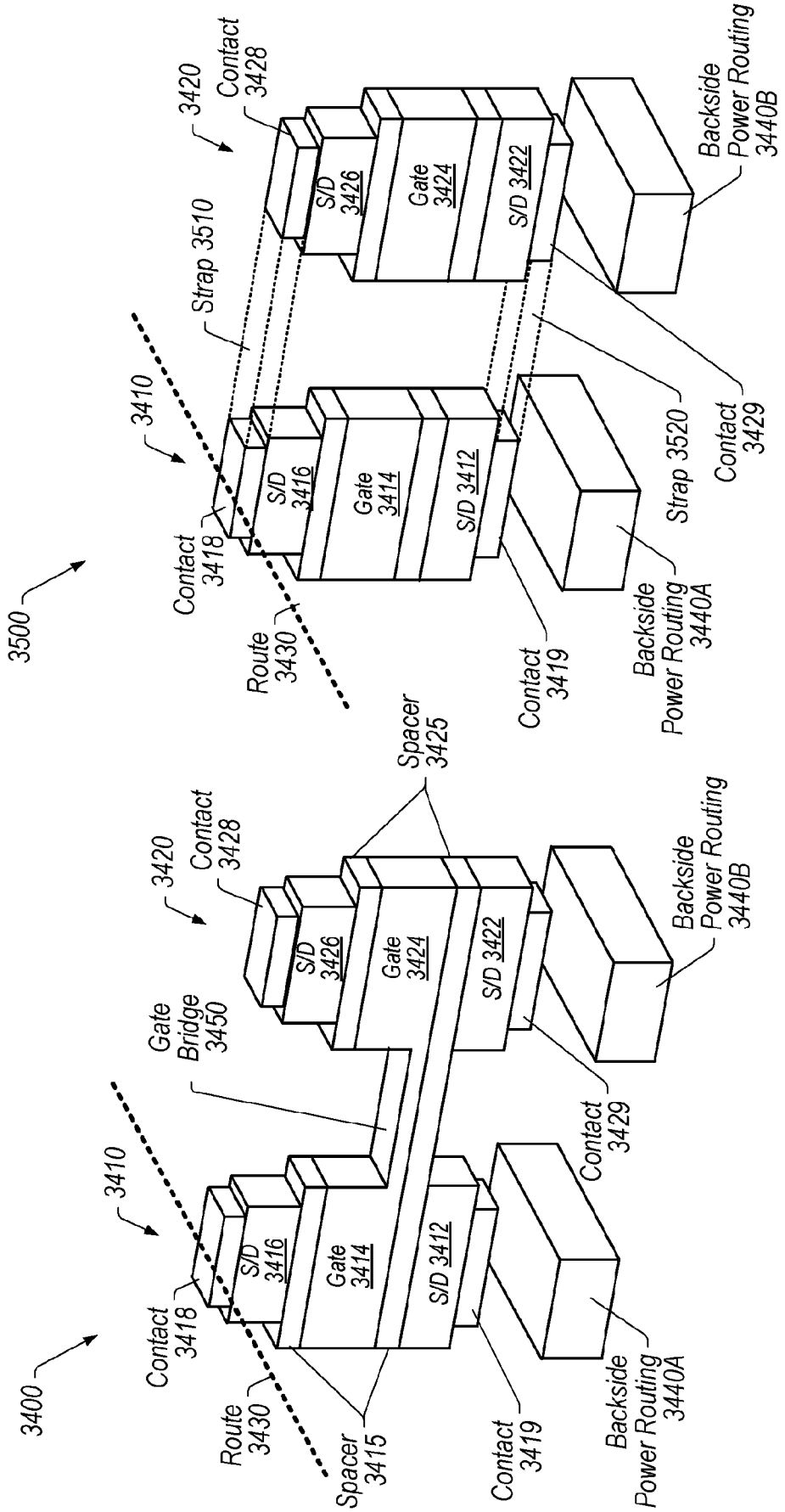

3500
3410
3420
Contact 3428
Strap 3510
S/D 3426
Gate 3424
S/D 3422
Backside Power Routing 3440B
Contact 3418
S/D 3416
Gate 3414
S/D 3412
Strap 3520
Contact 3429
Route 3430
Contact 3419
Backside Power Routing 3440A
Spacer 3425

FIG. 37

3400
3410
3420
Contact 3428
Gate Bridge 3450
S/D 3426
Gate 3424
S/D 3422
Backside Power Routing 3440B
Contact 3418
S/D 3416
Gate 3414
S/D 3412
Contact 3429
Route 3430
Spacer 3415
Contact 3419
Backside Power Routing 3440A

FIG. 36

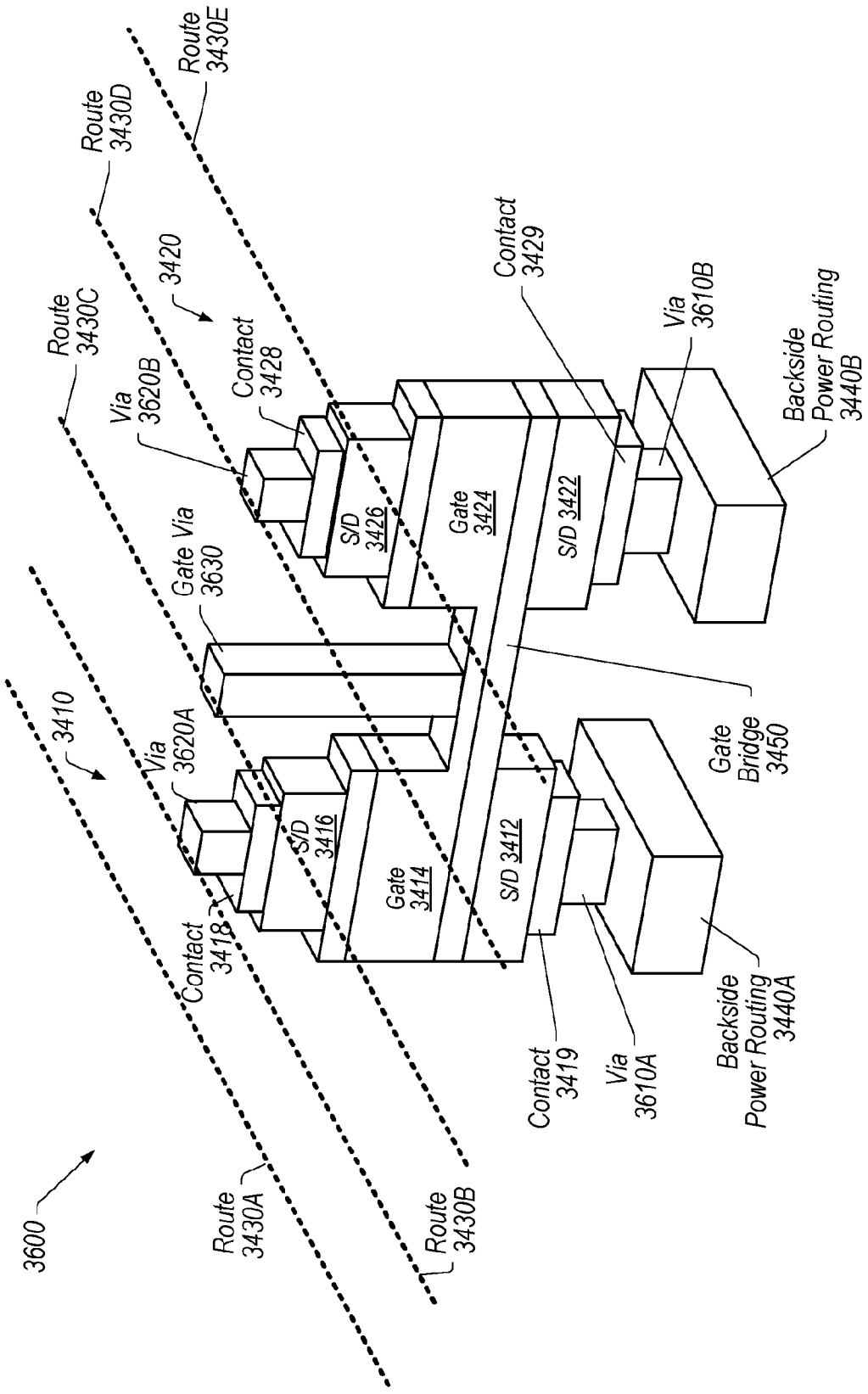

3600
3410
3420
Route 3430A
Route 3430B
Route 3430C
Route 3430D
Route 3430E
Via 3620A
Via 3620B
Gate Via 3630
Contact 3418
Contact 3428
Contact 3429
Contact 3419
S/D 3416
Gate 3414
S/D 3412
S/D 3426
Gate 3424
S/D 3422
Gate Bridge 3450
Via 3610A
Via 3610B
Backside Power Routing 3440A
Backside Power Routing 3440B

FIG. 38

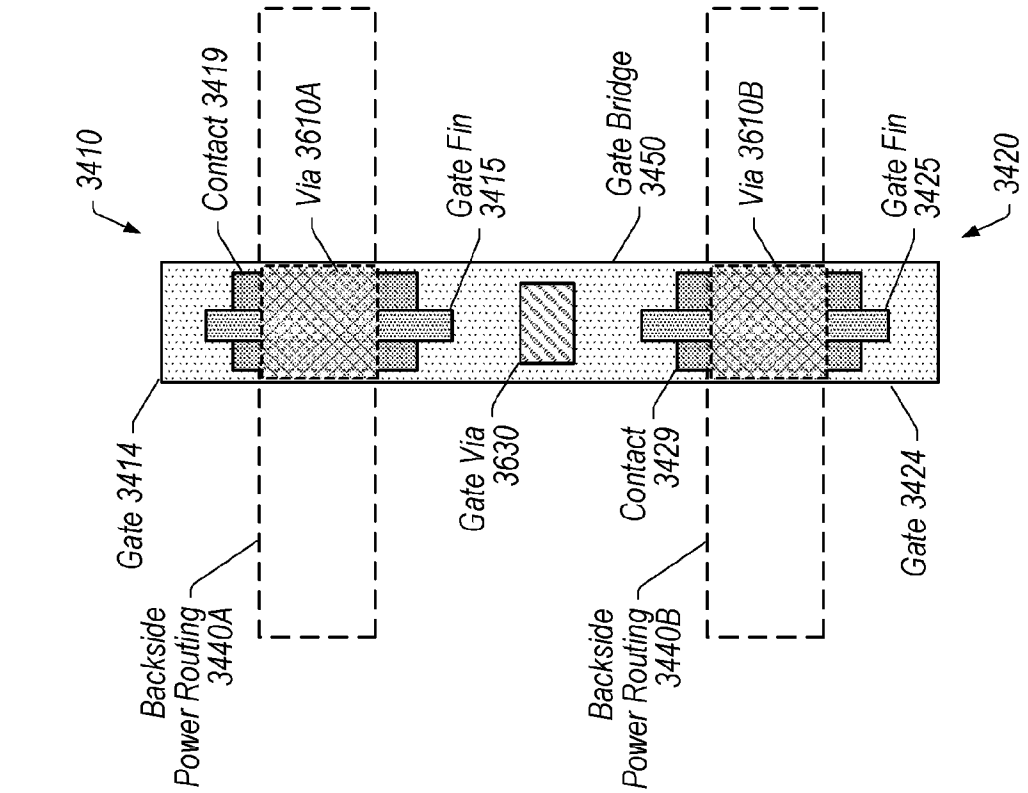

3410
Contact 3419
Via 3610A
Gate Fin 3415
Gate Bridge 3450
Via 3610B
Gate Fin 3425
3420
Gate 3414
Gate Via 3630
Contact 3429
Gate 3424
Backside Power Routing 3440A
Backside Power Routing 3440B

FIG. 40

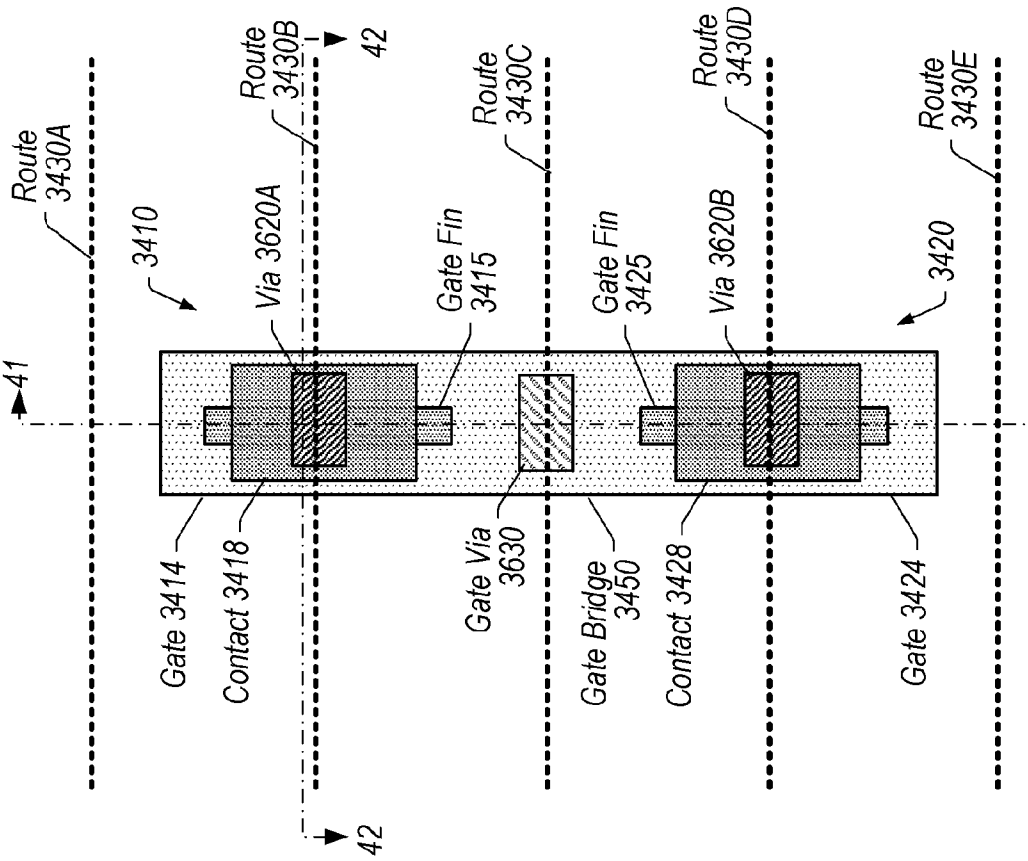

Route 3430A
Route 3430B
42
Route 3430C
Route 3430D
Route 3430E
3410
Via 3620A
Gate Fin 3415
Gate Fin 3425
Via 3620B
3420
41
41
Gate 3414
Contact 3418
Gate Via 3630
Gate Bridge 3450
Contact 3428
Gate 3424
42

FIG. 39

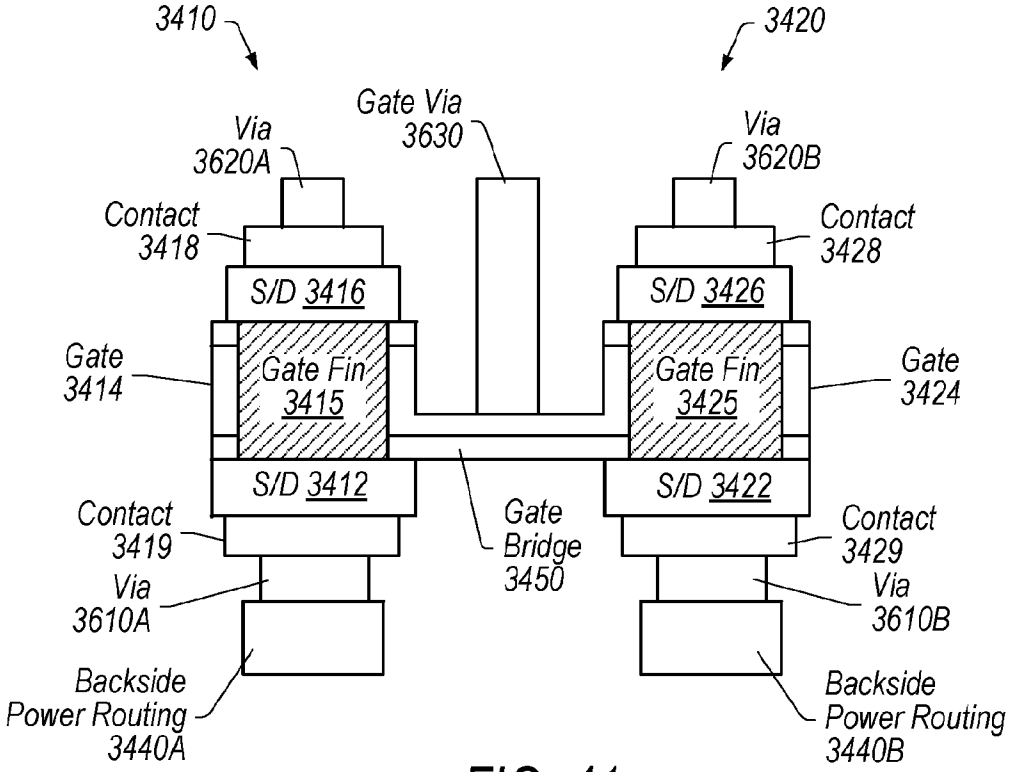

3410
3420
Gate Via
3630
Via
3620A
Via
3620B
Contact
3418
Contact
3428
S/D 3416
S/D 3426
Gate
3414
Gate Fin
3415
Gate Fin
3425
Gate
3424
S/D 3412
S/D 3422
Contact
3419
Gate
Bridge
3450
Contact
3429
Via
3610A
Via
3610B
Backside
Power Routing
3440A
Backside
Power Routing
3440B

FIG. 41

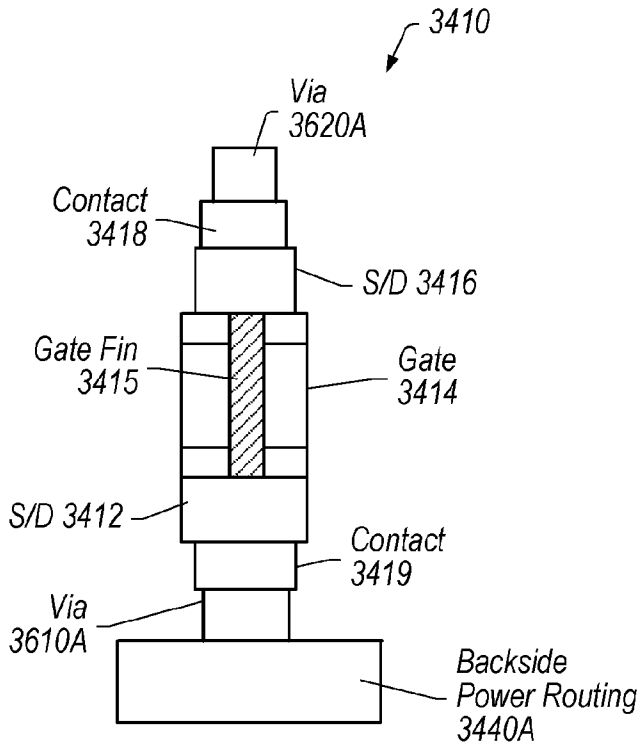

3410
Via
3620A
Contact
3418
S/D 3416
Gate Fin
3415
Gate
3414
S/D 3412
Contact
3419
Via
3610A
Backside
Power Routing
3440A

FIG. 42

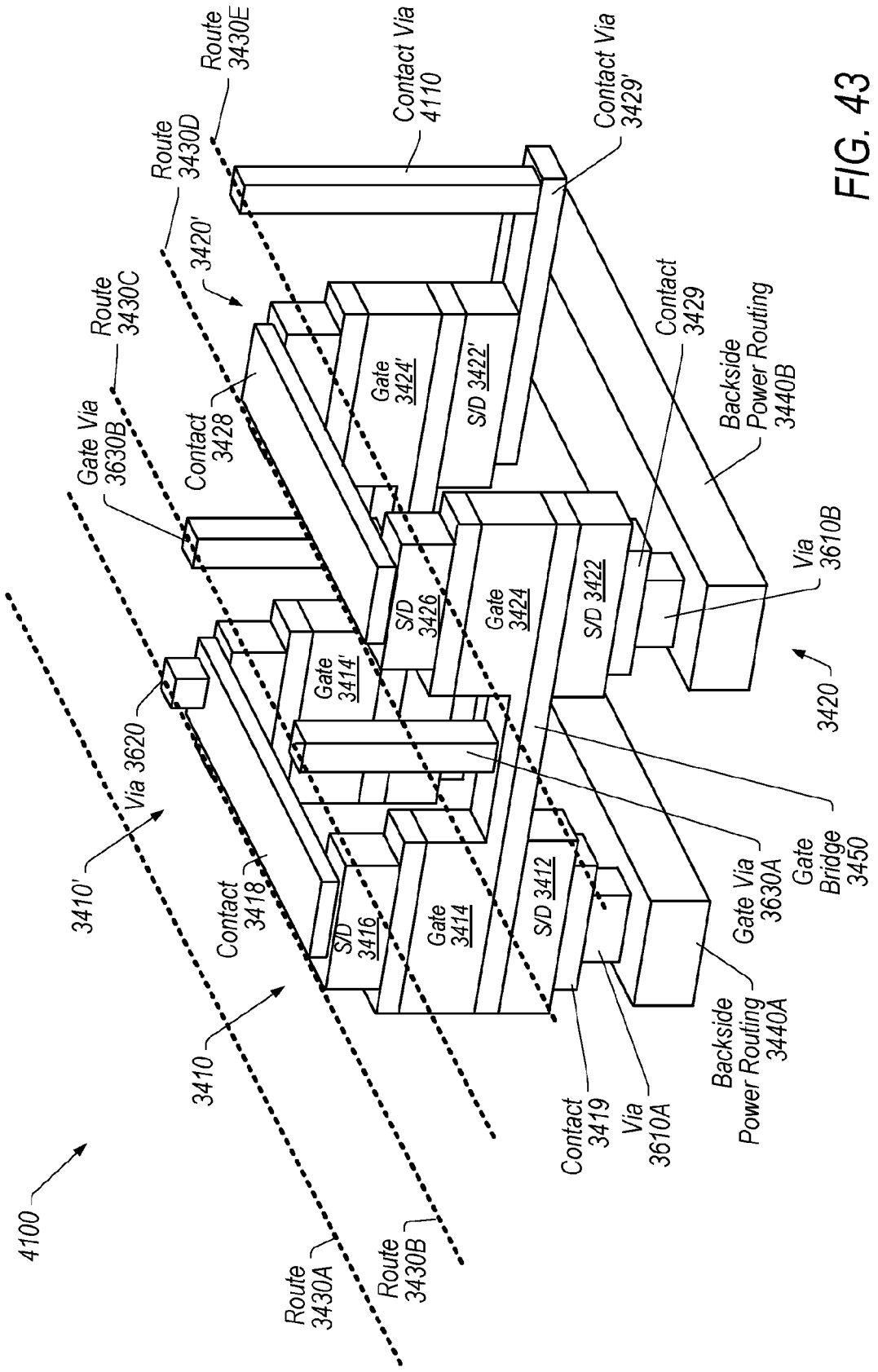

4100
Route 3430A
Route 3430B
3410
3410'
Via 3620
Gate Via 3630B
Route 3430C
Route 3430D
Route 3430E
3420'
Contact 3428
Contact 3418
Contact 3419
Via 3610A
Backside Power Routing 3440A
Gate Via 3630A
Gate Bridge 3450
Contact Via 4110
Contact Via 3429'
Contact 3429
Backside Power Routing 3440B
Via 3610B
3420
Gate 3414'
Gate 3424'
S/D 3422'
S/D 3426
Gate 3424
S/D 3422
S/D 3416
Gate 3414
S/D 3412

FIG. 43

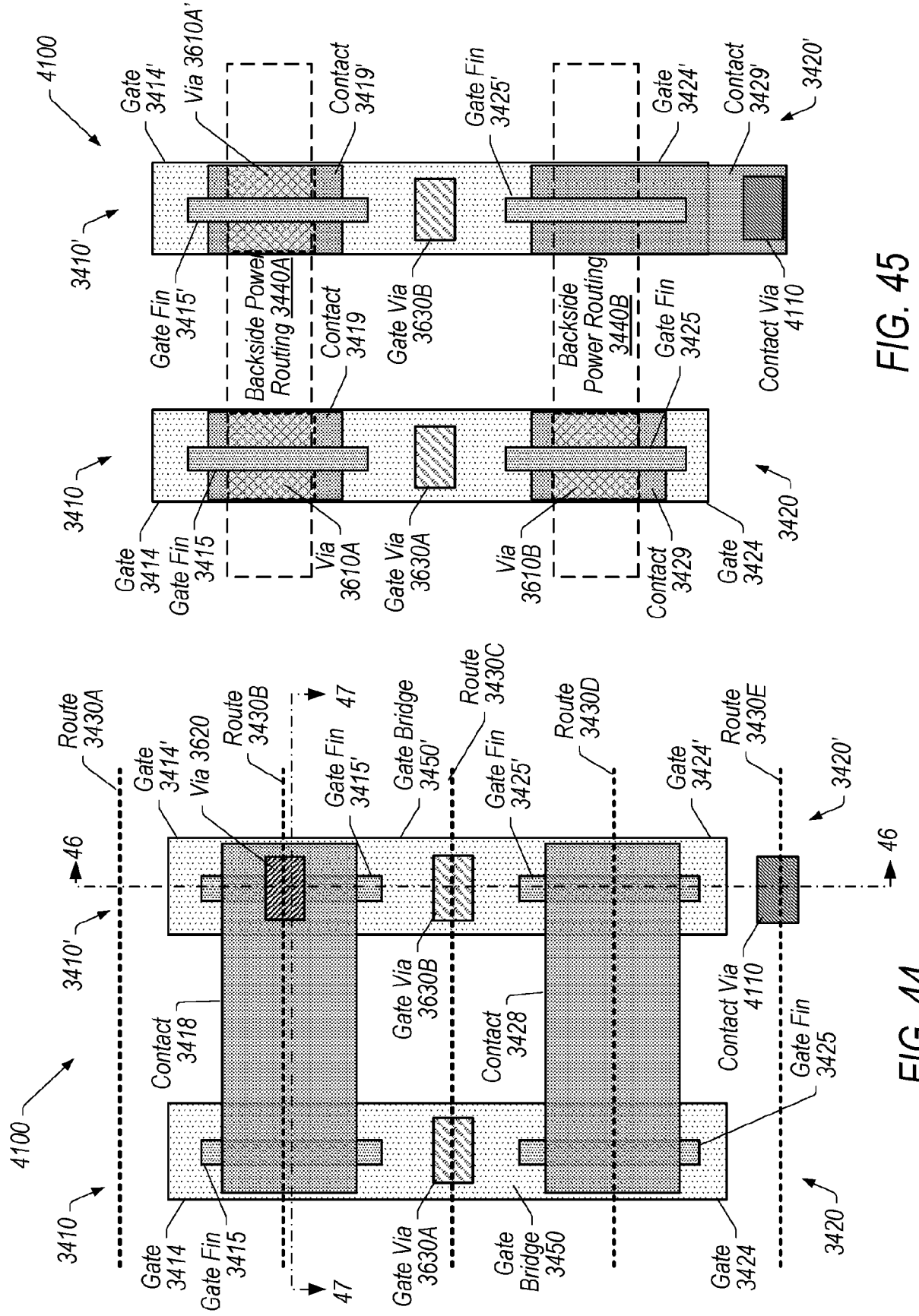

4100
3410
3410'
3420
3420'
Gate 3414
Gate Fin 3415
Via 3610A
Gate Via 3630A
Via 3610B
Contact 3429
Gate 3424
Gate 3414'
Via 3620
Route 3430A
Route 3430B
Gate Fin 3415'
Gate Bridge 3450'
Route 3430C
Gate Fin 3425'
Route 3430D
Gate 3424'
Route 3430E
Contact 3418
Gate Via 3630B
Contact 3428
Contact Via 4110
Gate Fin 3425
Gate Bridge 3450
46
47
Via 3610A'
Contact 3419'
Gate Fin 3425'
Gate 3424'
Contact 3429'
Gate Fin 3415'
Backside Power Routing 3440A
Contact 3419
Gate Via 3630B
Backside Power Routing 3440B
Gate Fin 3425
Contact Via 4110

FIG. 44

FIG. 45

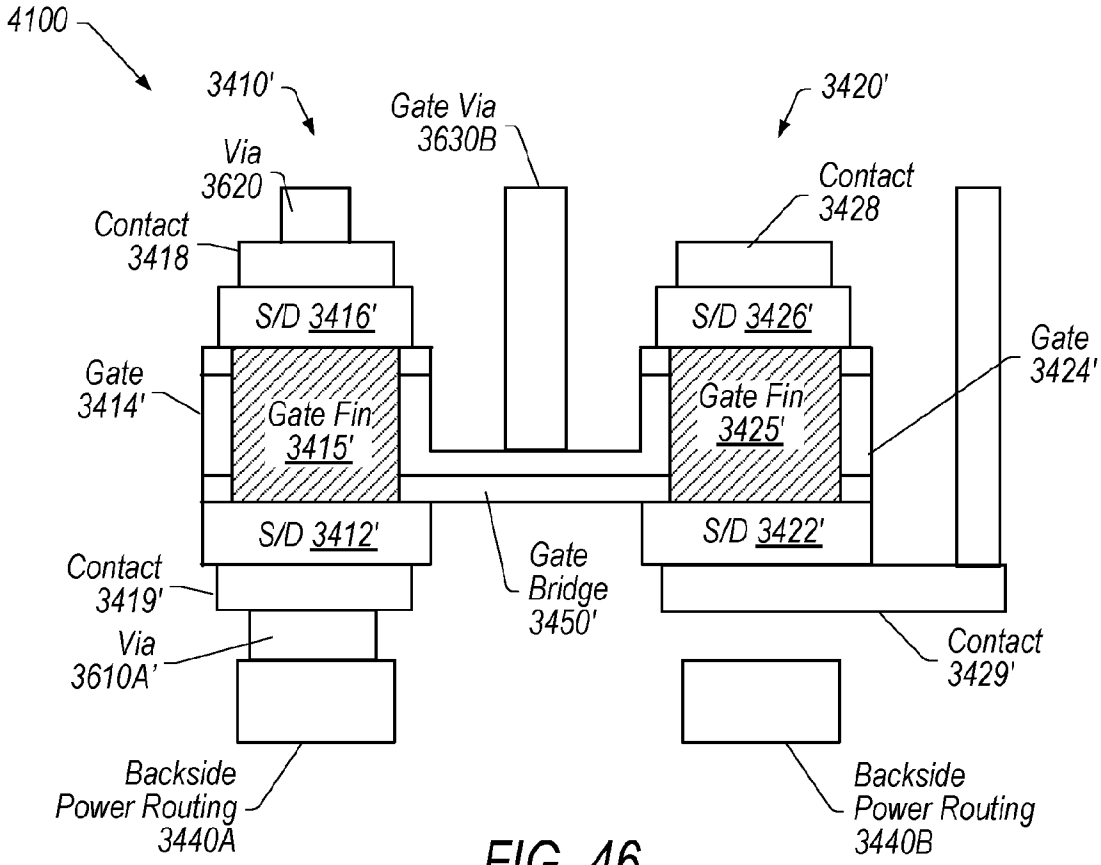

4100
3410'
Gate Via
3630B
3420'
Via
3620
Contact
3428
Contact
3418
S/D 3416'
S/D 3426'
Gate
3424'
Gate
3414'
Gate Fin
3415'
Gate Fin
3425'
S/D 3412'
S/D 3422'
Gate
Bridge
3450'
Contact
3419'
Via
3610A'
Contact
3429'
Backside
Power Routing
3440A
Backside
Power Routing
3440B

FIG. 46

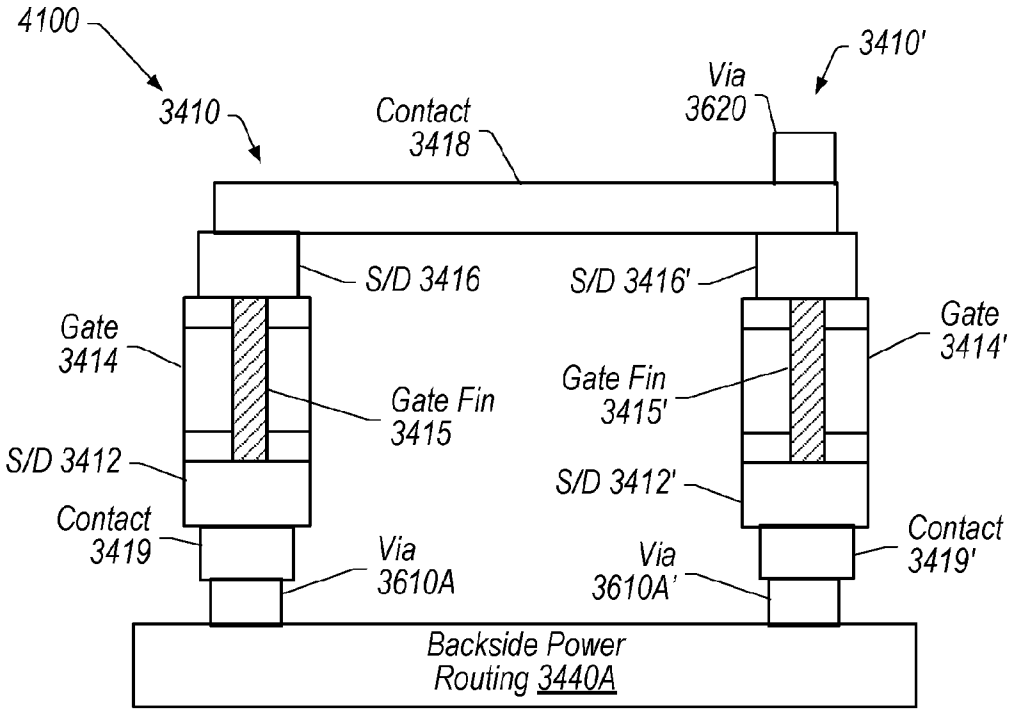

4100
3410
3410'
Contact
3418
Via
3620
S/D 3416
S/D 3416'
Gate
3414
Gate
3414'
Gate Fin
3415
Gate Fin
3415'
S/D 3412
S/D 3412'
Contact
3419
Via
3610A
Via
3610A'
Contact
3419'
Backside Power
Routing 3440A

FIG. 47

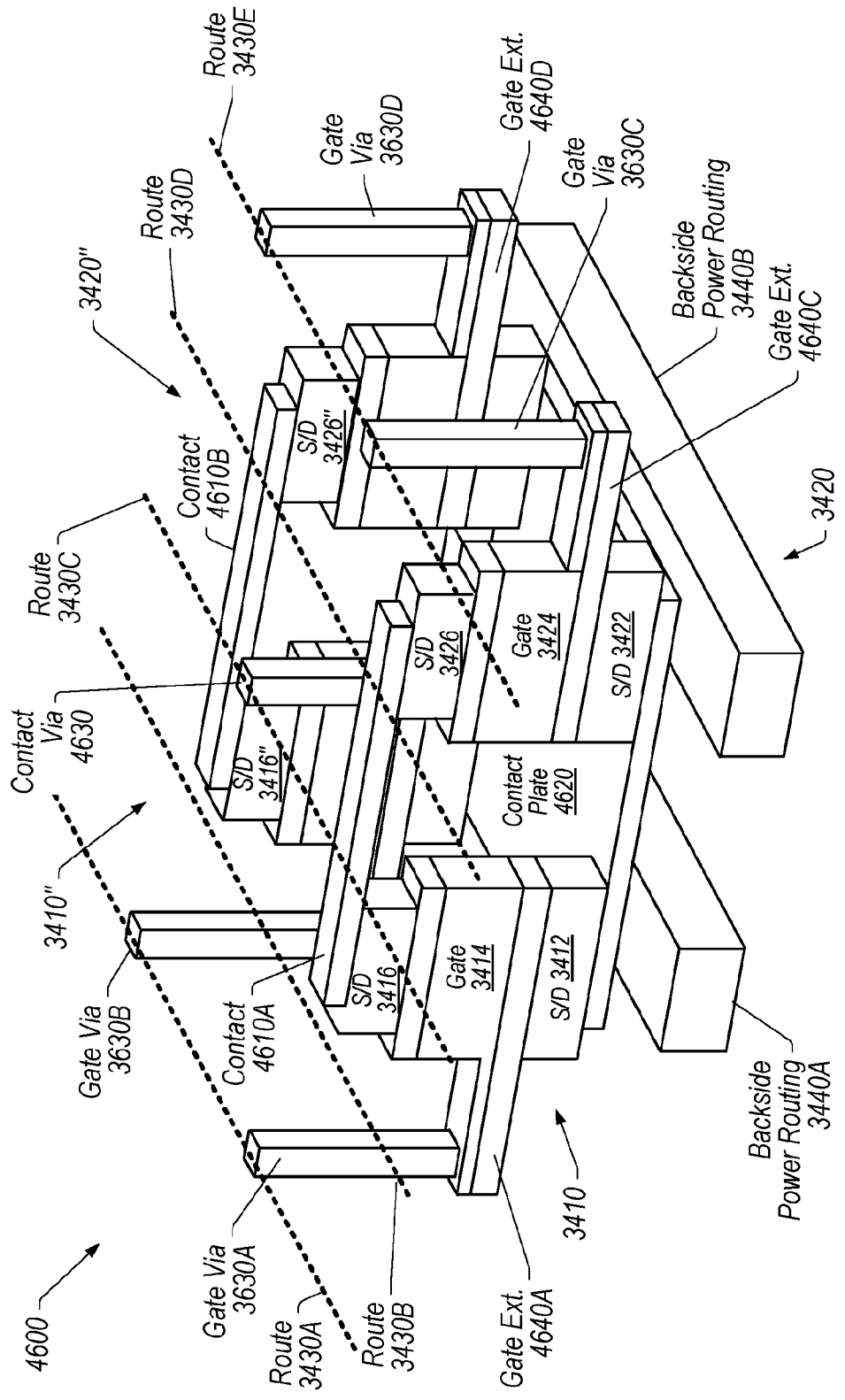

4600
Route 3430A
Route 3430B
Route 3430C
Route 3430D
Route 3430E
Gate Via 3630A
Gate Via 3630B
Gate Via 3630C
Gate Via 3630D
Gate Ext. 4640A
Gate Ext. 4640C
Gate Ext. 4640D
Contact 4610A
Contact 4610B
Contact Via 4630
Backside Power Routing 3440A
Backside Power Routing 3440B
3410
3410"
3420
3420"
S/D 3412
Gate 3414
S/D 3416
S/D 3416"
S/D 3422
Gate 3424
S/D 3426
S/D 3426"
Contact Plate 4620

FIG. 48

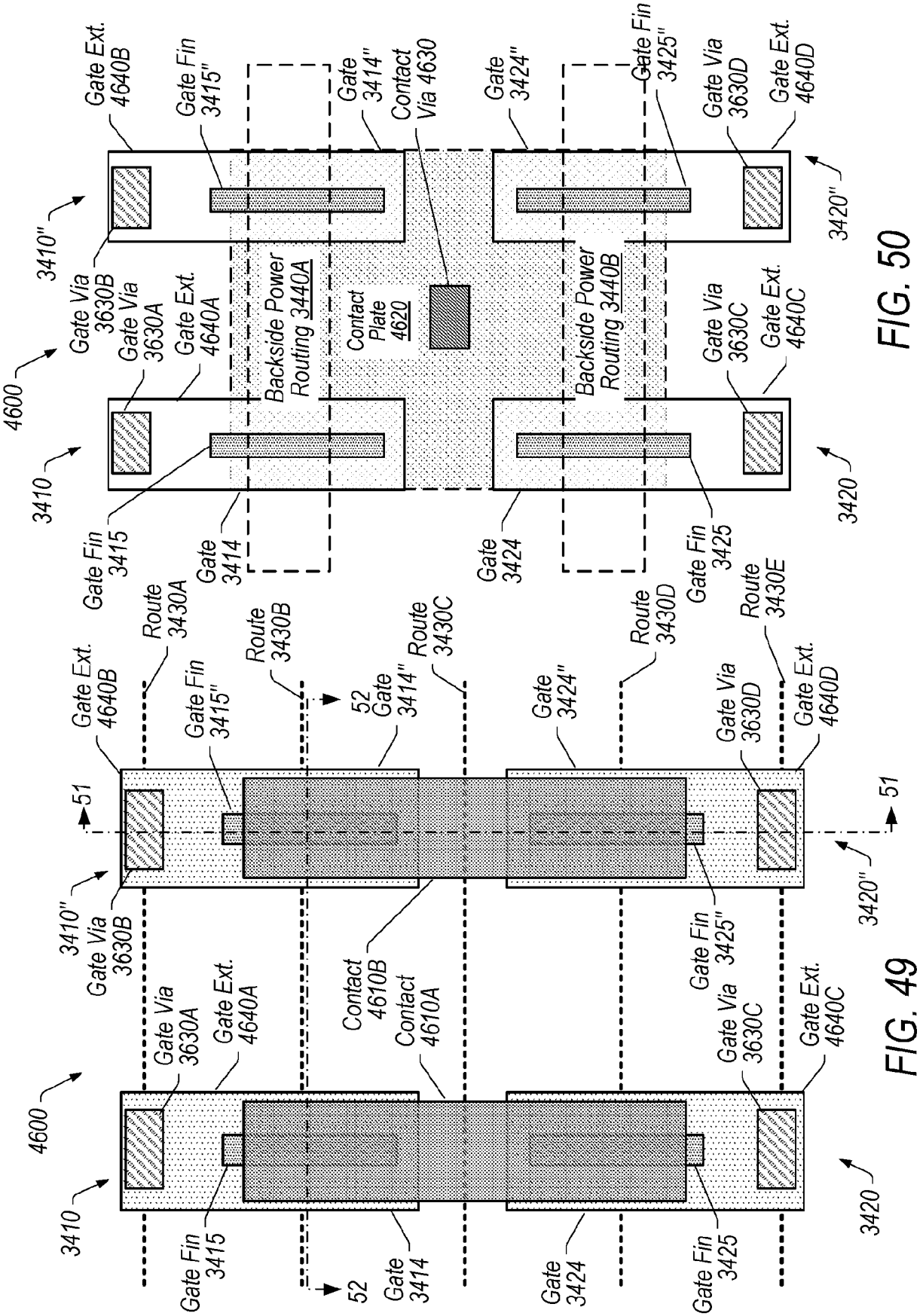

4600
3410
3410"
3420
3420"
Gate Ext. 4640B
Gate Fin 3415"
Gate 3414"
Contact Via 4630
Gate 3424"
Gate Fin 3425"
Gate Via 3630D
Gate Ext. 4640D
Gate Via 3630B
Gate Via 3630A
Gate Ext. 4640A
Backside Power Routing 3440A
Contact Plate 4620
Backside Power Routing 3440B
Gate Via 3630C
Gate Ext. 4640C
Gate Fin 3415
Gate 3414
Gate 3424
Gate Fin 3425
Route 3430A
Route 3430B
Route 3430C
Route 3430D
Route 3430E
51
52
Contact 4610B
Contact 4610A

FIG. 50

FIG. 49

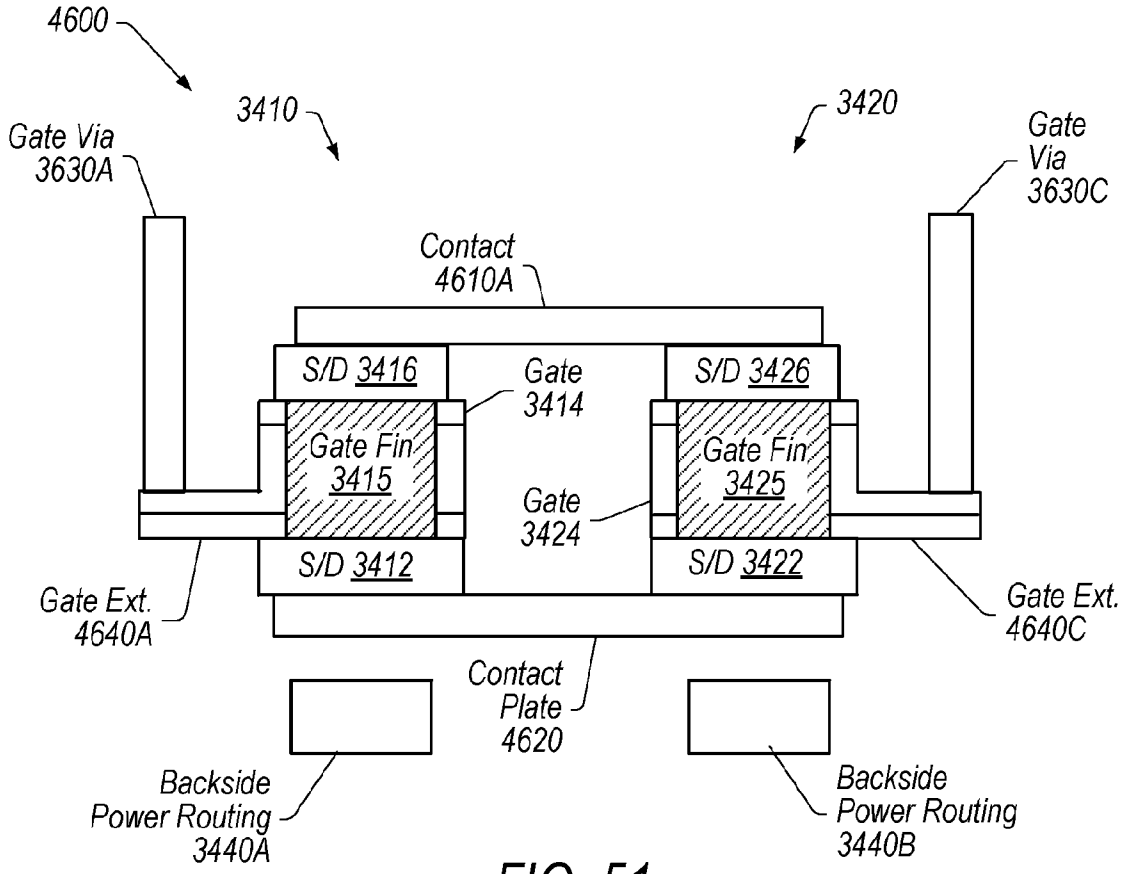

4600
3410
3420
Gate Via 3630A
Gate Via 3630C
Contact 4610A
S/D 3416
Gate 3414
S/D 3426
Gate Fin 3415
Gate Fin 3425
Gate 3424
S/D 3412
S/D 3422
Gate Ext. 4640A
Gate Ext. 4640C
Contact Plate 4620
Backside Power Routing 3440A
Backside Power Routing 3440B

FIG. 51

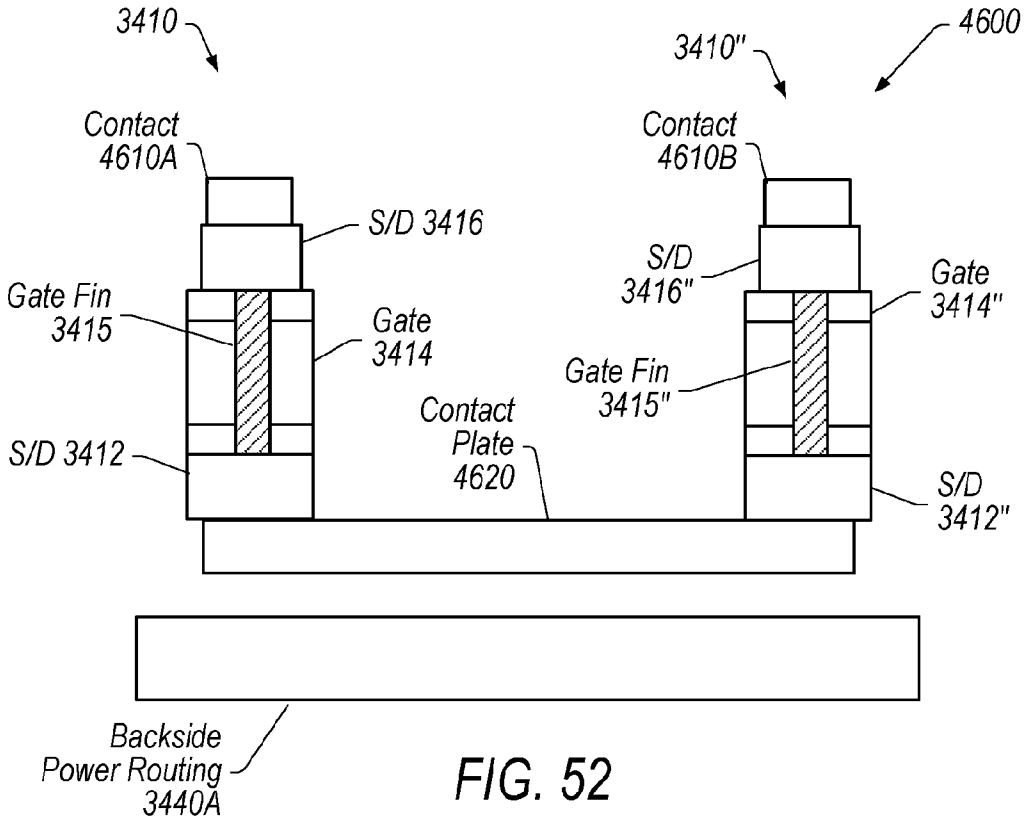

3410
3410"
4600
Contact 4610A
Contact 4610B
S/D 3416
S/D 3416"
Gate Fin 3415
Gate 3414
Gate 3414"
Gate Fin 3415"
Contact Plate 4620
S/D 3412
S/D 3412"
Backside Power Routing 3440A

FIG. 52

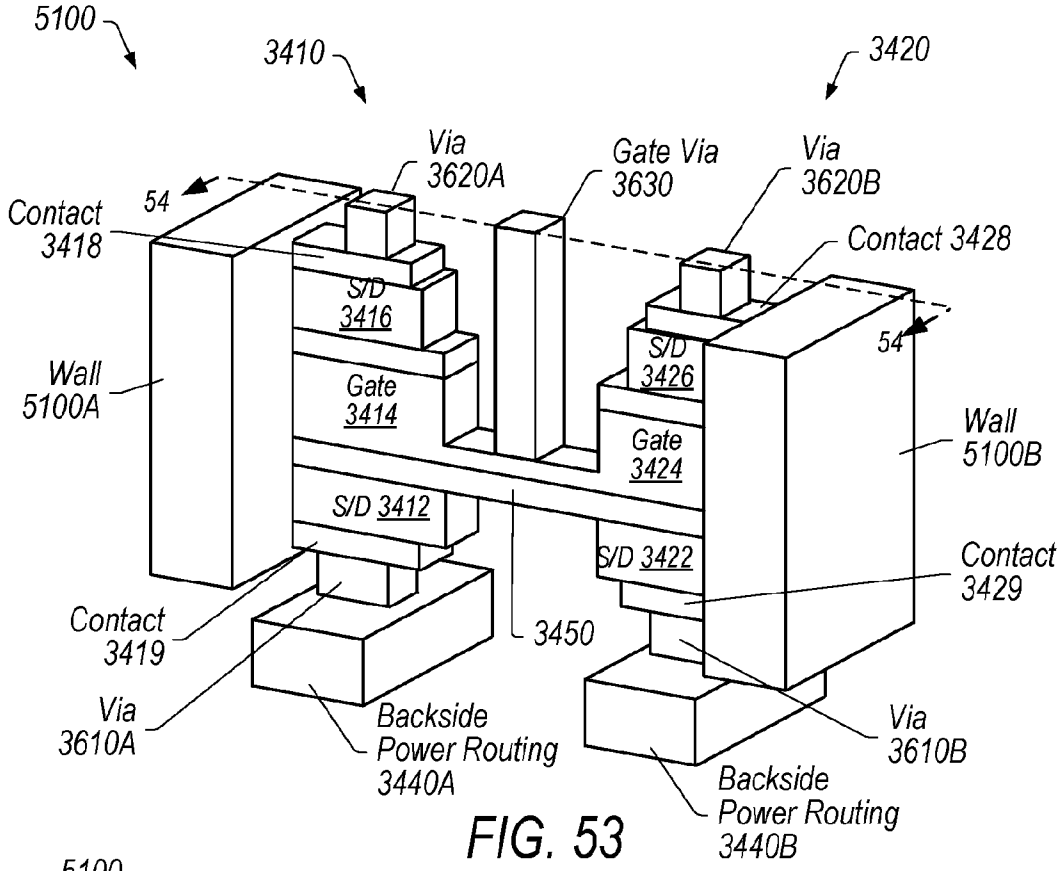

5100
3410
3420
Via 3620A
Gate Via 3630
Via 3620B
Contact 3418
54
Contact 3428
S/D 3416
S/D 3426
54
Wall 5100A
Gate 3414
Gate 3424
Wall 5100B
S/D 3412
S/D 3422
Contact 3429
Contact 3419
3450
Via 3610A
Backside Power Routing 3440A
Via 3610B
Backside Power Routing 3440B

FIG. 53

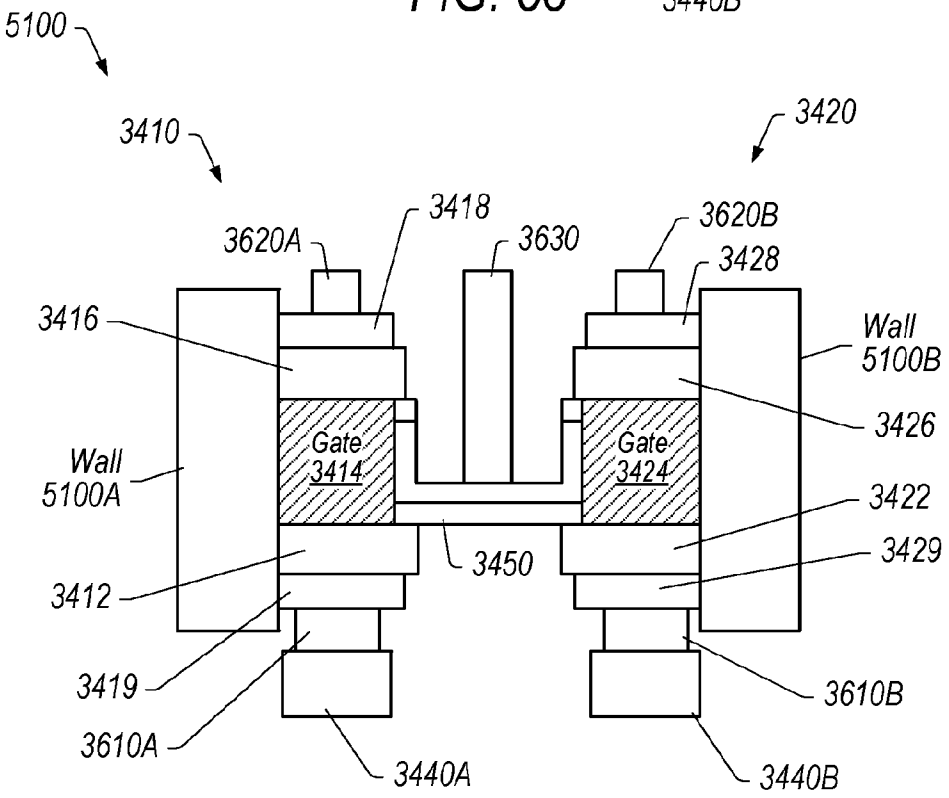

5100
3410
3420
3418
3620A
3630
3620B
3428
3416
Wall 5100B
3426
Gate 3414
Gate 3424
Wall 5100A
3422
3450
3429
3412
3419
3610B
3610A
3440A
3440B

FIG. 54

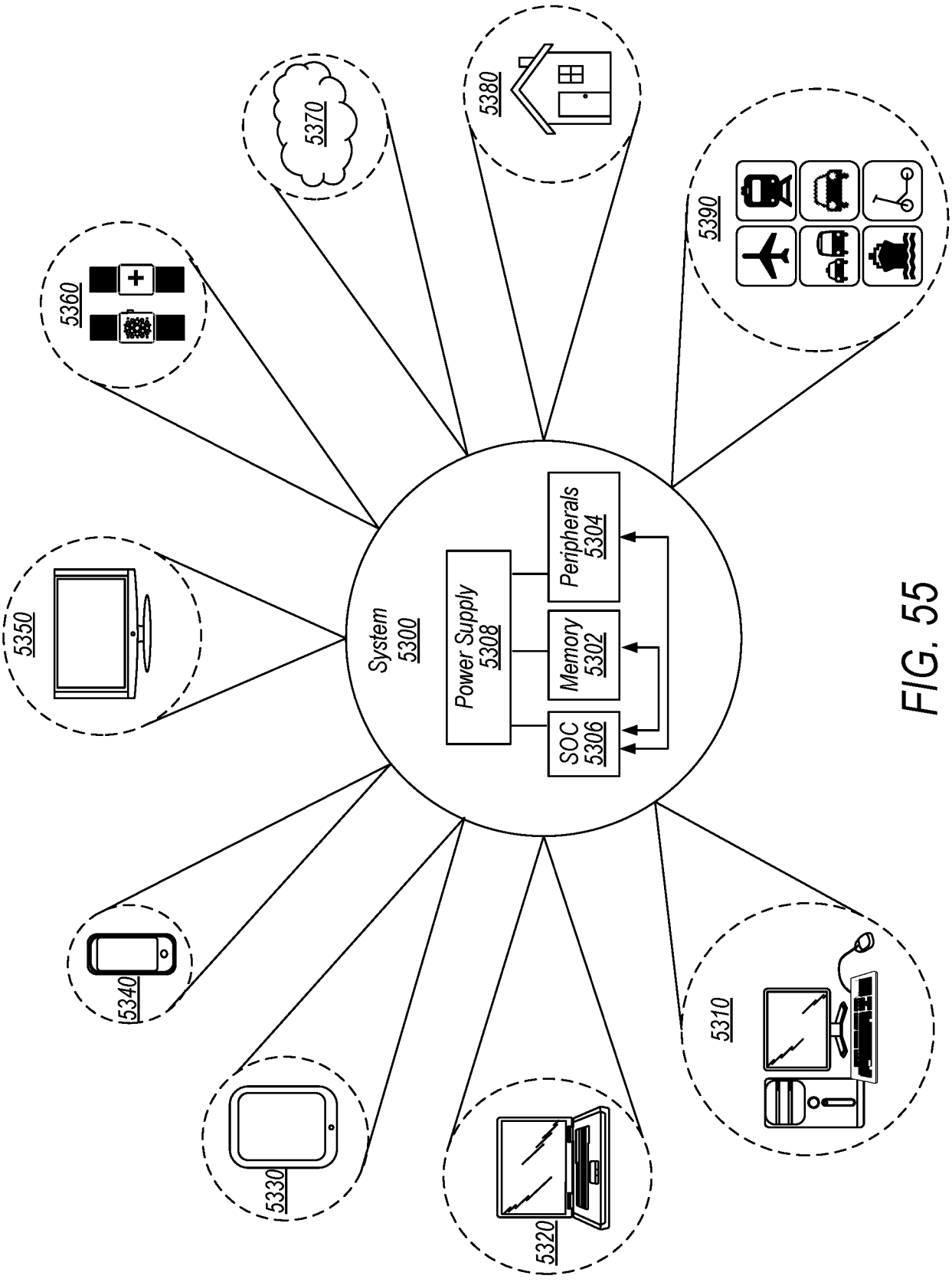

System
5300
Power Supply
5308
SOC
5306
Memory
5302
Peripherals
5304
5310
5320
5330
5340
5350
5360
5370
5380
5390

FIG. 55