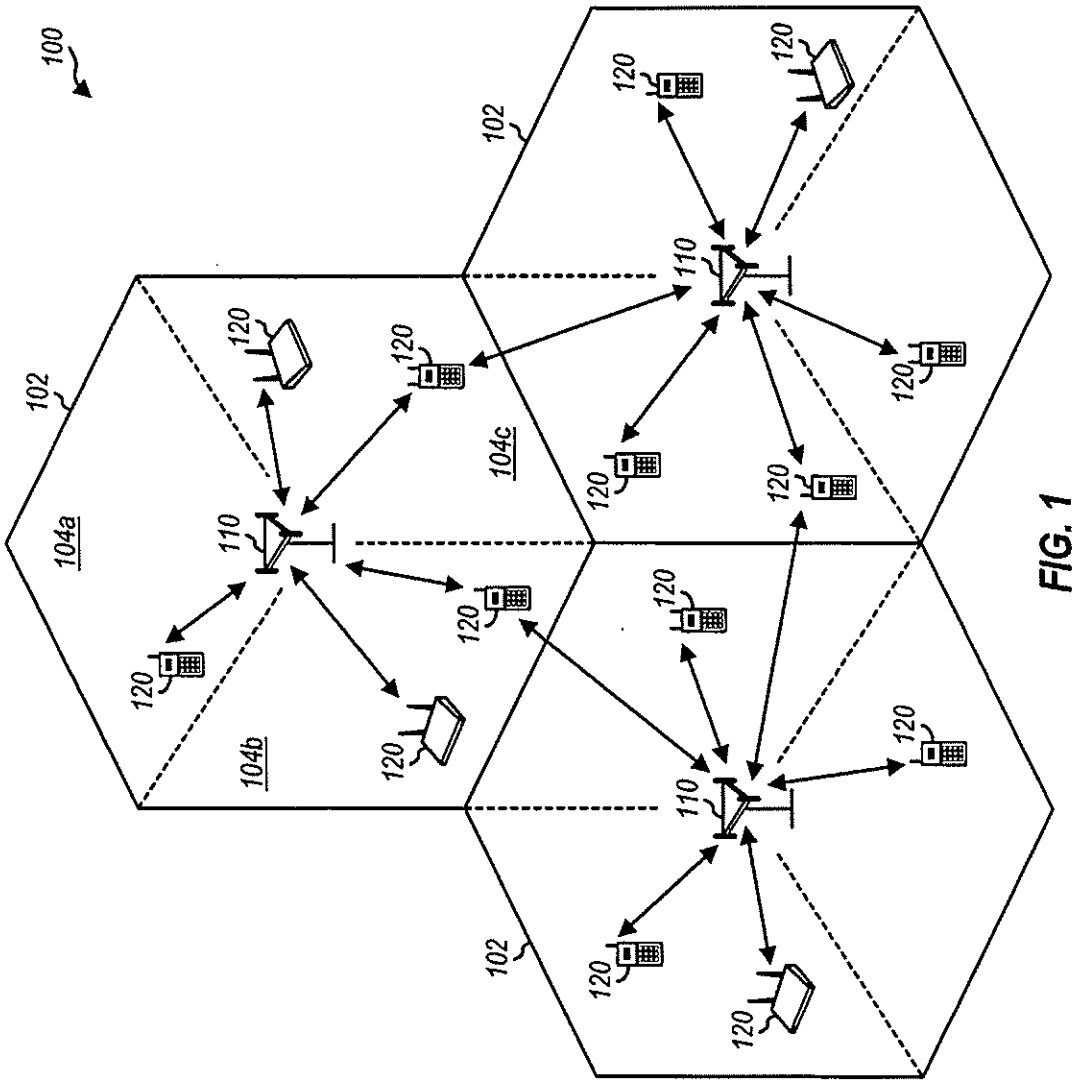

FIG. 1

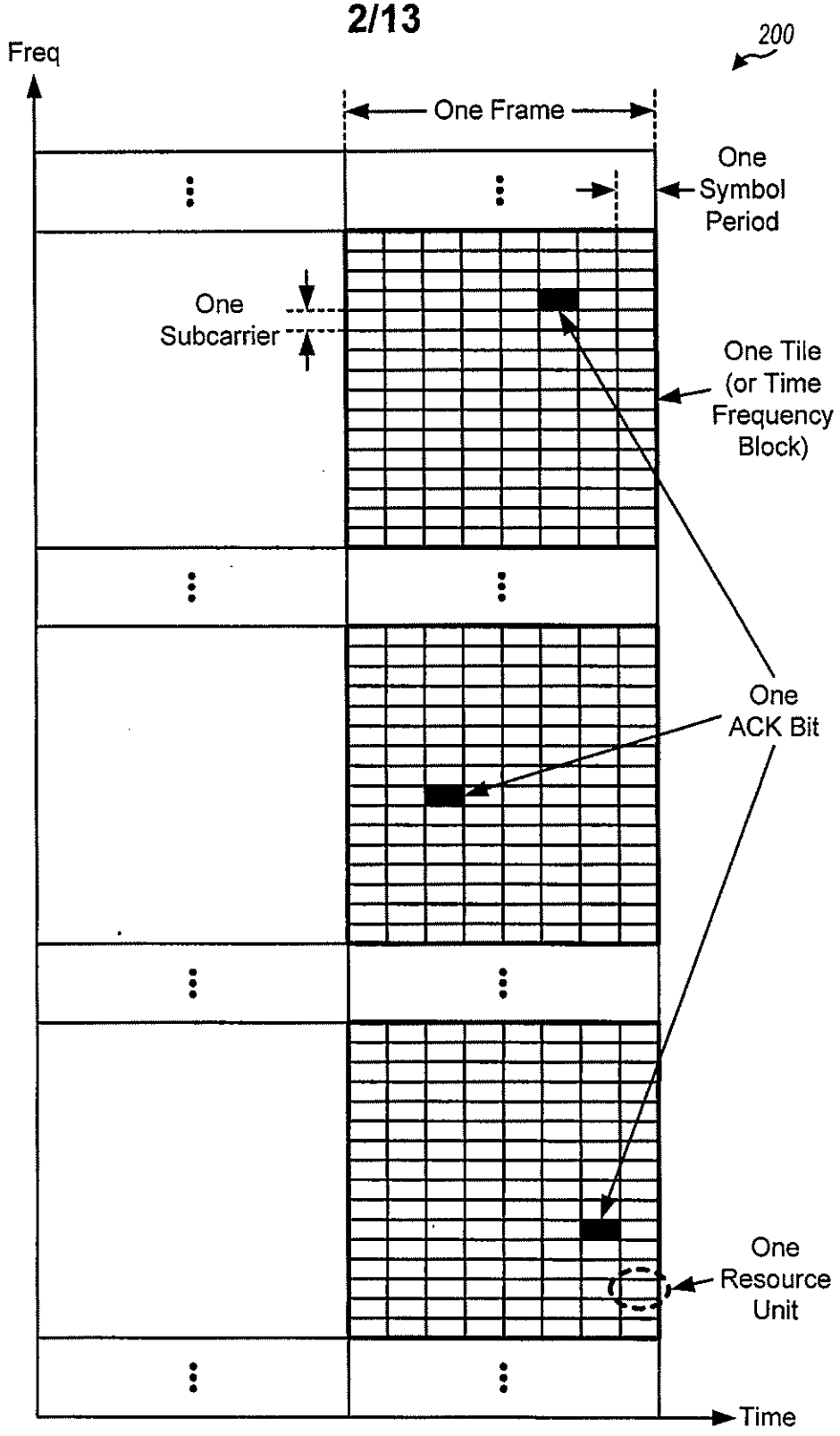
200
Freq
One Frame
One Symbol Period
One Subcarrier
One Tile (or Time Frequency Block)
One ACK Bit
One Resource Unit
Time

FIG. 2

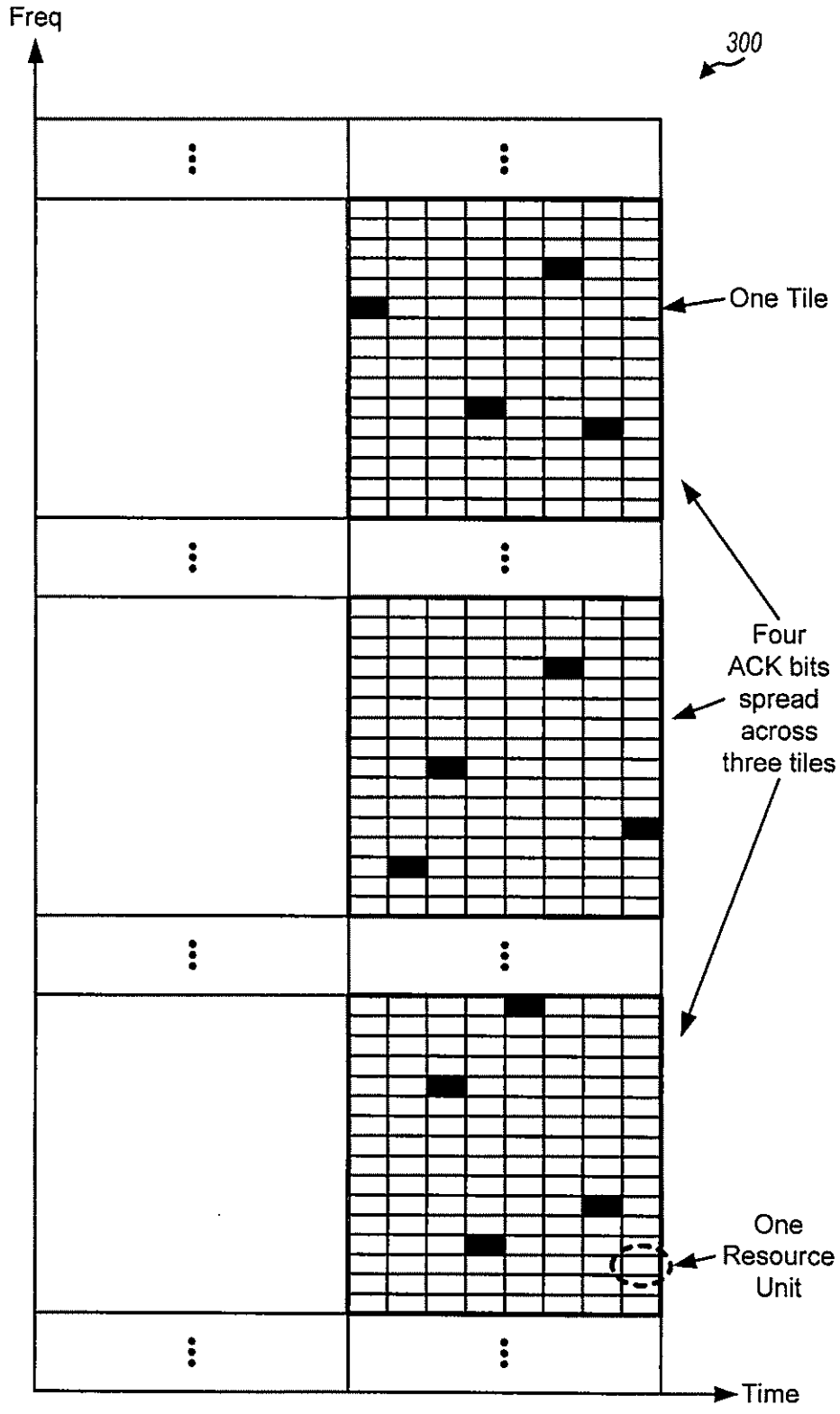
Freq
300
One Tile
Four ACK bits spread across three tiles
One Resource Unit
Time

FIG. 3

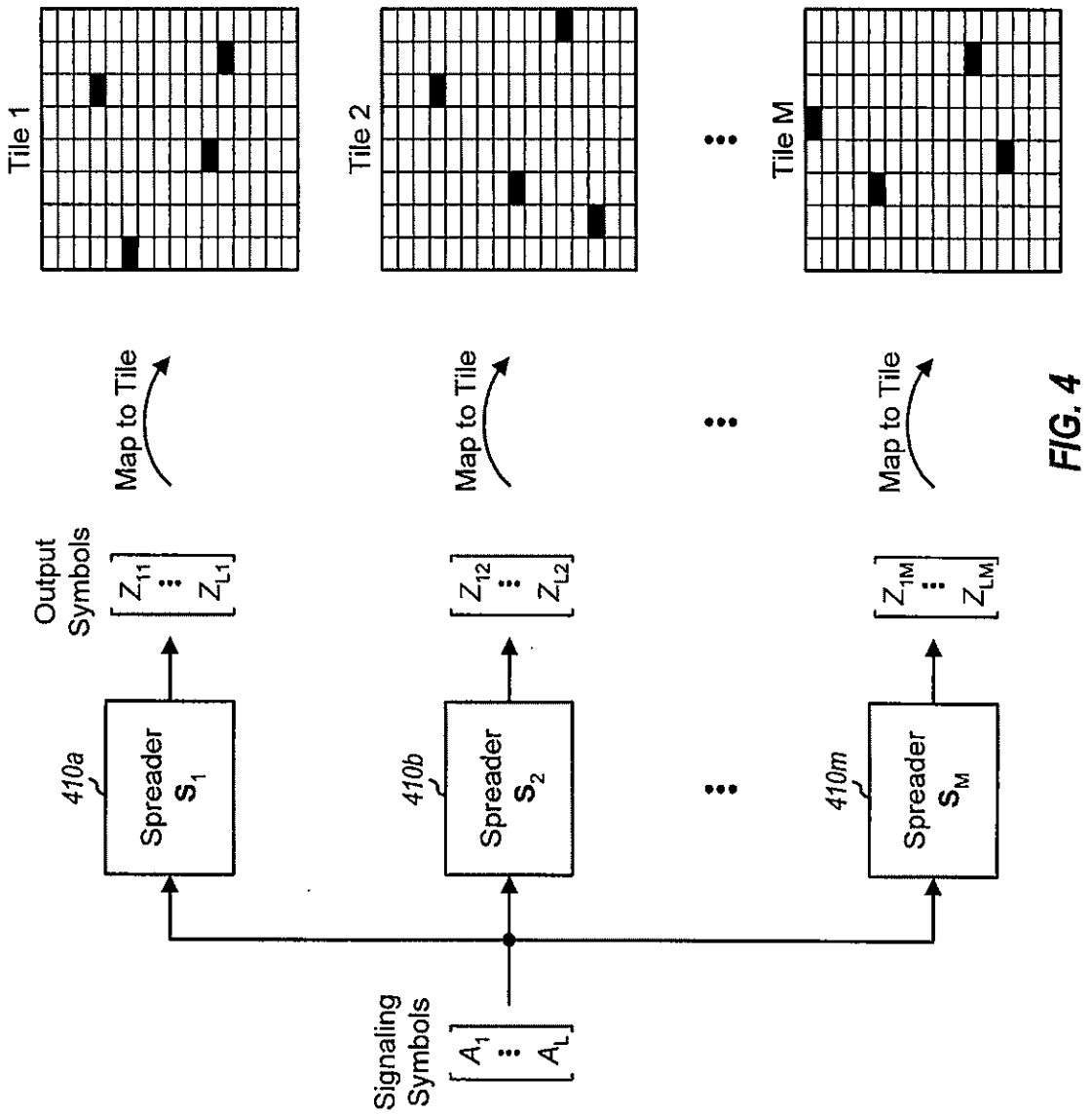
Tile 1
Tile 2
Tile M
Map to Tile
Map to Tile
Map to Tile
Output Symbols
$\begin{bmatrix} Z_{11} \\ \vdots \\ Z_{L1} \end{bmatrix}$
$\begin{bmatrix} Z_{12} \\ \vdots \\ Z_{L2} \end{bmatrix}$
$\begin{bmatrix} Z_{1M} \\ \vdots \\ Z_{LM} \end{bmatrix}$
410a
Spreader s_1
410b
Spreader s_2
410m
Spreader s_M
Signaling Symbols
$\begin{bmatrix} A_1 \\ \vdots \\ A_L \end{bmatrix}$

FIG. 4

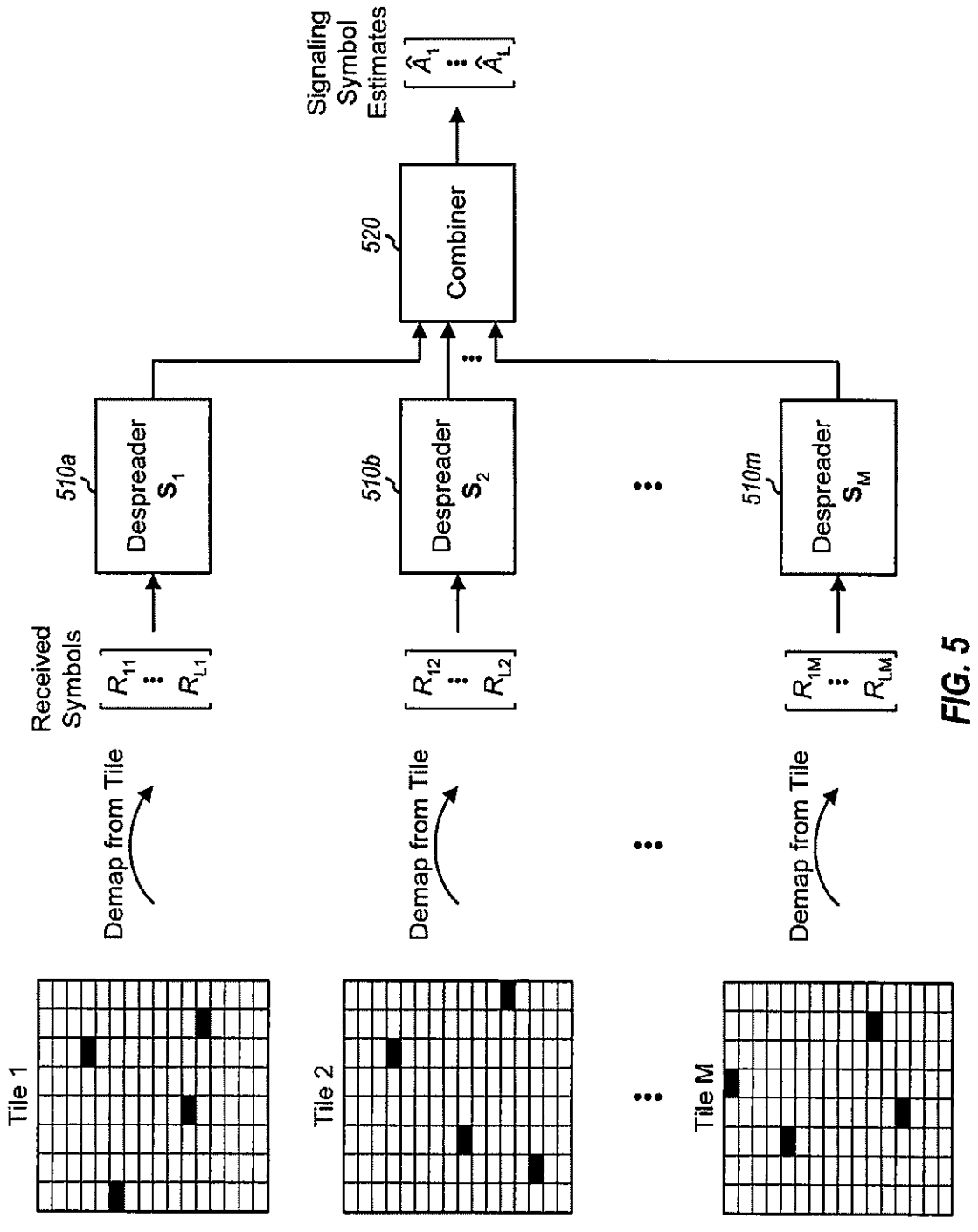
Signaling Symbol Estimates
$\begin{bmatrix}\hat{A}_1 \\ \vdots \\ \hat{A}_L\end{bmatrix}$
520
Combiner
510a
Despreader s_1
510b
Despreader s_2
510m
Despreader s_M
Received Symbols
$\begin{bmatrix}R_{11} \\ \vdots \\ R_{L1}\end{bmatrix}$
$\begin{bmatrix}R_{12} \\ \vdots \\ R_{L2}\end{bmatrix}$
$\begin{bmatrix}R_{1M} \\ \vdots \\ R_{LM}\end{bmatrix}$
Demap from Tile
Demap from Tile
Demap from Tile
Tile 1
Tile 2
Tile M

FIG. 5

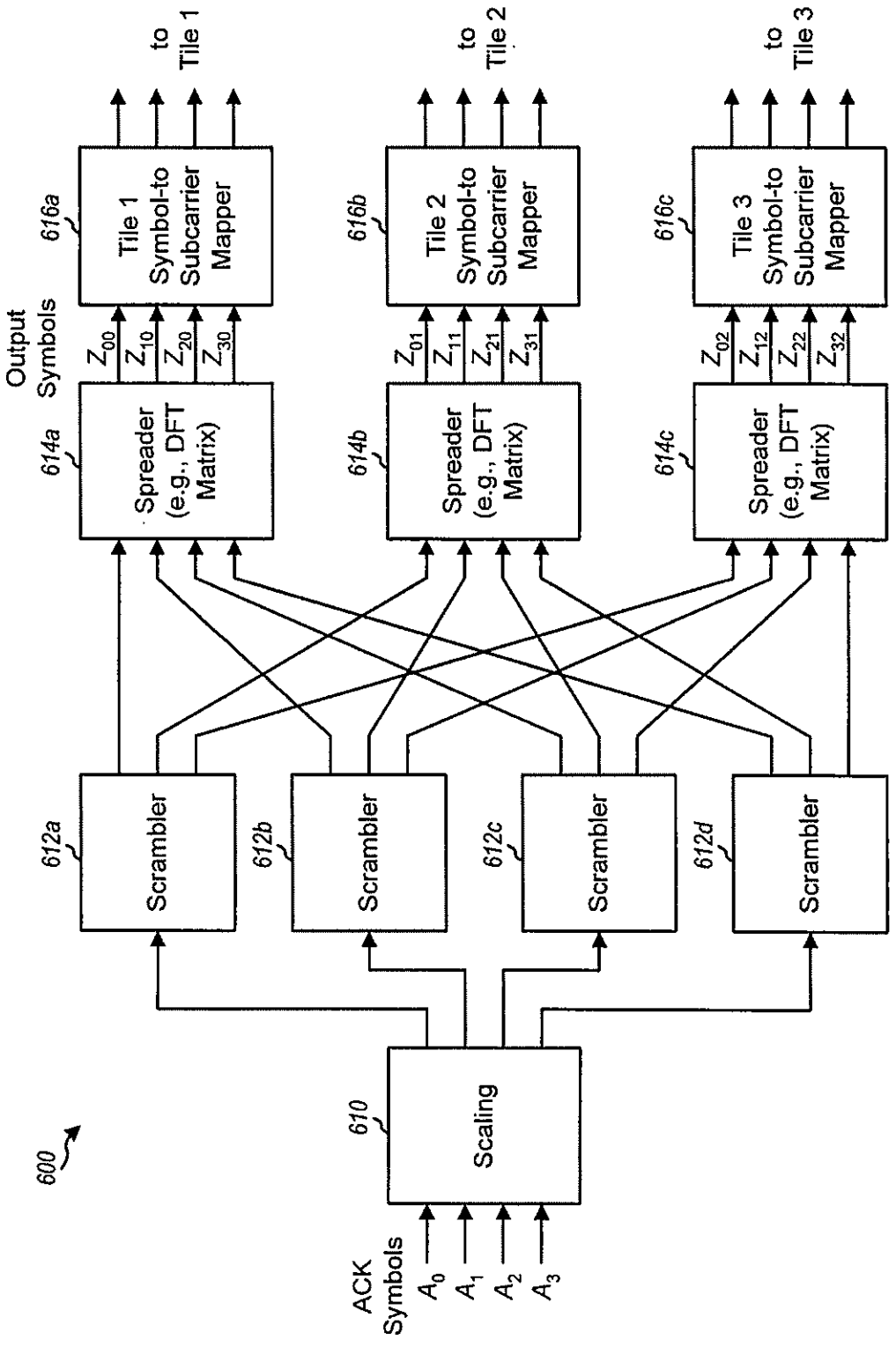
600
610
Scaling
ACK Symbols
A_0
A_1
A_2
A_3
612a
612b
612c
612d
Scrambler
614a
614b
614c
Spreader (e.g., DFT Matrix)
Output Symbols
Z_{00} Z_{10} Z_{20} Z_{30}
Z_{01} Z_{11} Z_{21} Z_{31}
Z_{02} Z_{12} Z_{22} Z_{32}
616a
616b
616c
Tile 1 Symbol-to Subcarrier Mapper
Tile 2 Symbol-to Subcarrier Mapper
Tile 3 Symbol-to Subcarrier Mapper
to Tile 1
to Tile 2
to Tile 3

FIG. 6

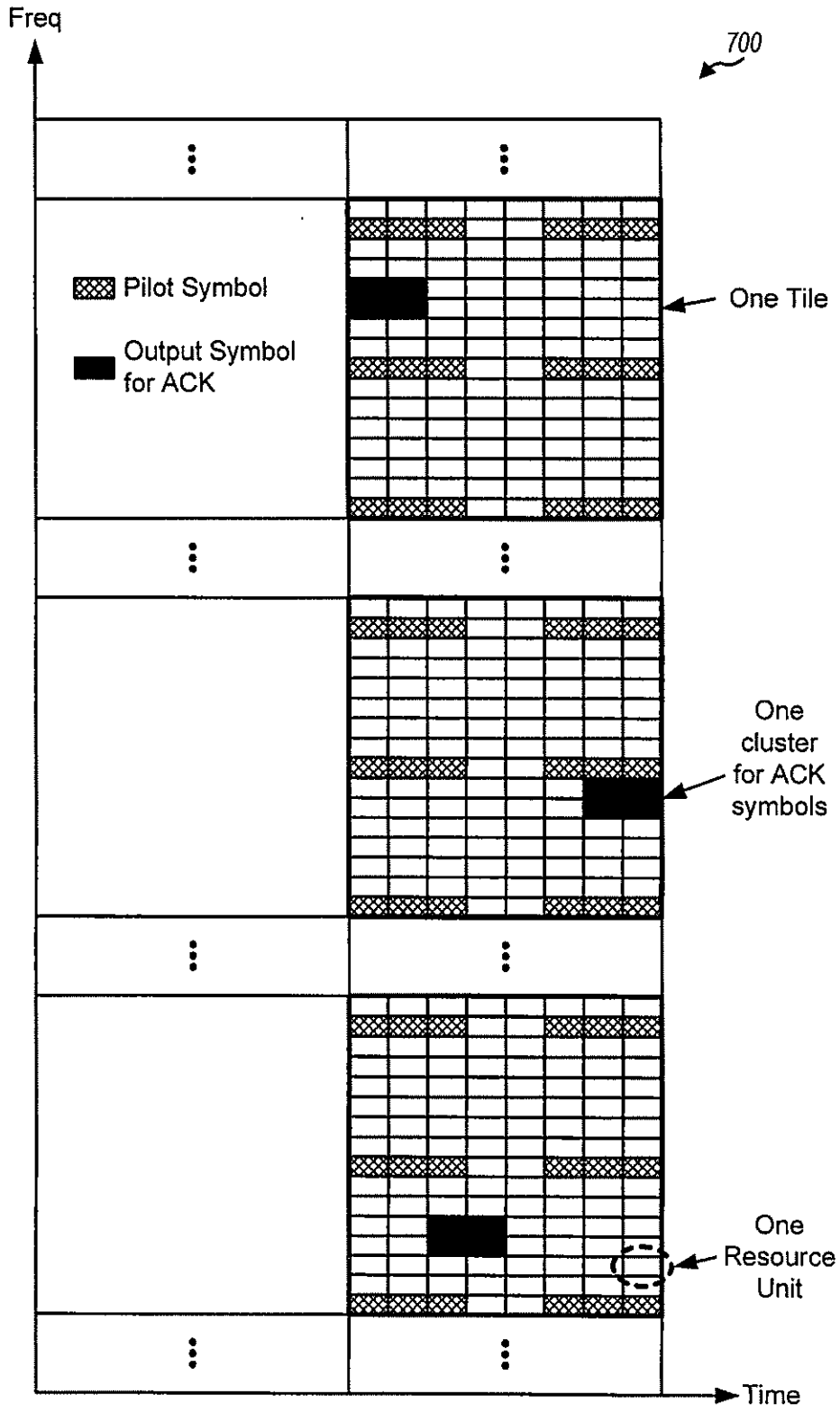
Freq
700
Pilot Symbol
Output Symbol for ACK
One Tile
One cluster for ACK symbols
One Resource Unit
Time

FIG. 7

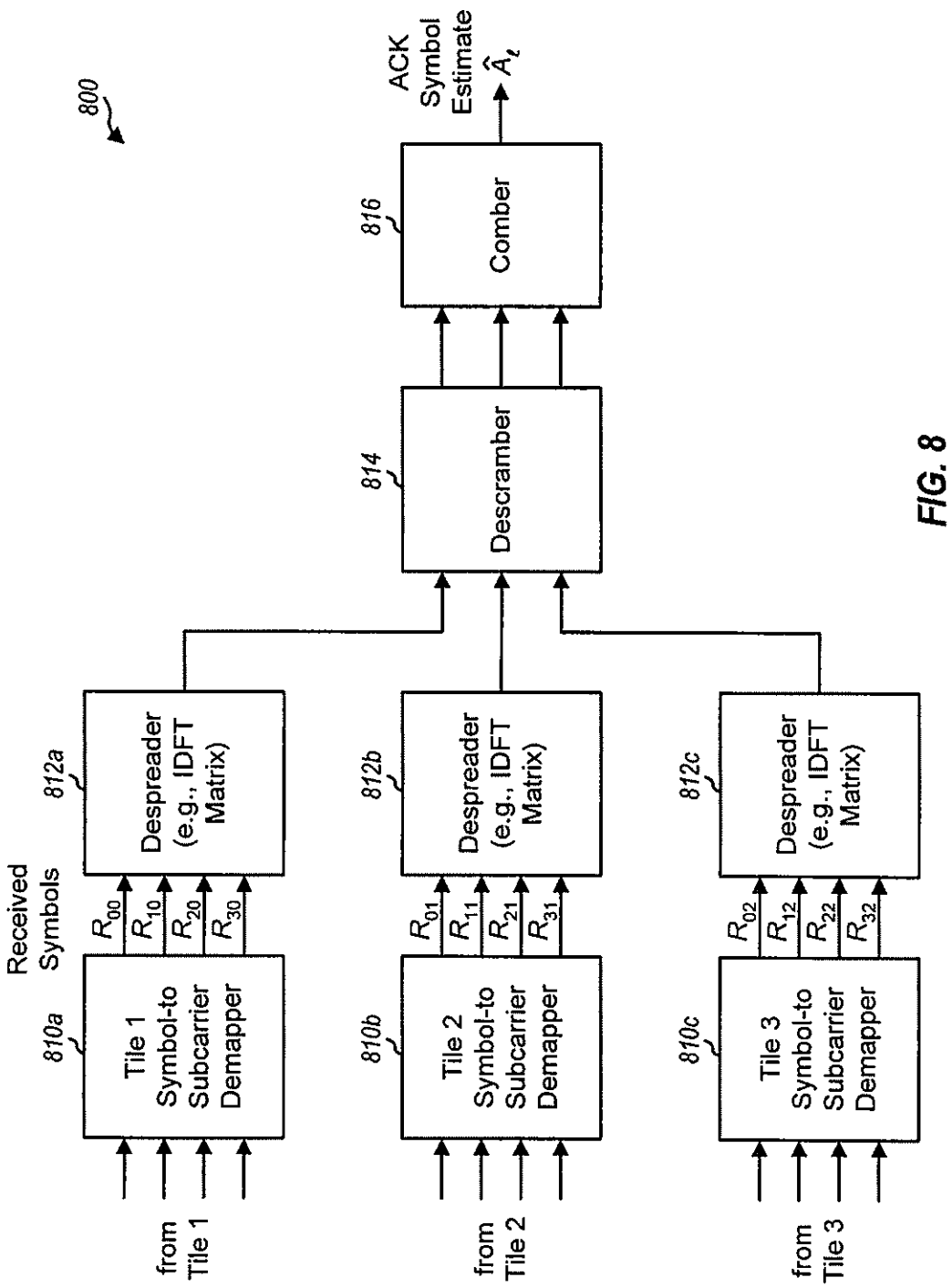
800
ACK Symbol Estimate $\hat{A}_t$
816
Comber
814
Descramber
812a
Despreader (e.g., IDFT Matrix)
812b
Despreader (e.g., IDFT Matrix)
812c
Despreader (e.g., IDFT Matrix)
Received Symbols
R_{00} R_{10} R_{20} R_{30}
R_{01} R_{11} R_{21} R_{31}
R_{02} R_{12} R_{22} R_{32}
810a
Tile 1 Symbol-to Subcarrier Demapper
810b
Tile 2 Symbol-to Subcarrier Demapper
810c
Tile 3 Symbol-to Subcarrier Demapper
from Tile 1
from Tile 2
from Tile 3

FIG. 8

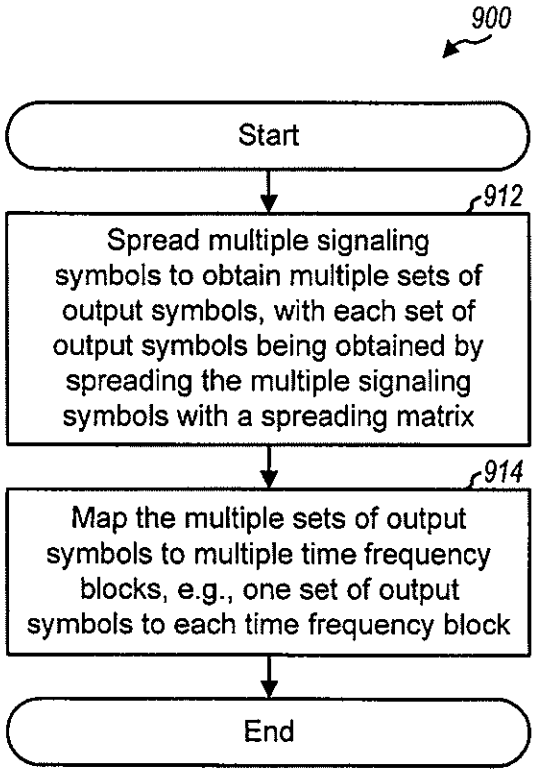
900
Start
912
Spread multiple signaling symbols to obtain multiple sets of output symbols, with each set of output symbols being obtained by spreading the multiple signaling symbols with a spreading matrix
914
Map the multiple sets of output symbols to multiple time frequency blocks, e.g., one set of output symbols to each time frequency block
End

FIG. 9

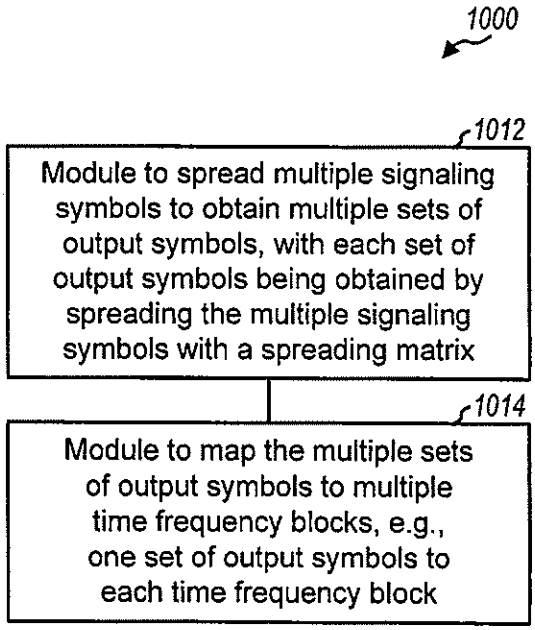
1000
1012
Module to spread multiple signaling symbols to obtain multiple sets of output symbols, with each set of output symbols being obtained by spreading the multiple signaling symbols with a spreading matrix
1014
Module to map the multiple sets of output symbols to multiple time frequency blocks, e.g., one set of output symbols to each time frequency block

FIG. 10

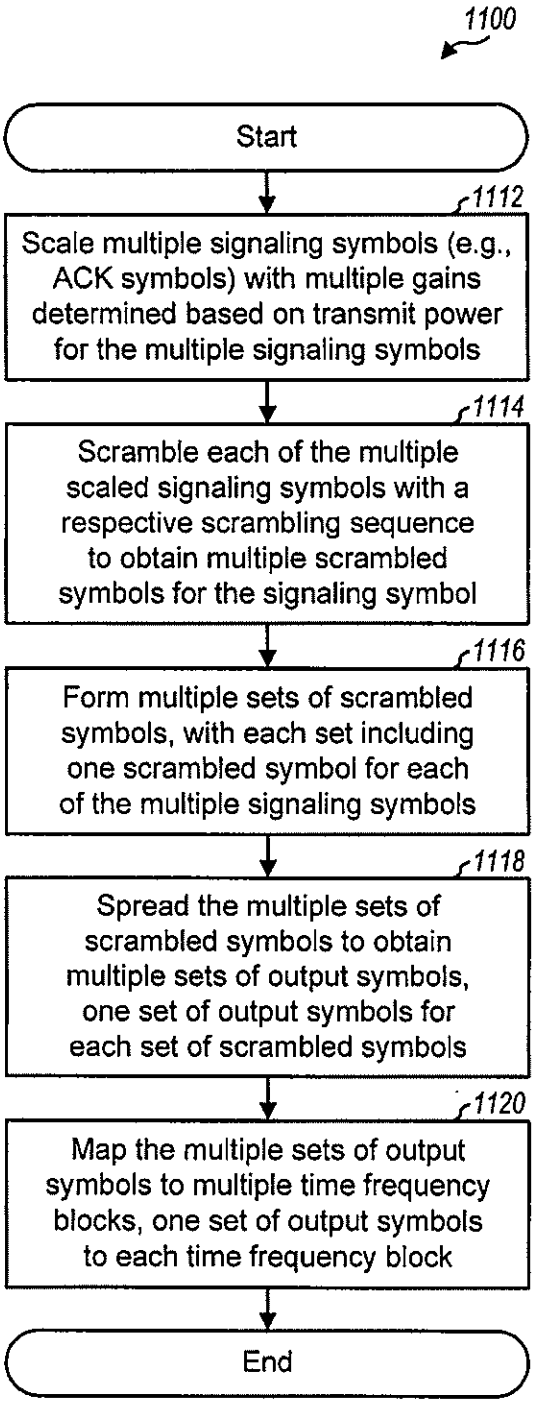
1100
Start
1112
Scale multiple signaling symbols (e.g., ACK symbols) with multiple gains determined based on transmit power for the multiple signaling symbols
1114
Scramble each of the multiple scaled signaling symbols with a respective scrambling sequence to obtain multiple scrambled symbols for the signaling symbol
1116
Form multiple sets of scrambled symbols, with each set including one scrambled symbol for each of the multiple signaling symbols
1118
Spread the multiple sets of scrambled symbols to obtain multiple sets of output symbols, one set of output symbols for each set of scrambled symbols
1120
Map the multiple sets of output symbols to multiple time frequency blocks, one set of output symbols to each time frequency block
End

FIG. 11

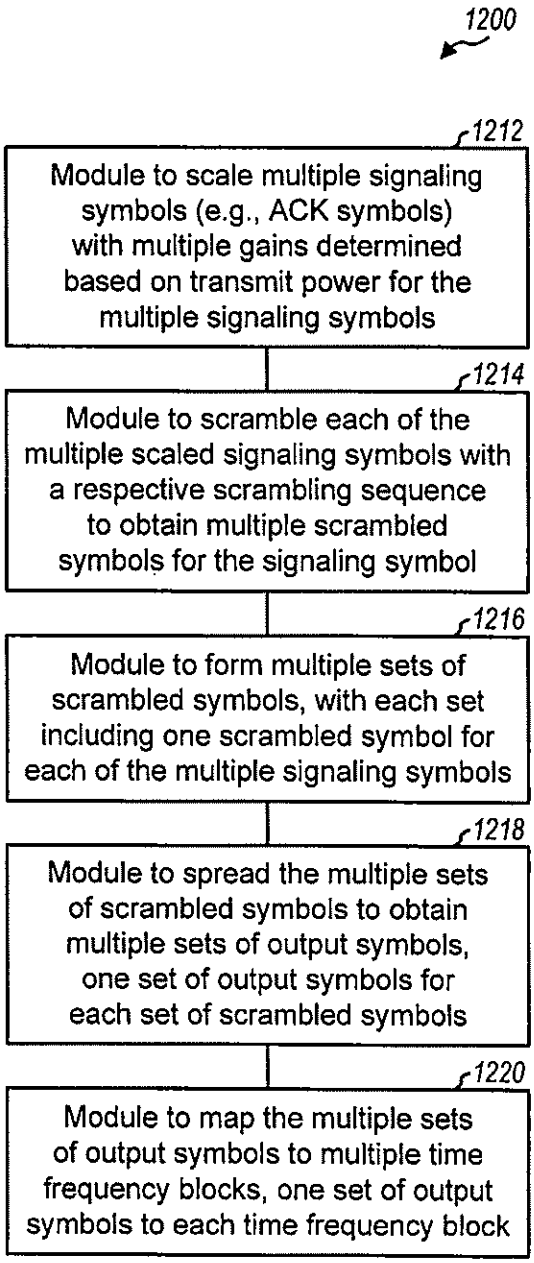
1200
1212
Module to scale multiple signaling symbols (e.g., ACK symbols) with multiple gains determined based on transmit power for the multiple signaling symbols
1214
Module to scramble each of the multiple scaled signaling symbols with a respective scrambling sequence to obtain multiple scrambled symbols for the signaling symbol
1216
Module to form multiple sets of scrambled symbols, with each set including one scrambled symbol for each of the multiple signaling symbols
1218
Module to spread the multiple sets of scrambled symbols to obtain multiple sets of output symbols, one set of output symbols for each set of scrambled symbols
1220
Module to map the multiple sets of output symbols to multiple time frequency blocks, one set of output symbols to each time frequency block

FIG. 12

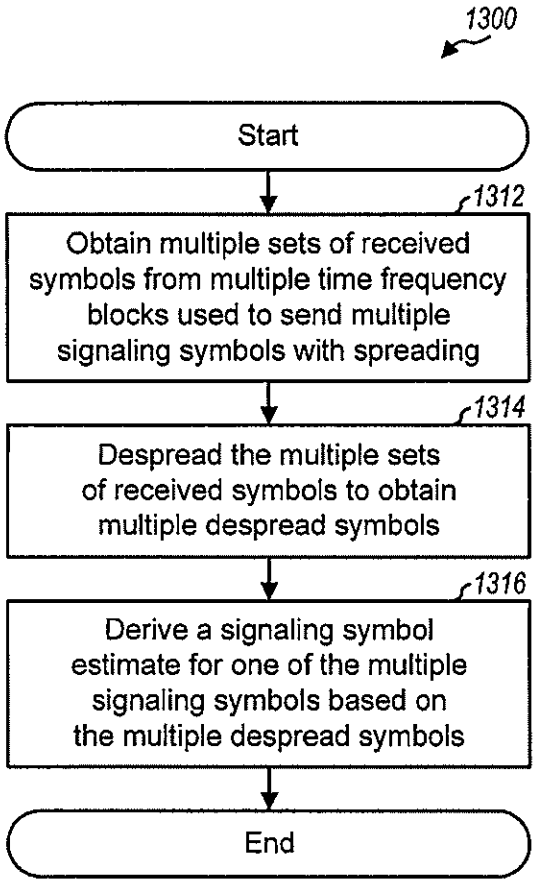
1300
Start
1312
Obtain multiple sets of received symbols from multiple time frequency blocks used to send multiple signaling symbols with spreading
1314
Despread the multiple sets of received symbols to obtain multiple despread symbols
1316
Derive a signaling symbol estimate for one of the multiple signaling symbols based on the multiple despread symbols
End

FIG. 13

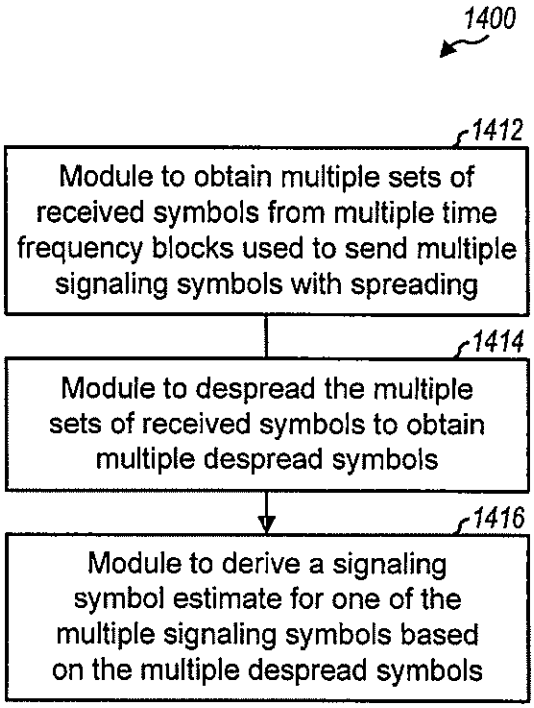
1400
1412
Module to obtain multiple sets of received symbols from multiple time frequency blocks used to send multiple signaling symbols with spreading
1414
Module to despread the multiple sets of received symbols to obtain multiple despread symbols
1416
Module to derive a signaling symbol estimate for one of the multiple signaling symbols based on the multiple despread symbols

FIG. 14

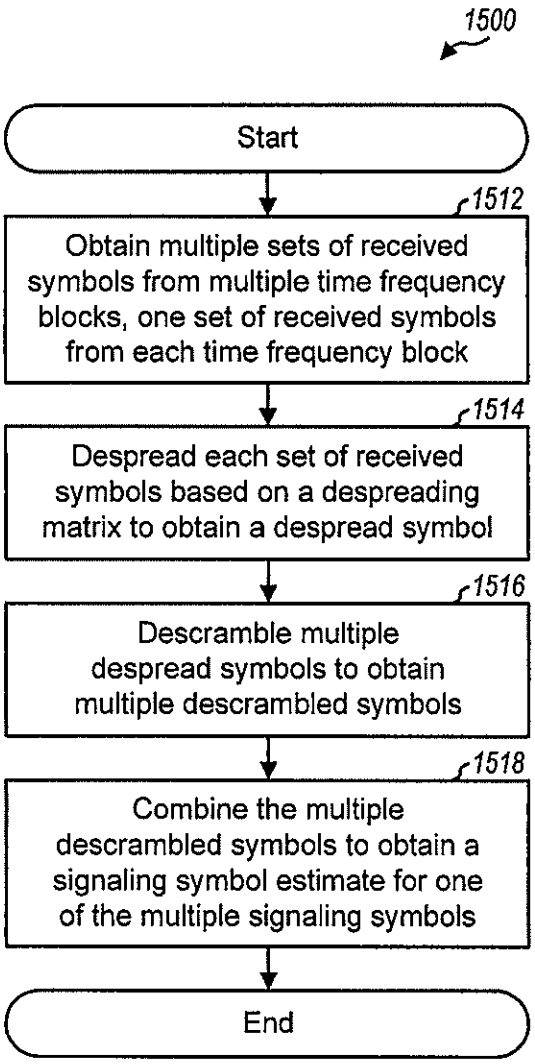
1500
Start
1512
Obtain multiple sets of received symbols from multiple time frequency blocks, one set of received symbols from each time frequency block
1514
Despread each set of received symbols based on a despreading matrix to obtain a despread symbol
1516
Descramble multiple despread symbols to obtain multiple descrambled symbols
1518
Combine the multiple descrambled symbols to obtain a signaling symbol estimate for one of the multiple signaling symbols
End

FIG. 15

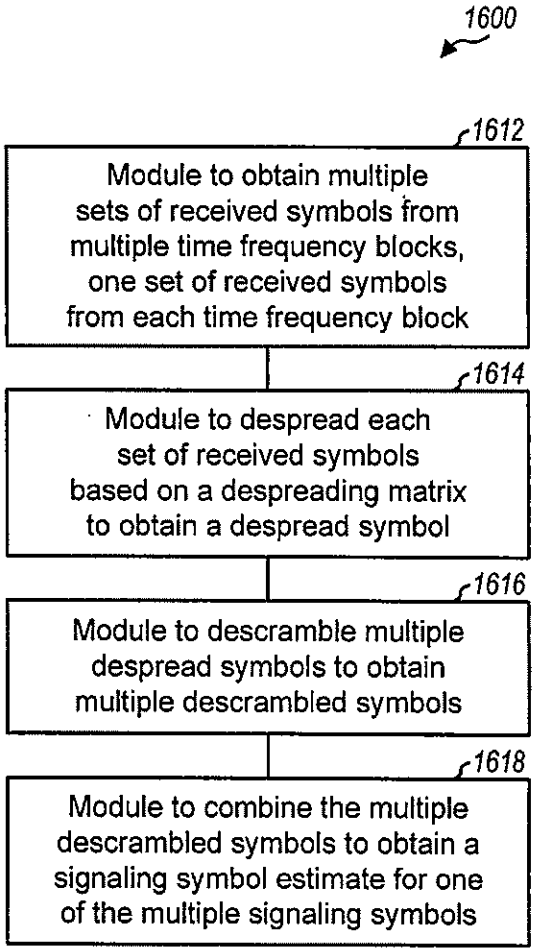
1600
1612
Module to obtain multiple sets of received symbols from multiple time frequency blocks, one set of received symbols from each time frequency block
1614
Module to despread each set of received symbols based on a despreading matrix to obtain a despread symbol
1616
Module to descramble multiple despread symbols to obtain multiple descrambled symbols
1618
Module to combine the multiple descrambled symbols to obtain a signaling symbol estimate for one of the multiple signaling symbols

FIG. 16

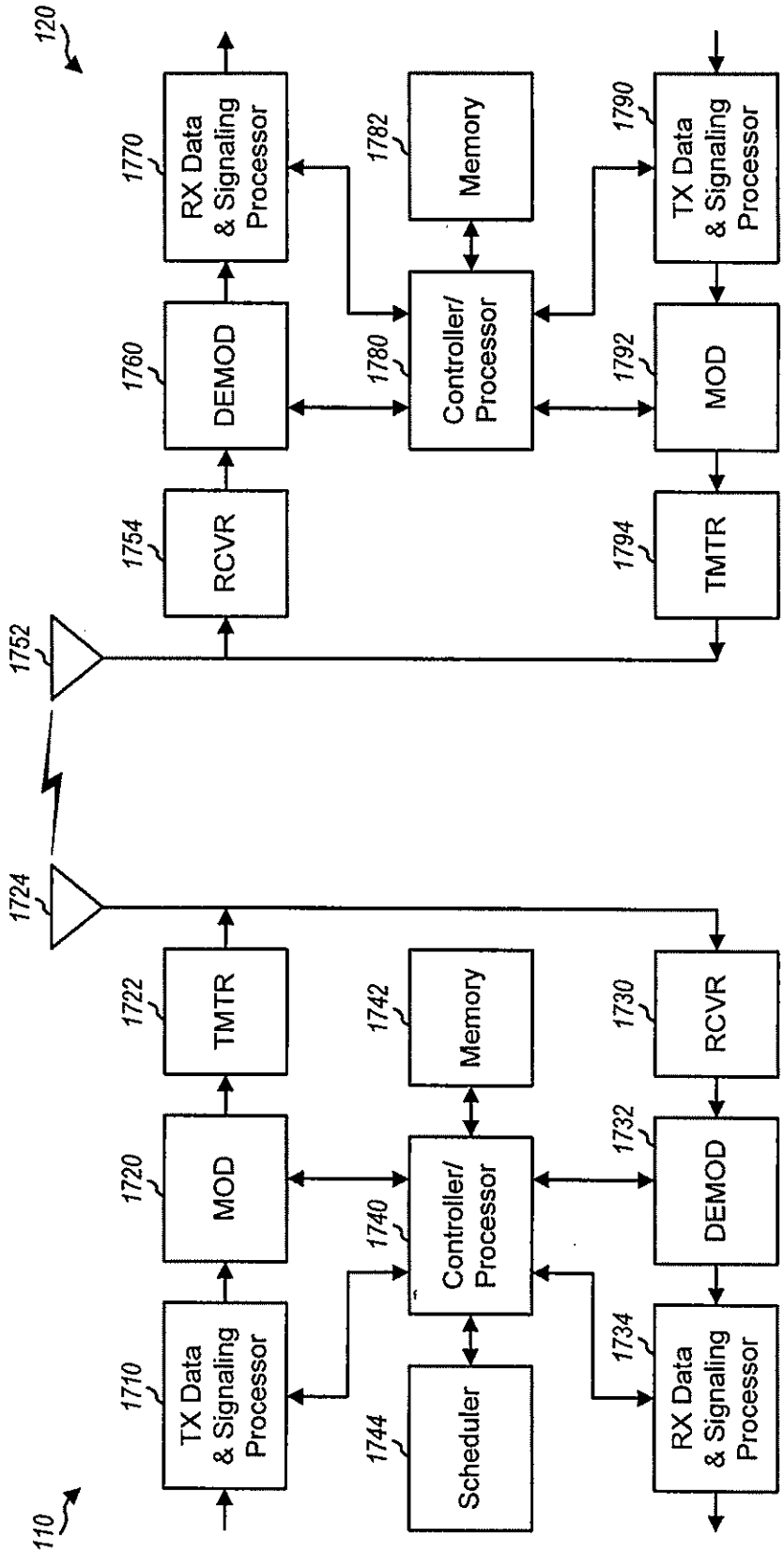
120
1770
RX Data & Signaling Processor
1782
Memory
1790
TX Data & Signaling Processor
1760
DEMOD
1780
Controller/ Processor
1792
MOD
1754
RCVR
1794
TMTR
1752
1724
1722
TMTR
1742
Memory
1730
RCVR
1720
MOD
1740
Controller/ Processor
1732
DEMOD
1710
TX Data & Signaling Processor
1744
Scheduler
1734
RX Data & Signaling Processor
110

FIG. 17