

(19) World Intellectual Property Organization  
International Bureau



(43) International Publication Date  
7 September 2001 (07.09.2001)

PCT

(10) International Publication Number  
**WO 01/65696 A2**

(51) International Patent Classification<sup>7</sup>: **H03K 19/00**

(21) International Application Number: PCT/US01/06442

(22) International Filing Date: 28 February 2001 (28.02.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:  
09/517,083 2 March 2000 (02.03.2000) US

(71) Applicant: **ADVANCED MICRO DEVICES, INC.**  
[US/US]; One AMD Place, Mail Stop 68, P.O. Box 3453,  
Sunnyvale, CA 94088-3453 (US).

(72) Inventor: **KIM, Yong**; 3450 Warburton Avenue, #10,  
Santa Clara, CA 95051 (US).

(74) Agent: **RODDY, Richard, J.**; Advanced Micro Devices,  
Inc., One AMD Place, Mail Stop 68, P.O. Box 3453, Sun-  
nyvale, CA 94088-3453 (US).

(81) Designated States (*national*): CN, JP, KR, SG.

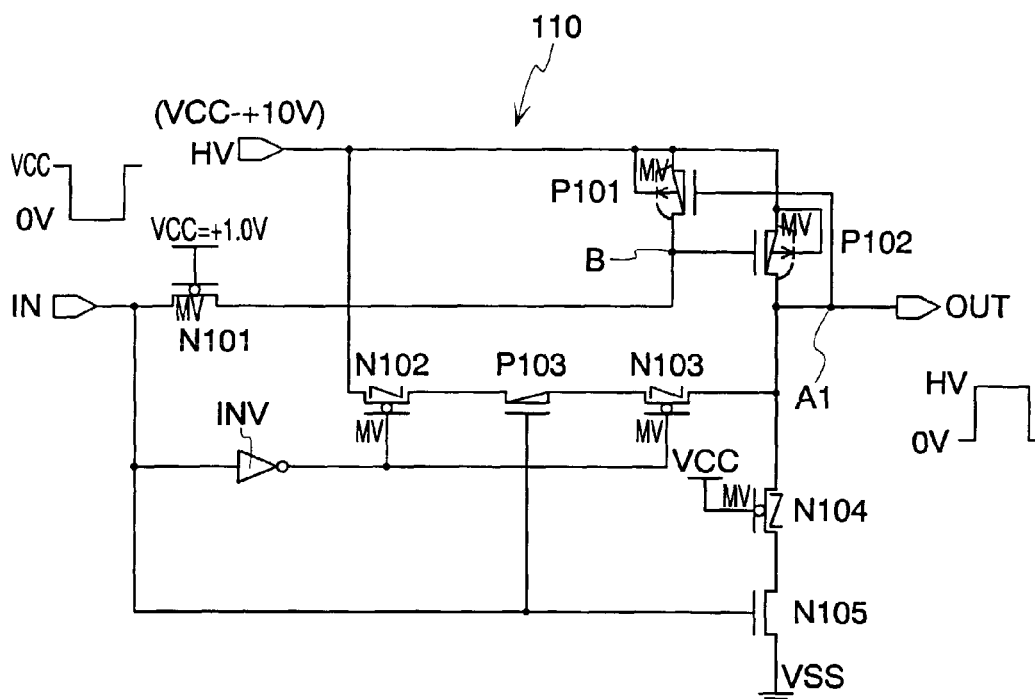
(84) Designated States (*regional*): European patent (AT, BE,  
CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC,  
NL, PT, SE, TR).

**Published:**

— without international search report and to be republished  
upon receipt of that report

For two-letter codes and other abbreviations, refer to the "Guid-  
ance Notes on Codes and Abbreviations" appearing at the begin-  
ning of each regular issue of the PCT Gazette.

(54) Title: LEVEL-SHIFTER FOR EXTREMELY LOW POWER SUPPLY



(57) Abstract: An improved level shifter circuit is provided which is designed for use with an extremely low power supply voltage. The level shifter circuit includes a fourth NMOS transistor (N102), a third PMOS transistor (P103), and a fifth NMOS transistor (N103) connected in series and interconnected between the high voltage and the output terminal. As a result, the high voltage will still be passed to the output terminal when the high voltage is lowered to be equal to the low power supply voltage.