

ABSTRACT OF THE DISCLOSURE

A nonvolatile memory (NVM) device includes a data pin, a control pin, an on-die termination (ODT) pin, and a plurality of NVM memory chips commonly connected to the data pin and the control pin. A first NVM chip among the NVM chips includes an ODT circuit. The first NVM chip determines one of an ODT write mode and an ODT read mode based on a control signal received through the control pin and an ODT signal received through the ODT pin, uses the ODT circuit to perform an ODT on the data pin during the ODT write mode, and uses the ODT circuit to perform the ODT on the control pin during the ODT read mode.

FIG. 1