WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a package base substrate comprising a base layer, a plurality of connection terminals on a first side of the base layer, and a plurality of electromagnetic shielding terminals spaced apart from one another on the first side of the base layer to provide a perimeter around the plurality of connection terminals;

a package body on a second side of the base layer that is opposite the first side, the package body comprising at least one semiconductor chip; and

an electromagnetic shielding layer on a surface of the package base substrate and on first and second surfaces of the package body,

wherein a value of a shortest distance between the plurality of connection terminals and the plurality of electromagnetic shielding terminals is equal to or higher than a separation distance between two adjacent ones of the plurality of electromagnetic shielding terminals; and

a ground plate layer extending along a portion of the first side of the base layer from an edge of the first side of the base layer,

wherein the ground plate layer is between the base layer and the plurality of electromagnetic shielding terminals, and

wherein the plurality of electromagnetic shielding terminals is electrically connected to the ground plate layer.

2. The semiconductor package of claim 1, wherein the electromagnetic shielding layer is electrically connected to the ground plate layer by contact with a side surface of the ground plate layer.

3. The semiconductor package of claim 1 or claim 2,

wherein the plurality of electromagnetic shielding terminals are on a lowermost surface of the ground plate layer, and

wherein the electromagnetic shielding layer extends lower than the lowermost surface of the ground plate layer.

4. The semiconductor package of any one of claims 1 to 3, further comprising:

a solder resist layer on a portion of the ground plate layer,

wherein the portion of the ground plate layer is between the solder resist layer and the base layer, and

wherein the electromagnetic shielding layer is on a side surface of the solder resist layer.

5. The semiconductor package of any one of claims 1 to 4, further comprising:

a dummy terminal on a through hole that separates first and second portions of the ground plate layer.

6. The semiconductor package of any one of claims 1 to 5,

wherein the separation distance between the two adjacent ones of the plurality of electromagnetic shielding terminals comprises a first spacing or a second spacing,

wherein first ones of the plurality of electromagnetic shielding terminals are spaced apart from one another by the first spacing, and second ones of the plurality of electromagnetic shielding terminals are spaced apart from one another by the second spacing, the second spacing being longer than the first spacing, and

wherein the value of the shortest distance between the plurality of connection terminals and the plurality of electromagnetic shielding terminals is higher than the first spacing and the second spacing.

7. The semiconductor package of claim 6, wherein adjacent ones of the first ones of the plurality of electromagnetic shielding terminals that are spaced apart from one another by the first spacing are adjacent a center line extending in a long-axis direction of the package base substrate.

8. The semiconductor package of any one of claims 1 to 7, wherein the plurality of electromagnetic shielding terminals are symmetric about each of a first center line extending in a long-axis direction of the package base substrate and a second center line extending in a short-axis direction of the package base substrate.

9. The semiconductor package of any one of claims 1 to 7, wherein the plurality of electromagnetic shielding terminals are symmetric about a first center line extending in a

diagonal direction of the package base substrate and are asymmetric about each of a second center line extending in a long-axis direction of the package base substrate and a third center line extending in a short-axis direction of the package base substrate.

10. A semiconductor package comprising:

a package base substrate comprising a bridge region, a fence region around the bridge region, a spacing region between the bridge region and the fence region, an edge region around the fence region, a base layer, a plurality of connection terminals on a lower surface of the base layer, a ground plate layer on an end portion of the lower surface of the base layer, and a plurality of electromagnetic shielding terminals electrically connected to the ground plate layer in the fence region around the plurality of connection terminals; wherein the ground plate layer extends along a portion of the first side of the base layer from an edge of the edge region;

a package body on the package base substrate, the package body comprising a plurality of semiconductor chips; and

an electromagnetic shielding layer on a side surface of the package base substrate and a side surface and an upper surface of the package body and contacting a side surface of the ground plate layer,

wherein a width of the spacing region is equal to or greater than a separation distance between two adjacent ones of the plurality of electromagnetic shielding terminals.

11. The semiconductor package of claim 10,

wherein the plurality of semiconductor chips comprises a first semiconductor chip and a second semiconductor chip,

wherein the first semiconductor chip is electrically connected to the second semiconductor chip through a NAND interface,

wherein the second semiconductor chip is electrically connected to first ones of the plurality of connection terminals through a host interface, and

wherein the semiconductor package further comprises a plurality of test pads on the lower surface of the base layer in at least one of the spacing region or the bridge region and electrically connected to the NAND interface.

12. The semiconductor package of claim 11, wherein the plurality of semiconductor chips further comprises a third semiconductor chip electrically connected to second ones of the plurality of connection terminals through a DRAM interface.

13. The semiconductor package of any one of claims 10 to 12, wherein the plurality of electromagnetic shielding terminals comprises two rows of the plurality of electromagnetic shielding terminals along a periphery of the plurality of connection terminals.

14. The semiconductor package of claim 13, wherein the plurality of electromagnetic shielding terminals defines a zigzag pattern along a periphery of the plurality of connection terminals.

15. The semiconductor package of any one of claims 10 to 14,

wherein a ratio of a first width of the edge region to a first width of the spacing region in a long-axis direction of the package base substrate is greater than one, and

wherein a ratio of a second width of the edge region to a second width of the spacing region in a short-axis direction of the package base substrate is less than one.

16. A semiconductor package comprising:

a package base substrate comprising a base layer, a plurality of connection terminals on a bottom of the base layer to provide a ball map, a ground plate layer on the bottom of the base layer, and a plurality of electromagnetic shielding terminals attached to a bottom of the ground plate layer, the plurality of electromagnetic shielding terminals being spaced apart from one another to provide a ground fence around the ball map;

a package body on the package base substrate, the package body comprising a plurality of semiconductor chips and an encapsulation layer that is on a top of the package base substrate and is on the plurality of semiconductor chips; and

an electromagnetic shielding layer on a side surface of the package base substrate and a side surface and a top of the package body and contacting the ground plate layer,

wherein the ground plate layer extends along the bottom of the base layer from an edge of a first side of the base layer, and

wherein a shortest distance between the ball map and the ground fence is equal to or greater than a separation distance between two adjacent ones of the plurality of electromagnetic shielding terminals.

17. The semiconductor package of claim 16, further comprising:

a bottom solder resist layer on a portion of the ground plate layer,

wherein the electromagnetic shielding layer extends lower than the bottom of the ground plate layer and is on a side surface of the bottom solder resist layer.

18. The semiconductor package of claim 16 or 17, wherein the ground fence comprises a polygonal shape comprising four vertex portions around the ball map.

19. The semiconductor package of claim 18, further comprising:

four dummy terminals in the four vertex portions, respectively, of the ground fence,

wherein the four dummy terminals are electrically insulated from the ground plate layer.