

APPARATUSES AND METHODS INCLUDING MEMORY AND OPERATION OF SAME

BACKGROUND

[001] Traditional memory cells include a memory element, which is used to store a logic state, and a selector device. The memory element and selector device may be located at a cross-point of a first signal line (e.g., word line) and a second signal line (e.g., bit line) in a memory array having a cross-point architecture. The selector may be coupled to the word line and the memory element may be coupled to the bit line in some architectures. The selector device may reduce leakage currents and allow selection of a single memory element for reading data and/or writing data. However, the use of separate memory elements and selector devices increases the number of materials and/or layers that must be formed during fabrication of the memory device, thus increasing the complexity of the structure and fabrication process. Moreover, activating the selector device and writing or reading the memory element may require high voltage and/or long duration pulses to be provided, which may increase power consumption of the memory device.

SUMMARY

[002] An example apparatus according to an embodiment of the disclosure may include a memory cell that may be configured to store a logic state, a first memory access line coupled to the memory cell, and a second memory access line coupled to the memory cell, wherein the first and second memory access lines may be configured to provide a first voltage having a first polarity across the memory cell to write a first logic state to the memory cell and the first and second memory access lines may be further configured to provide a second voltage having a second polarity across the memory cell to write a second logic state to the memory cell.

[003] Another example apparatus according to an embodiment of the disclosure may include a memory cell that may be configured to exhibit a first threshold voltage when in a first logic state and a second threshold voltage when in a second logic state responsive to a read operation, wherein the memory cell may be configured to act as a memory element and a selector device, a first memory access line coupled to the

shown in Figure 1, WL 105 extends parallel to the page and BL 125 extends into the page. A memory cell 115 may be located at an intersection of the WL 105 and the BL 125. The memory cell 115 may be coupled to WL 105 by a first electrode 110 and coupled to BL 125 by a second electrode 120. The memory cell 115 may include a layer of phase change material. In some embodiments, the chalcogenide may be phase change material. In some embodiments, the memory cell 115 may include a ternary composition that may include selenium (Se), arsenic (As), and germanium (Ge). In some embodiments, the memory cell 115 may include a quaternary composition that may include silicon (Si), Se, As, and Ge. Other materials may also be used. The memory cell 115 may act as both a selector device and a memory element.

[025] The memory cell 115 may be written to store one of at least two different logic states (e.g., '1,' '0') by a write operation. In some embodiments, the different logic states may be represented by different threshold voltages (V_{TH}) of the memory cell 115. For example, a '1' logic state may be represented by a first V_{TH} and a '0' logic state may be represented by a second V_{TH} . The threshold voltage the memory cell 115 exhibits may be based on a polarity of a write pulse applied to the memory cell 115 during a write operation and a polarity of a read pulse applied to the memory cell 115 during a read operation. The write pulse and read pulse may be applied to the memory cell 115 using the first and second access lines 105 and 125.

[026] The memory cell 115 may be configured as a two-terminal device between the BL 125 and WL 105 in some embodiments. A first logic state may be written to the memory cell 115 by applying a voltage (e.g., a write pulse) across the memory cell 115 in a first polarity. A second logic state may be written to the memory cell 115 by applying a voltage (e.g., a write pulse) across the memory cell 115 in a second polarity, which may be opposite to the first polarity. The memory cell 115 is read by applying a voltage (e.g., a read pulse) across the terminals. In some embodiments, the memory cell 115 is read by applying a voltage across the memory cell 115 in the first polarity. In other embodiments, the memory cell 115 is read by applying a voltage across the memory cell 115 in the second polarity. The memory cell 115 may always be read with the same polarity. When the memory cell 115 is read with a voltage in the same voltage polarity with which the memory cell 115 was written, the memory cell 115 may exhibit a first V_{TH} . When the memory cell 115 is read with a voltage in the opposite

[032] As shown in Figure 3B, when the memory cell in State₀ is read by a read pulse (Read₁) in the opposite polarity having a voltage with a magnitude equal to or greater than V_{TH0} , the memory cell may be rewritten to State₁. The memory cell will exhibit V_{TH1} during a subsequent read (Read₂). That is, when the read pulse has a voltage greater than or equal to V_{TH0} of a memory cell previously written in the opposite polarity as the read pulse, the read may be destructive for cells in State₀. After a first read pulse, the memory cell may be rewritten to restore the logic state of the memory cell for a future read operation.

[033] Figure 3C is a voltage plot 300C of threshold voltages of a memory cell in State₀ according to an embodiment of the disclosure. Figure 3C illustrates two read pulses applied to the memory cell in State₀. A first read pulse Read₁ may be applied to the memory cell. The memory cell may have been written to with a write pulse in the opposite polarity as the polarity of Read₁. Read₁ may have a voltage less than the threshold voltage of the memory cell in State₀. When Read₁ is applied, the memory cell exhibits threshold voltage V_{TH0} , corresponding to State₀. However, the memory cell does not threshold. A second read pulse Read₂ may be applied to the memory cell. Read₂ has the same polarity as Read₁. When Read₂ is applied, the memory cell exhibits threshold voltage V_{TH0} , corresponding to State₀, and similar to when Read₁ was applied, the memory cell does not threshold.

[034] As shown in Figure 3C, when the memory cell in State₀ is read by a read pulse (Read₁) in the opposite polarity having a voltage with a magnitude less than V_{TH0} , the memory cell may maintain State₀. The memory cell may continue to exhibit V_{TH0} during a subsequent read pulse (e.g., Read₂). That is, when the read pulse has a voltage less than V_{TH0} , the read pulse may not modify the logic state of the cell. As shown in Figure 3C, the magnitude of the read pulses Read₁ and Read₂ may be selected to be between threshold voltages V_{TH0} and V_{TH1} .

[035] As shown in Figures 3A-C, a read pulse may or may not affect the logic state of a memory cell, based at least in part, on the magnitude of the voltage of the read pulse and the logic state of the memory cell. A voltage magnitude of the read pulse may be selected based on the desired effect of the read pulse on the memory cell (e.g., less than V_{TH0} for non-destructive read, greater than V_{TH0} for destructive read).

materials may be used. In some embodiments, the selector device 915 may also include a layer of chalcogenide material. Other materials may also be used.

[059] In an alternative embodiment of the disclosure, the protocols for reading and writing a memory cell with different voltage polarities as described in reference to Figures 4-8 may be applied to a selector device and memory element of a memory array, for example, selector device 915 and memory element 925 shown in Figure 9. Similar to memory cell 115 illustrated in Figure 1, the selector device and memory element may be written to two or more logic states represented by different threshold voltages as shown in Figure 2. The threshold voltage effects of the different read and write polarities may be additive across the selector device and the memory element. As shown in the voltage plot of Figure 10, a difference between the threshold voltages of different logic states for the selector device and memory element may be greater than the difference between threshold voltages of different logic states of a memory cell. That is, $|V_{TH0}-V_{TH1}| < |V_{TH0+N}-V_{TH1}|$ where V_{TH0+N} is the voltage V_{TH0} summed with the additional difference in magnitude between threshold voltages of the different logic states due to the additive effect of the selector device and memory element. This larger difference between threshold voltages may provide a wider margin for detecting different logic states. Although State₁ is shown in Figure 10 as having the same threshold voltage V_{TH1} for both the memory cell and the selector device and memory element, the threshold voltage for State₁ for the memory cell may be different from the threshold voltage for State₁ of the selector device and memory element in some embodiments.

[060] Figure 11 illustrates a memory 1100 according to an embodiment of the disclosure. The memory 1100 includes a memory array 1160 with a plurality of memory cells that are configured to store data. The memory cells may be accessed in the array through the use of various signal lines, word lines (WLs) and bit lines (BLs). The memory cells may be non-volatile memory cells, such as phase change memory cells, or may generally be any type of memory cells. The memory cells may be single level cells configured to store data for one bit of data. The memory cells may also be multi-level cells configured to store data for more than one bit of data.

[061] Commands, address information, and write data may be provided to the memory 1100 as sets of sequential input/output (I/O) transmitted through an I/O bus

1128. Similarly, read data may be provided from the memory 1100 through the I/O bus 1128. A data strobe signal DQS may be transmitted through a data strobe bus 1130. The DQS signal may be used to provide timing information for the transfer of data to the memory or from the memory. The I/O bus 1128 is connected to an I/O control circuit 1120 that routes data signals, address information signals, and other signals between the I/O bus 1128 and an internal data bus 1122, an internal address bus 1124, and an internal command bus 1126. An address register 1125 may be provided address information by the I/O control circuit 1120 to be temporarily stored. The I/O control circuit 1120 is coupled to a status register 1134 through a status register bus 1132. Status bits stored by the status register 1134 may be provided by the I/O control circuit 1120 responsive to a read status command provided to the memory 1100. The status bits may have respective values to indicate a status condition of various aspects of the memory and its operation.

[062] The memory 1100 also includes a control logic 1110 that receives a number of control signals either externally (e.g., CE#, CLE, ALE, CLK, W/R#, and WP#) or through the command bus 1126 to control the operation of the memory 1100. A command register 1136 is coupled to the internal command bus 1126 to store information received by the I/O control circuit 1120 and provide the information to the control logic 1110. The control logic 1110 may further access a status register 1134 through the status register bus 1132, for example, to update the status bits as status conditions change. The control logic 1110 is further coupled to a ready/busy circuit 1138 to control a value (e.g., logic value) of a ready/busy signal R/B# that may be provided by the memory 1100 to indicate whether the memory is ready for an operation or is busy. The control logic 1110 may be configured to provide internal control signals to various circuits of the memory 1100. For example, responsive to receiving a memory access command (e.g., read, write, program), the control logic 1110 may provide internal control signals to control various memory access circuits to perform a memory access operation. The various memory access circuits are used during the memory access operation, and may generally include circuits such as row and column decoders, signal line drivers, data 1180 and cache registers 1170, I/O circuits, as well as others.

- [063]** The address register 1125 provides block-row address signals to a row decoder 1140 and column address signals to a column decoder 1150. The row decoder 1140 and column decoder 1150 may be used to select blocks of memory cells for memory operations, for example, read, program, and erase operations. The row decoder 1140 and/or the column decoder 1150 may include one or more signal line drivers configured to provide a biasing signal to one or more of the signal lines in the memory array 1160.
- [064]** In some embodiments, during a write operation on a memory cell of the memory array 1160, a first voltage (e.g., 0V) may be provided to a selected word line and a second voltage may be provided to a selected bit line. The memory cell may be at the intersection of the selected word line and bit line. The second voltage may be higher or lower than the voltage provided to the word line, based on the logic state to be stored at the address corresponding to the selected word line and bit line (e.g., -6V for '1' and +6V for '0'). In some embodiments, during a write operation, the selected bit line may always be provided a specific voltage, and the word line may be provided a voltage higher or lower than the voltage of the bit line, based on the logic state to be stored at the address.
- [065]** In some embodiments, during a read operation on a memory cell, a first voltage (e.g., 0V) may be provided to a selected word line and a second voltage (e.g., -5V, +5V) may be provided to a selected bit line. The memory cell may be at the intersection of the selected word line and bit line. The second voltage may be greater than or less than the first voltage provided to the word line, however, the second voltage may provide the same voltage polarity for every read operation. The logic state of the memory cell may be sensed by a sense amplifier coupled to the selected bit line. The sensed logic state of the memory cell may be provided to the data register 180.
- [066]** Figure 12 is a diagram illustrating a portion of an array 1200 of memory cells according to an embodiment of the disclosure. The array 1200 may be used to implement the memory array 1160 of Figure 11 in some embodiments. In the example illustrated in Figure 12, the array 1200 is a cross-point array including a first number of conductive lines 1230-0, 1230-1, . . . , 1230-N, e.g., access lines, which may be referred to herein as word lines, and a second number of conductive lines 1220-0, 1220-1, . . . , 1220-M, e.g., access lines, which may be referred to herein as bit lines. A memory cell 1225 is located at each of the intersections of the word lines 1230-0, 1230-1, . . . ,

CLAIMS

What is claimed is:

1. An apparatus, comprising:
a memory cell configured to store a logic state;
a first memory access line coupled to the memory cell; and
a second memory access line coupled to the memory cell,
wherein the first and second memory access lines are configured to provide a first voltage having a first polarity across the memory cell to write a first logic state to the memory cell and provide a second voltage having a second polarity across the memory cell to write a second logic state to the memory cell.
2. The apparatus of claim 1, wherein, during a read operation on the memory cell, the memory cell exhibits a first threshold voltage representative of the first logic state responsive to the first voltage having the first polarity provided to write to the memory cell,
or the memory cell exhibits a second threshold voltage representative of the second logic state responsive to the second voltage having the second polarity provided to write to the memory cell.
3. The apparatus of claim 1, wherein the memory cell comprises a chalcogenide material.
4. The apparatus of claim 3, wherein the chalcogenide material is not a phase change material.
5. The apparatus of claim 1, wherein the memory cell comprises at least one of silicon (Si), selenium (Se), arsenic (As), and germanium (Ge).
6. The apparatus of claim 1, wherein the memory cell is a two-terminal threshold switching device.

7. The apparatus of claim 1, wherein the memory cell comprises a selector device coupled to the first memory access line and a memory element coupled to the selector device and the second memory access line.

8. The apparatus of claim 1, wherein the first memory access line is configured to provide a negative voltage and the second memory access line is configured to provide a positive voltage to provide the first voltage having the first polarity.

9. The apparatus of claim 1, wherein the first memory access line is configured to provide a first non-negative voltage and the second memory access line is configured to provide a second non-negative voltage to provide the first voltage having the first polarity, wherein the second non-negative voltage is greater than the first non-negative voltage.

10. An apparatus, comprising:

a memory cell configured to exhibit a first threshold voltage when in a first logic state and a second threshold voltage when in a second logic state responsive to a read operation, wherein the memory cell is further configured to act as a memory element and a selector device;

a first memory access line coupled to the memory cell; and

a second memory access line coupled to the memory cell,

wherein the first and second memory access lines are configured to provide a read pulse during the read operation, the read pulse having a first polarity.

11. The apparatus of claim 10, wherein the first and second memory access lines are further configured to provide a write pulse having the first polarity or a second polarity during a write operation.

12. The apparatus of claim 11, wherein the first memory access line is configured to provide a negative voltage and the second memory access line is

configured to provide a positive voltage to provide the write pulse having the first polarity.

13. The apparatus of claim 11, wherein the first memory access line is configured to provide a first non-negative voltage and the second memory access line is configured to provide a second non-negative voltage to provide the write pulse having the first polarity, wherein the second non-negative voltage is greater than the first non-negative voltage.

14. The apparatus of claim 11, wherein the memory cell exhibits the first threshold voltage responsive to the read operation when the write pulse having the first polarity was provided during the write operation and the memory cell exhibits the second threshold voltage responsive to the read operation when the write pulse having the second polarity was provided during the write operation.

15. The apparatus of claim 10, further comprising a memory array including a plurality of memory cells and a plurality of memory access lines coupled to at least some of the plurality of memory cells,

wherein the memory cell is one of the plurality of memory cells and the first and second memory access lines are each one of the plurality of memory access lines.

16. The apparatus of claim 15, wherein the memory array is a two-dimensional array.

17. The apparatus of claim 15, wherein the memory array is a three-dimensional array.

18. The apparatus of claim 10, further comprising:
a first electrode coupled between the memory cell and the first memory access line; and
a second electrode coupled between the memory cell and the second memory access line.