

ABSTRACT

A sequential circuit includes a first gate circuit, a second gate circuit and an output circuit. The first circuit generates a first signal based on an input signal, an input clock signal and a second signal. The second circuit generates an internal clock signal by performing a NOR operation on the first signal and an inversion clock signal which is inverted from the input clock signal, and generates the second signal based on the internal clock signal and the input signal. The output circuit generates an output signal based on the second signal. Operation speed of the sequential circuit and the integrated circuit including the same may be increased by increasing the negative setup time reflecting a transition of the input signal after a transition of the input clock signal, through mutual controls between the first circuit and the second circuit.

FIG. 1