METHOD OF FABRICATING T-SHAPED RECESSED POLYSILICON GATE TRANSISTORS

ABSTRACT

A patterned pad and a lower nitride layers are formed over a substrate defining a gate opening over a gate area. A gate trench is formed in the substrate through the gate opening. A gate oxide layer is formed on the sidewalls and bottom of the gate trench. A gate is formed over the gate oxide layer. The lower SiN and pad dielectric layers are removed. A first oxide layer is formed over the gate and the substrate. Low doped drain (LDD) regions are formed adjacent to the gate. A first nitride layer is formed over the first oxide layer. The first nitride and first oxide layers are etched to form first and second spacers on the gate sidewalls. Source and drain regions are formed adjacent to the first and second spacers. Silicide contacts are formed to the source and drain regions and silicide gate contacts are formed to the gate.

Fig. 19