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(54) Title: PASSIVATION OF ETCHED SEMICONDUCTOR STRUCTURES

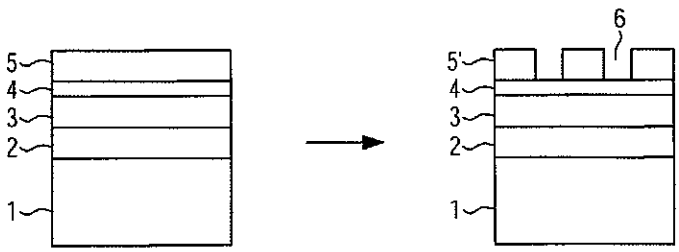


FIG. 1

(57) Abstract: The present invention relates to a method for passivation of a semiconductor structure, comprising the steps providing at least one first material layer; forming at least one second material layer that is to be patterned above the first material layer; forming a diffusion barrier layer between the at least one second material layer and the at least one first material layer thereby forming a multilayer stack and patterning, in particular, etching, the at least one second material layer down to but not completely through the diffusion barrier layer and without exposing portions of the at least one first material layer such that diffusion of material of the at least one first material layer through the diffusion barrier layer during a subsequent heat treatment of the multilayer stack is substantially prevented. The invention also relates to a method for passivation of a semiconductor structure, comprising the steps providing a multilayer stack comprising at least one buried layer formed below a second material layer; patterning, in particular, etching, the surface of the multilayer stack through the second material layer thereby exposing portions of the at least one buried layer and depositing a diffusion barrier layer at least on the exposed portions of the at least one buried layer such that diffusion of material of the at least one buried layer through the diffusion barrier layer during a subsequent heat treatment of the multilayer stack is substantially prevented.

WO 2010/015301 A1