ABSTRACT

A SILICON NITRIDE - TEOS OXIDE, SALICIDE BLOCKING LAYER FOR DEEP SUB-MICRON DEVICES

A method for forming self-aligned, metal silicide, (salicide), layers, on polysilicon gate structures, and on source/drain regions, located in a first region of a semiconductor substrate, while avoiding the salicide formation, on polysilicon gate structures, and on source/drain regions, located in a second region of a semiconductor substrate, has been developed. A composite insulator shape, comprising an overlying silicon nitride layer, and an underlying TEOS deposited, silicon oxide layer, is used to block polysilicon, as well as silicon regions, in the second region of the semiconductor substrate, from salicide formation. Unwanted silicon oxide spacers, created on the sides of polysilicon gate structures, during the patterning of the composite insulator shape, is selectively removed using dilute hydrofluoric acid solutions.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)