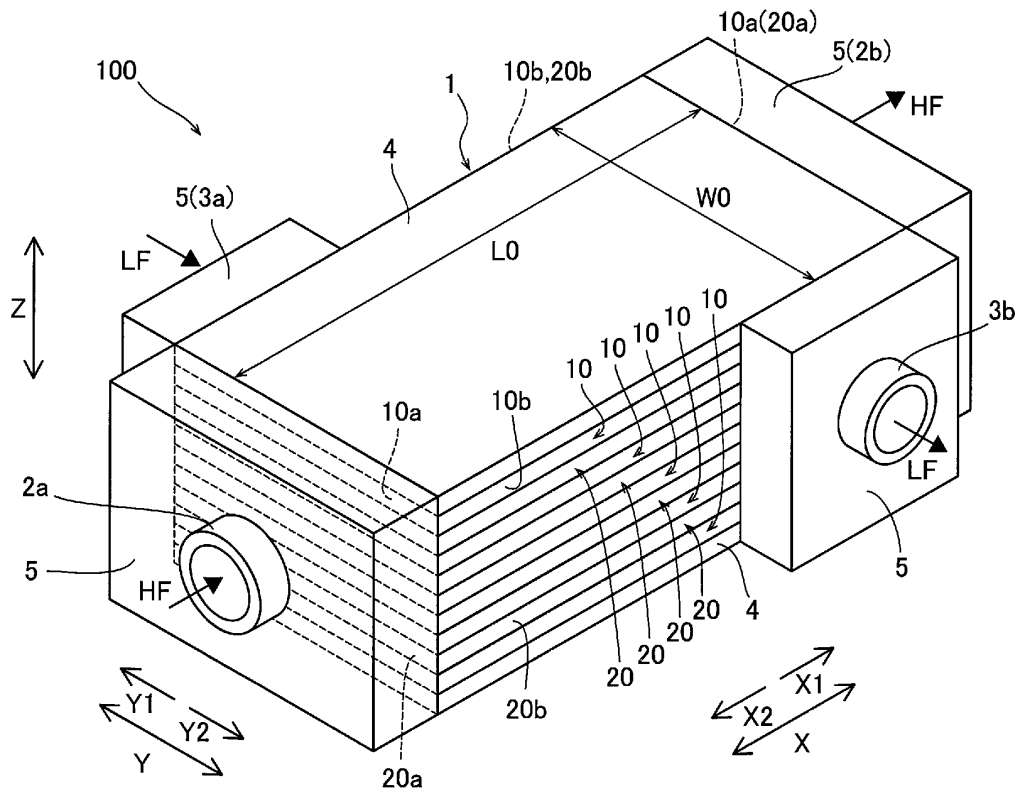


[図1]



[図2]

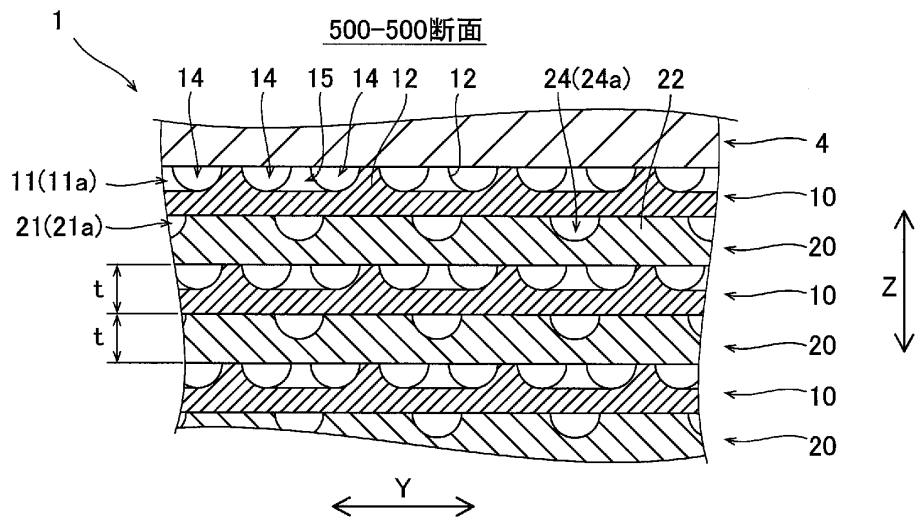


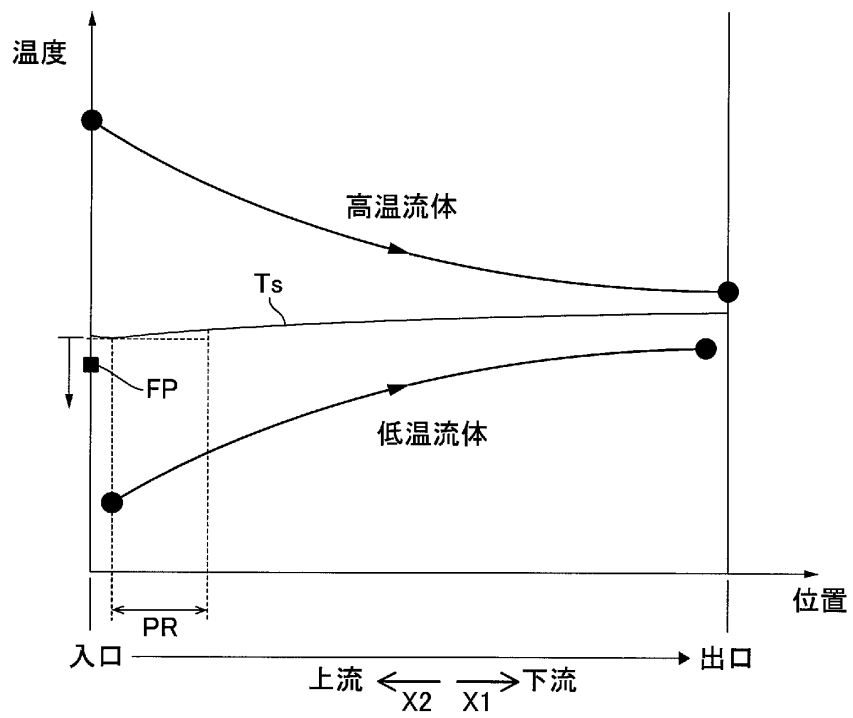
Figure 1 is a cross-sectional view of a semiconductor device 10(1). The device consists of a substrate 5 with a top layer 10b and a bottom layer 10a. A central region 11(11a) contains a grid of small rectangular elements. The device is surrounded by a frame 2a and 2b. Dimensions X1, X2, and X are indicated horizontally, and Y1 and Y2 are indicated vertically. A scale bar of 500 is shown. A label (PRと重なる範囲) points to a specific area within the grid.

This cross-sectional diagram illustrates a semiconductor device. It features a substrate 5 containing a first conductive layer 20a and a second conductive layer 20b. A gate stack 21 is positioned above the first conductive layer 20a, consisting of a gate insulating film 22 and a gate electrode 23b. A source/drain region 24a(24) is formed in the first conductive layer 20a, and a contact plug 24b(24) connects this region to a pad 23a. The entire structure is covered by a passivation layer 500. Dimensions X1, X2, and X are indicated horizontally, while Y1 and Y2 are indicated vertically.

11(11a)

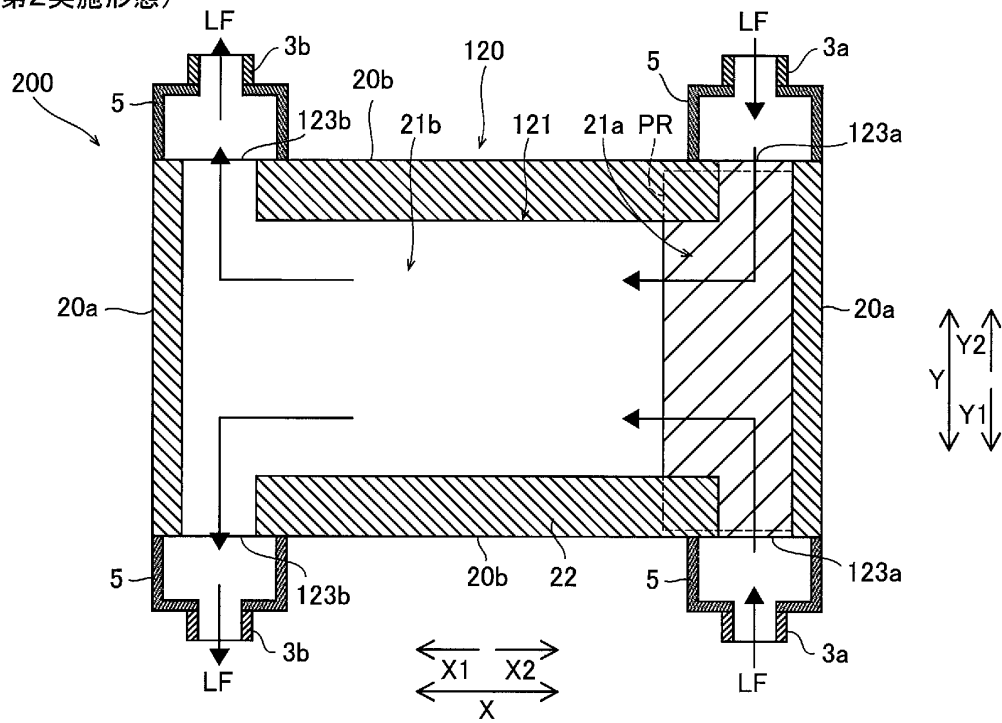
Diagram illustrating a plan view of a semiconductor device 11(11a). The device features a grid of rectangular elements 12 and 14. The elements 12 are arranged in a staggered pattern, while the elements 14 form the background. The pitch between the elements is denoted by p . The vertical dimensions are labeled $W1$ and $W2$, and the horizontal dimensions are labeled $L1$ and $W3$. A coordinate system with X and Y axes is shown.

[図7]



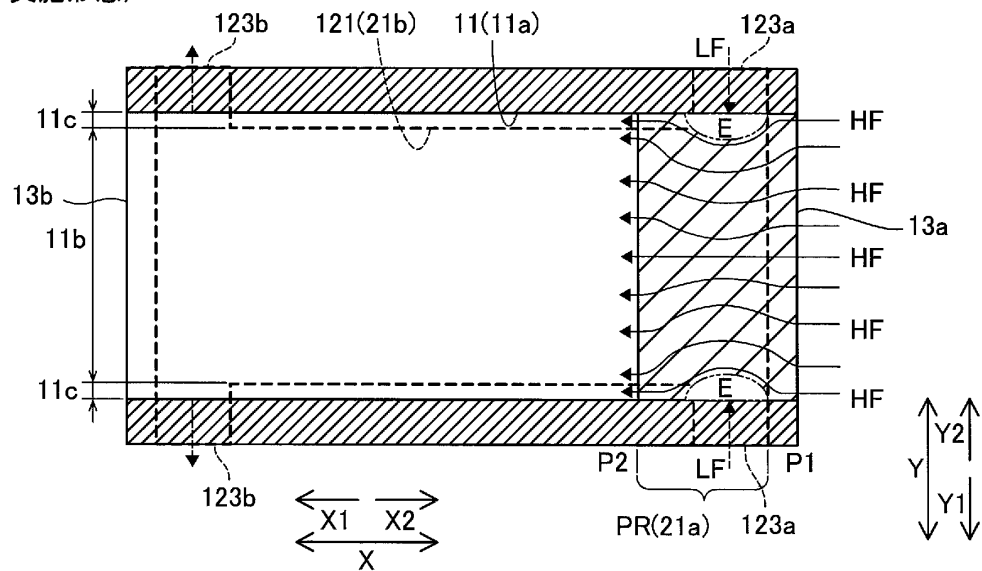
[図8]

(第2実施形態)

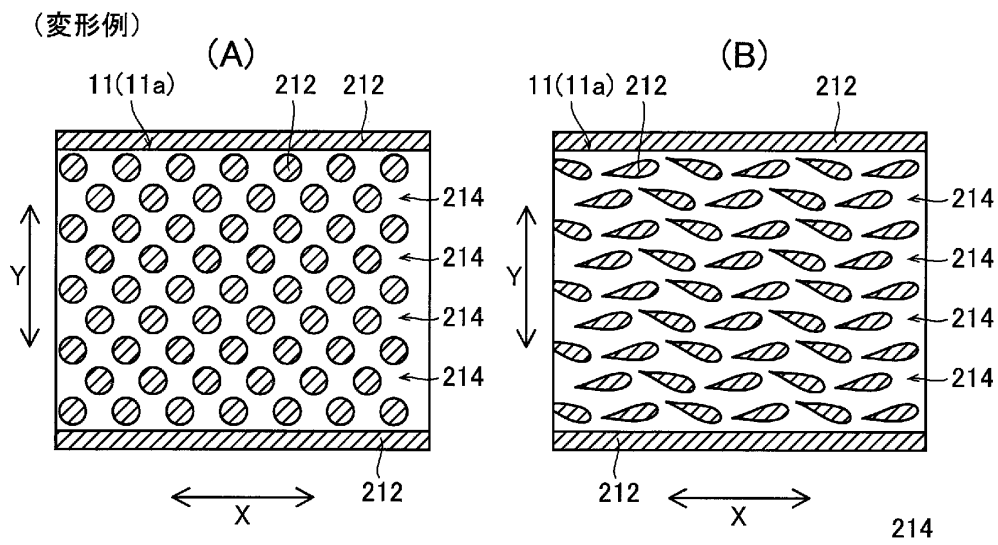


[図9]

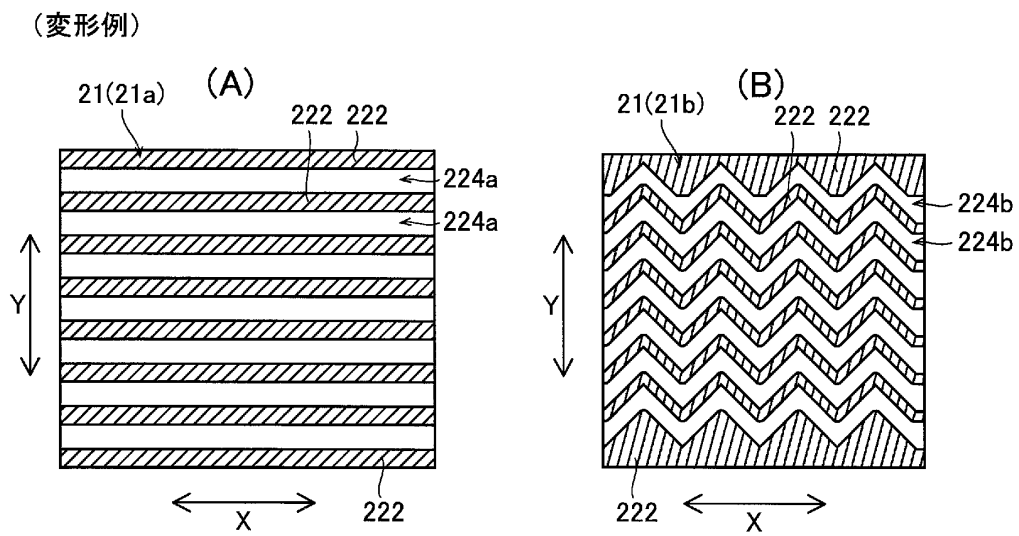
(第2実施形態)



[図10]



[図11]



[図12]

(変形例)

