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Differential Amplifier Circuit For Use In A Read Channel For A Magnetic Recording System

Related Application

This patent application is related to concurrently filed U. S. patent
5 application serial no. 08/534,524, entitled "A Read Channel For At Least Partially
Offsetting Nonlinear Signal Effects Associated With The Use Of Magneto-Resistive
Heads," filed September 27, 1995, by Sonntag, (Sonntag 11) herein incorporated by
reference and assigned to the assignee of the present invention.

Technical Field

10 The present invention is related to amplifier circuits, and more
particularly, to differential amplifier circuits.

Background of the Invention

Amplifiers, and, particularly, operational amplifiers and differential
amplifiers, are well-known in the art. Such amplifiers have a variety of applications,
15 such as described, for example, in Design of MOS VLSI Circuits for
Telecommunications, edited by Y. Tsividis and P. Antognetti, published by
Prentice-Hall, Inc. (1985), and herein incorporated by reference. Typically, it is
desirable to ensure that such differential amplifiers and operational amplifiers
operate linearly so that the output voltage signal is approximately an amplified
20 version of the applied input voltage signal. However, it is sometimes also desirable
to produce harmonic components of an applied voltage signal.

Summary of the Invention

Briefly, in accordance with one embodiment of the invention, a circuit
comprises: at least one differential amplifier. The differential amplifier is coupled in
25 a circuit configuration so that the differential output voltage signal of the differential
amplifier circuit includes a scalable second-order harmonic component of the
differential input voltage signal applied to the differential amplifier circuit. Briefly,
in accordance with another embodiment of the invention, a method of applying a
differential input voltage signal to a differential amplifier circuit to produce a
30 differential output voltage signal comprises the step of: driving the differential
amplifier circuit so that the differential output voltage signal of the differential
amplifier circuit includes a second-order harmonic component of the differential
input voltage signal.

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Brief Description of the Drawings

The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with features,
5 objects, and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanying drawings in which:

FIG. 1 is a circuit diagram illustrating an embodiment of a differential amplifier circuit in accordance with the invention

FIG. 2 is a block diagram illustrating an embodiment of a read channel
10 for a magnetic recording system coupled to a magneto-resistive (MR) read head that may employ an embodiment of a differential amplifier circuit in accordance with the invention.

FIG. 3 is a circuit diagram illustrating an alternative embodiment of a differential amplifier circuit in accordance with the invention.

FIG. 4 is a circuit diagram illustrating a portion of another embodiment
15 of a differential amplifier circuit in accordance with the invention.

FIG. 5 is a circuit diagram illustrating yet another embodiment of a differential amplifier circuit in accordance with the invention.

FIG. 6 is a circuit diagram illustrating still another embodiment of a
20 differential amplifier circuit in accordance with the invention.

Detailed Description

Magnetic recording systems, such as disk drives, for example, employ electronic circuits to read electro-magnetically stored signals, such as those stored on a disk or diskette, for example. Typically, such systems employ magnetic induction
25 to read the electro-magnetically stored signals, such as described, for example, in An Introduction To Direct Access Storage Devices, written by Hugh N. Sierra, published by Academic Press, Inc. (1990), and herein incorporated by reference. It has become increasingly popular to employ magneto-resistive (MR) read heads with such systems. One reason is because such read heads may provide improved signal-
30 to-noise (S/N) ratios in comparison with other conventional types of read heads that may be employed with such systems.

Aforementioned concurrently filed U.S. patent application serial no. 08/534,524, (Sonntag 11) describes an embodiment of a read channel, such as may be used in a magnetic recording system, for at least partially offsetting nonlinear
35 signal effects associated with the use of MR read heads. FIG. 2 illustrates a portion 1000 of an embodiment of a read channel described in that patent application. A MR

head or MR read head 2000 is also illustrated in FIG. 2. Likewise, a preamplifier 3000 is illustrated. Where preamplifier 3000 is relatively wideband, the transfer function for the preamplifier may be approximated as a scale factor and/or a substantially constant delay. Of course, it is understood that appropriate components
5 illustrated in the signal path are AC coupled in a manner so as to reduce or remove DC bias voltages.

As illustrated in FIG. 2, read channel 1000 includes a nonlinear adjustment 1100. Likewise nonlinear adjustment 1100 may be adapted so as to introduce a controllable amount of second-order nonlinearity into the magnetic
10 recording read channel signal path, as described in more detail in the aforementioned concurrently filed U.S. patent application serial no. 08/534,524 (Sonntag 11). In this particular embodiment illustrated in FIG. 2, nonlinear adjustment 1100 is illustrated as including compensating nonlinearity component 1115 in which the output signal provided by variable gain amplifier (VGA) 1135 is processed by compensating
15 nonlinearity element 1115 so as to produce a nonlinear output signal, $y(Av)$, such as a second-order harmonic component of the read channel voltage signal. Likewise, in this particular embodiment of a nonlinear adjustment, the output signal of VGA 1135 and the output signal of compensating nonlinearity element 1115 are then superpositioned at a summing node, such as node 1130 illustrated in FIG. 2.

20 Although FIG. 2 illustrates a block diagram embodiment of nonlinear adjustment 1100, it would be convenient if a circuit configuration implemented compensating nonlinearity element 1115 and summing node 1130. Furthermore, it would be convenient if this circuit configuration could be configured using conventional amplifiers or similar electronic circuitry.

25 FIG. 1 illustrates an embodiment 250 of a differential amplifier circuit in accordance with the invention that may be employed to provide the desired nonlinear adjustment. As illustrated in FIG. 1, embodiment 250 comprises a conventional differential amplifier 900. Likewise, conventional MOS transistors are illustrated, such as transistors 910, 920, 930, and 940. Although not explicitly illustrated, either
30 P-channel or N-channel MOS transistors will suffice. For the configuration illustrated in FIG. 1, the control voltage, V_c , may be of a sufficiently high magnitude to ensure that MOS transistors 910, 920, 930 and 940 remain substantially triode-biased, although the invention is not limited in scope in this respect, as explained in more detail hereinafter. As is well-known, by operating in the triode region,
35 operationally the MOS transistors resemble resistors. See, for example, "Continuous-Time MOSFET-C Filters In VLSI," by Tsividis et al., IEEE

Transactions On Circuits And Systems, Volume CAS-33, No. 2, February, 1986, herein incorporated by reference.

As illustrated in FIG. 1, in this particular embodiment, gamma (γ) may be employed to scale or control the amount of common mode (CM) feedback provided to differential amplifier 900. Thus, the relationship between V_{cmfb} , V_{op} and V_{on} may be described by the following equation.

$$V_{cmfb} = \gamma V_{op} + (1-\gamma) V_{on} = V_{cref} \quad (1)$$

where V_{cref} is the common mode reference voltage level in this particular embodiment. Based on the configuration illustrated in FIG. 1, differential amplifier 975 operates in conjunction with differential amplifier 900 in a manner to maintain V_{cmfb} substantially equal to V_{cref} . This relationship therefore provides the following equation.

$$0.5(V_{op} + V_{on}) = V_{cref} + (0.5-\gamma) (V_{op} - V_{on}) \quad (2)$$

Therefore, as will be explained in more detail hereinafter, the actual common mode output voltage signal of amplifier 900 includes a scalable fraction of the differential output voltage signal of amplifier 900. The fraction of the differential output voltage signal of amplifier 900 included in its common mode output voltage signal depends on the value of γ , in accordance with the configuration illustrated. Furthermore, in this particular embodiment, the output voltage signal of amplifier 900 comprises the output voltage signal of the differential amplifier circuit.

Because the actual common mode output voltage signal of amplifier 900 includes a scalable fraction of the differential output voltage signal of amplifier 900, the differential output voltage signal of amplifier 900, which in this embodiment is the differential output voltage signal of the differential amplifier circuit, includes a second-order harmonic component of the differential input voltage signal applied to the differential amplifier circuit, $V_{ip} - V_{in}$ in this particular embodiment, as will be explained in more detail hereinafter. Furthermore, the magnitude of this second-order harmonic component is adjustable or controllable. For example, adjusting γ and/or adjusting the magnitude of V_c will adjust the magnitude as desired, as also will be explained in more detail hereinafter.

FIG. 5 illustrates an embodiment 270 of a differential amplifier circuit in accordance with the invention in which a scalable fraction of the differential input voltage signal applied to the differential amplifier circuit is applied to amplifier 675 in a manner so as to drive the common mode output voltage signal of differential amplifier 600 to include a scalable fraction of the differential input voltage signal. As illustrated, the output voltage signal of amplifier 675 is applied as the common mode feedback voltage signal of amplifier 600. In this particular embodiment, the common mode feedback voltage signal and the common mode output voltage signal of amplifier 600 respectively comprise the common mode feedback voltage signal and the common mode output voltage signal of the differential amplifier circuit. This is similar in some respects to the approach employed in FIG. 1 and is employed here to simplify the mathematical analysis for purposes of illustration.

For the embodiment illustrated in FIG. 5, the current in a triode-biased device, such as MOS transistors 610, 620, 630, and 640, may be written as

$$I_{DS} = \kappa \left[V_G - V_{TH} - \frac{V_D + V_S}{2} \right] V_{DS} \quad (3)$$

where I_{DS} is the drain-to-source current, V_G is the gate voltage, V_{TH} is the threshold voltage, V_D is the drain voltage, V_S is the source voltage, V_{DS} is the drain-to-source voltage and κ is a known value that may vary based, at least in part, upon temperature and device geometry.

Employing the conventional assumption of a substantially ideal amplifier, the drain-to-source current of transistor 640 should approximately equal the drain-to-source current of transistor 610 and, likewise, the drain-to-source current of transistor 630 should approximately equal the drain-to-source current of transistor 620. Utilizing these equalities and equation (3) above results in two equations that may be subtracted to yield the following result.

$$V_{ID} (V_c - V_{TH} - V_{IC}) = V_{OD} (V_c - V_{TH} - V_{OC}) \quad (4)$$

or

$$V_{OD} = V_{ID} \left[\frac{V_c - V_{TH} - V_{IC}}{V_c - V_{TH} - V_{OC}} \right] \quad (4a)$$

where V_{ID} is the differential input voltage, V_{IC} is the common mode input voltage,

V_{OD} is the differential output voltage and V_{OC} is the common mode output voltage.
For the embodiment illustrated in FIG. 5,

$$\begin{aligned} V_{IC} &= V_{cref} \\ V_{OC} &= V_{cref} + (\gamma - 0.5) V_{ID} \end{aligned} \quad (5)$$

Inserting equation (5) for V_{OC} into equation (4a) and letting $V_c' = V_c - V_{TH} - V_{cref}$ results in

$$V_{OD} = V_{ID} \cdot 1 / \left[1 - \frac{(\gamma - 0.5) V_{ID}}{V_c'} \right] \quad (5a)$$

10 which, for relatively small values of $\frac{(\gamma - 0.5) V_{ID}}{V_c'}$, may be approximated as

$$\approx V_{ID} \left[1 + \frac{(\gamma - 0.5) V_{ID}}{V_c'} \right] \quad (5b)$$

$$= V_{ID} + V_{ID}^2 \left[\frac{(\gamma - 0.5)}{V_c - V_{TH} - V_{cref}} \right] \quad (5c)$$

15 Employing these mathematical manipulations, therefore, yields the following equation for the differential output voltage signal.

$$V_{OD} \approx V_{ID} + \left[\frac{\gamma - 0.5}{V_c - V_{TH} - V_{cref}} \right] V_{ID}^2 \quad (6)$$

20 Equation (6) above illustrates that, for the embodiment illustrated in FIG. 5, the magnitude of the second-order harmonic component of the differential input voltage signal applied to the differential amplifier circuit that may be introduced into the differential output voltage signal may be adjusted by adjusting γ and/or by adjusting V_c .

25 The equations above were obtained by driving the differential amplifier circuit so that a fraction of the differential input voltage signal applied to the differential amplifier circuit is included as the common mode of the output voltage signal of the differential amplifier circuit. The common mode feedback voltage signal in this particular embodiment provides a mechanism to accomplish this, as

illustrated in FIG. 5. However, as previously indicated, alternatively, the common mode feedback voltage signal may be obtained by using the differential output voltage signal, such as for the embodiment illustrated in FIG. 1. It may, likewise, be demonstrated that this approach will produce a result similar to equation (6) above.

5 One advantage of the FIG. 5 embodiment over the FIG. 1 embodiment, however, is that the FIG. 5 embodiment provides more bandwidth. This is due, at least in part, to the use of the differential input voltage signal applied to the differential amplifier circuit, such as illustrated in FIG. 5, instead of using the differential output voltage signal, such as illustrated in FIG. 1. Less delay occurs in the FIG. 5 embodiment, for
10 example. This reduction in delay, therefore, increases the bandwidth of the embodiment of a differential amplifier circuit in accordance with the invention.

FIG. 3 illustrates yet another alternative embodiment 500 of a differential amplifier circuit in accordance with the invention. In FIG. 3, embodiment 500 is illustrated as embodied in or on an integrated circuit, although
15 the invention is not limited in scope in this respect. The approach employed in this particular embodiment is similar to the approach employed in the embodiment shown in FIG. 5 in that a fraction of the differential input voltage signal applied to the differential amplifier circuit is added to the common mode of the output voltage signal of a differential amplifier via the common mode feedback voltage signal.
20 However, whereas for the embodiment illustrated in FIG. 5 the common mode feedback voltage signal was applied to a differential amplifier employed in a triode-biased circuit configuration, e.g., with the differential amplifier coupled to MOS transistors biased to operate in their triode region, such as differential amplifier 600 in FIG. 5, in contrast, for embodiment 500 of a differential amplifier circuit in
25 accordance with the invention illustrated in FIG. 3, the embodiment comprises a linear amplifier circuit portion 540 and a triode-biased amplifier circuit portion 550. In fact, in this particular embodiment, the triode-biased amplifier circuit portion 550 comprises a conventional MOSFET-C circuit including a differential amplifier, where the conventional feedback capacitors for the MOSFET-C circuit are replaced
30 with triode-biased MOS transistors 515 and 525. Likewise, although not explicitly illustrated in FIG. 3, differential amplifier 520 is assumed to include conventional common mode feedback circuitry.

Whereas previously, such as illustrated in FIG. 5, the common mode feedback voltage signal was applied to a differential amplifier coupled in a triode-biased amplifier circuit configuration, instead for the embodiment illustrated in FIG.
35 3, the common mode feedback voltage signal is applied to differential amplifier 510,

which is coupled in a linear amplifier circuit configuration at least in part. For example, in this particular embodiment, linear amplifier configuration 540 includes impedances 560, 570, 580, and 590. Depending upon the particular implementation, these impedances may comprise, for example, resistances, capacitances, or combinations thereof. Likewise, this particular linear amplifier circuit configuration employs the approach illustrated by the embodiment of FIG. 5 in which a fraction of the differential input voltage signal applied to the differential amplifier circuit is added to the common mode of the output voltage signal of the differential amplifier via the common mode feedback voltage signal of the differential amplifier; however, in this particular embodiment, the output voltage signal is the output voltage signal of differential amplifier 510, not a differential amplifier employed in a triode-based amplifier circuit configuration, such as differential amplifier 600 in FIG. 5, and the common mode feedback voltage signal is the common mode feedback voltage signal of differential amplifier 510.

When this particular configuration is employed, the common mode output voltage signal of differential amplifier 510 may be given by the following equation.

$$V_{OC} = V_{cref} + (\gamma - 0.5) V_{ID} \quad (7)$$

where V_{ID} is the differential input voltage signal applied to embodiment 500 of a differential amplifier circuit in accordance with the invention.

However, as illustrated by the embodiment shown in FIG. 3, the inverting and noninverting output voltage signals of differential amplifier 510 are likewise applied to triode-biased amplifier circuit configuration 550. Due to equation (7) above, the common mode input voltage signal of triode-based amplifier circuit configuration 550 may be given by the following equation.

$$V_{IC} = V_{cref} + (\gamma - 0.5) V_{ID} \quad (8)$$

Thus, by this technique the differential output voltage signal of a differential amplifier circuit, which in this particular embodiment is the output voltage signal of amplifier 520, includes a scalable second-order harmonic component of the differential input voltage signal applied to the differential amplifier circuit, as desired. It will now be appreciated by one of ordinary skill in the art that the approach employed in the embodiment illustrated in FIG. 1 may, likewise, be

adapted for an embodiment of a differential amplifier in accordance with the invention including a linear amplifier circuit portion and a triode-biased amplifier circuit portion. In one such embodiment, for example, the common mode input voltage signal of a first differential amplifier in the triode-biased amplifier circuit portion may include an adjustable fraction of the differential output voltage signal of a second differential amplifier in the linear amplifier circuit portion.

FIG. 4 is a circuit diagram illustrating a portion of another embodiment of a differential amplifier circuit in accordance with the invention. As illustrated in FIG. 4, the differential input voltage signal of a differential amplifier circuit may be provided to a resistor network that may include series and/or parallel switches in the form of MOS transistors. For example, for the network illustrated, the output signal produced by this particular network, V_{COM} , may be provided to a differential amplifier, such as amplifier 675 illustrated in FIG. 5, and thereby provide a common mode feedback voltage signal, similar to the approach employed in connection with the embodiment illustrated in FIG. 5. Where this configuration is employed, MOS transistors, such as 710, 720, 730 and 740, may be actuated in response to externally-derived voltage signals applied to their respective gates to adjust the magnitude of the second-order harmonic signal produced by the differential amplifier circuit. Likewise, other configurations in which the magnitude of the second-order harmonic component signal produced may be digitally-controlled may be configured.

It will, of course, be appreciated that a differential amplifier circuit in accordance with the present invention is not limited in scope to the particular embodiments illustrated. For example, in an embodiment in which V_c is used to control or adjust the magnitude of the second-order harmonic component of the differential input voltage signal applied to the differential amplifier circuit, any one of a number of schemes may be employed to adjust V_c . For example, in an embodiment in which binary digital signals are employed, such as described in aforementioned concurrently filed U. S. patent application serial no. 08/534,524 (Sonntag 11), the binary digital signals may be integrated or summed to provide a digital signal control and this digital signal control may be provided to a digital-to-analog converter (DAC) to provide an analog signal for V_c . Furthermore, the invention is not restricted in scope to employing either γ or V_c to scale the second-order harmonic component of the differential input voltage signal. These and other parameters may be adjusted individually or in combination, depending on the particular embodiment. For example, in one embodiment of a differential amplifier

circuit in accordance with the invention, γ may be employed to provide a coarse adjustment and V_c may be employed to provide a fine adjustment to scale the second-order harmonic component. More specifically, a differential amplifier circuit in accordance with the invention may be employed, for example, in an embodiment of a read channel as described in aforementioned concurrently filed patent application serial no. 08/534,524, (Sonntag 11). For example, in such a read channel, V_c may be adjustable adaptively under closed loop control so as to provide real-time fine adjustment, whereas γ may be adjustable, for example, based on externally-derived signals, such as described, for example, in connection with FIG. 4. For example, the coarse adjustment may be programmable, although, of course, the invention is not restricted in scope to this particular approach.

Likewise, in an alternative embodiment, the gain of the differential amplifier in a differential amplifier circuit in accordance with the invention may be adjusted to scale the second-order harmonic component of the differential input voltage signal. For example, referring to embodiment 400 illustrated in FIG. 6, again a triode-biased amplifier circuit configuration may be employed, such as differential amplifier 410 and MOS transistors 420, 430, 440 and 450 coupled in the configuration illustrated. In this particular embodiment, although not explicitly illustrated, differential amplifier 410 is assumed to include conventional common mode feedback circuitry. It may be demonstrated that for this differential amplifier circuit configuration, the gain may be given by the following equation.

$$\text{Gain} = \frac{V'_{c1}}{V'_{c2}} \quad (9)$$

where the V'_{c1} and V'_{c2} are given by the following equations,

$$\begin{aligned} V'_{c1} &= V_{c1} - V_{TH} - V_{\text{common}} \\ V'_{c2} &= V_{c2} - V_{TH} - V_{\text{common}} \end{aligned} \quad (10)$$

where V_{TH} is the threshold voltage and V_{common} is the common mode voltage. As illustrated by the embodiment of FIG. 6, V_{c1} is given by the following equation.

$$V_{c1} = V_{c2} + \gamma V_{ID} \quad (11)$$

where

$$V_{ID} = V_{ip} - V_{in}$$

Applying equations (10) and (11) to equation (9) gives the following expression for the gain.

$$\text{Gain} = \frac{V'_{c2}}{V'_{c1}} \approx \frac{V_{c2} + \gamma V_{ID}}{V_{c2}} = 1 + \frac{\gamma}{V_{c2}} V_{ID} \quad (12)$$

- 5 Thus, for embodiment 400 of a differential amplifier circuit in accordance with the invention,

$$V_{out} = V_{in} \left[1 + \frac{\gamma}{V_{c2}} V_{in} \right] \quad (13)$$

- indicating that the gain is adjustable at least in part in accordance with control
10 voltage V_{c2} .

A differential amplifier circuit in accordance with the invention, such as embodiments 250 and 270, for example, may be driven to generate a second-order harmonic component of a differential input voltage signal applied to the differential amplifier circuit. Likewise, its differential amplifier circuit may be driven so that the
15 differential input voltage signal includes a scaled fraction of the second-order harmonic component. A differential amplifier, such as differential amplifiers 900 or 600 as previously described, for example, may driven in a manner so that the common mode output voltage signal includes a fraction of the differential output voltage signal of the differential amplifier circuit or includes a fraction of the
20 differential input voltage signal applied to the differential amplifier circuit, respectively. Likewise, the common mode output voltage signal of the differential amplifier may be driven so as to include a scaled fraction of the differential output voltage signal of the differential amplifier circuit or the differential input voltage signal applied to the differential amplifier circuit. Furthermore, the common mode
25 input voltage signal of a differential amplifier may be driven so as to include a scaled fraction of the differential output voltage signal of another differential amplifier, or a scaled fraction of the differential input voltage signal applied to the differential amplifier circuit, such as illustrated in FIG. 3, for example. In such embodiments, a second-order harmonic component of the differential input voltage signal in the
30 differential output voltage signal of the differential amplifier circuit may be adjusted or scaled by a variety of techniques such as by adjusting relative resistances, adjusting control voltages, adjusting amplifier gain, or combinations thereof, as

previously described. For example, where one of the previous techniques is employed to provide a coarse adjustment to the amplitude of the second-order harmonic component generated, such as by adjusting the fraction of the differential input voltage signal based on relative resistor values, for example, a fine adjustment
5 of scaling may occur by driving selected controlling gate voltages for the MOS transistors of the circuit configuration. For the embodiments illustrated in FIGs. 1 and 5, respectively, for example, the controlling gate voltages for transistors 610, 620, 630 and 640 or for transistors 910, 920, 930 and 940 may be driven, as previously described. Further, alternatively, the gain of the differential amplifier
10 may be adjusted to scale the amplitude of the second-order harmonic component of the differential input voltage signal applied to the differential amplifier, such as described in connection with the embodiment illustrated in FIG. 6. For example, selected controlling gate voltages may be driven in a manner to include a scaled fraction of the differential input voltage signal.

15 While only certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes or equivalents will now occur to those skilled in the art.

Claims:

1. An integrated circuit comprising:
at least one differential amplifier (900);
said differential amplifier being coupled in a differential amplifier
5 circuit configuration so that the differential output voltage signal of said differential
amplifier circuit configuration includes a scalable second-order harmonic component
of the differential input voltage signal applied to said differential amplifier circuit.
2. The integrated circuit of claim 1,
wherein said differential amplifier includes a common mode output
10 voltage signal (V_{cmfb});
said common mode output voltage signal including an adjustable
fraction (γ) of said differential output voltage signal.
3. The integrated circuit of claim 2,
wherein said differential amplifier includes an inverting and
15 noninverting output voltage signal (V_{on} , V_{op}), and a common mode feedback
voltage signal;
the circuit configuration being coupled so that adjusting the relative
imbalance between said inverting and noninverting output voltage signals in said
common mode feedback voltage signal adjusts the fraction of said differential output
20 voltage signal included in said common mode output voltage signal.
4. The integrated circuit of claim 2,
wherein said differential amplifier includes respective, inverting and
noninverting, input and output voltage signal ports;
a first MOS transistor (940) being coupled to the noninverting input
25 voltage signal port, a second MOS transistor (930) being coupled to the inverting
input voltage signal port, a third MOS transistor (920) coupling the inverting input
voltage signal port to the noninverting output voltage signal port, and a fourth MOS
transistor (910) coupling the noninverting input voltage signal port to the inverting
output voltage signal port.
- 30 5. The integrated circuit of claim 4,



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wherein said differential amplifier includes an inverting and noninverting input voltage signal (V_{in} , V_{ip}), and a common mode feedback voltage signal;

5 the circuit configuration being coupled (FIG. 3) so that adjusting the relative imbalance between said inverting and noninverting input voltage signals in said common mode feedback voltage signal adjusts the fraction of said differential input voltage signal included in said common mode output voltage signal.

6. The integrated circuit of claim 4,

10 wherein said differential amplifier includes respective, inverting and noninverting, input and output voltage signal ports;

a first MOS transistor (640) being coupled to the noninverting input voltage signal port, a second MOS transistor (630) being coupled to the inverting input voltage signal port, a third MOS transistor (620) coupling the inverting input voltage signal port to the noninverting output voltage signal port, and a fourth MOS
15 transistor (610) coupling the noninverting input voltage signal port to the inverting output voltage signal port.

7. The integrated circuit of claim 1,

20 wherein said differential amplifier includes a common mode input voltage signal; said common mode input voltage signal including an adjustable fraction of said differential input voltage signal.

8. The integrated circuit of claim 1,

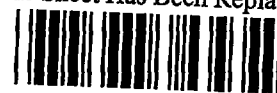
25 wherein said differential amplifier circuit configuration (FIG. 5) comprises a first differential amplifier (600) including a common mode input voltage signal;

said differential amplifier circuit configuration further comprising a second differential amplifier (675) including a differential output voltage signal (Common Mode Feedback);

30 said first and second differential amplifiers being coupled in the circuit configuration so that the common mode input voltage signal of said first differential amplifier includes an adjustable fraction (γ) of the differential output voltage signal of said second differential amplifier.



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9. The integrated circuit of claim 1,

wherein said differential amplifier (410) includes respective, inverting and noninverting, input and output voltage signal ports and a common mode output voltage signal;

5 a first MOS transistor (640) being coupled to the noninverting input voltage signal port, a second MOS transistor (630) being coupled to the inverting input voltage signal port, a third MOS transistor (620) coupling the inverting input voltage signal port to the noninverting output voltage signal port, and a fourth MOS transistor (610) coupling the noninverting input voltage signal port to the inverting
10 output voltage signal port;

each of said MOS transistors including a controlling gate voltage;

said differential amplifier being coupled in the circuit configuration so that said common mode output voltage signal includes an adjustable fraction (γ) of one of said differential input voltage signal and said differential output voltage
15 signal;

the circuit configuration being adapted (FIG. 5) to apply the controlling gate voltages to said MOS transistors in a manner so that adjusting the controlling gate voltages scales the amplitude of the second-order harmonic component of said differential input voltage signal included in said differential output voltage signal.

20 10. The integrated circuit of claim 1,

wherein said differential amplifier includes respective, inverting and noninverting, input and output voltage signal ports;

a first MOS transistor (440) being coupled to the noninverting input voltage signal port, a second MOS transistor (430) being coupled to the inverting
25 input voltage signal port, a third MOS transistor (420) coupling the inverting input voltage signal port to the noninverting output voltage signal port, and a fourth MOS transistor (450) coupling the noninverting input voltage signal port to the inverting output voltage signal port;

said differential amplifier being coupled in the circuit configuration
30 (FIG. 6) so that adjusting the gain of said differential amplifier scales the amplitude of the second-order harmonic component of said differential input voltage signal included in said differential output voltage signal.

11. The integrated circuit of claim 10,

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wherein each of said MOS transistors includes a controlling gate voltage;

said differential amplifier being further coupled in the circuit configuration so that adjusting the controlling gate voltage (V_{c2}) of the third and
5 fourth MOS transistors scales the amplitude of the second-order harmonic component of said differential input voltage signal included in said differential output voltage signal.

12. A method of applying a differential input voltage signal applied to a differential amplifier circuit to produce a differential output voltage signal
10 comprising the step of:

driving said differential amplifier circuit so that said differential output voltage signal of said differential amplifier circuit includes a second-order harmonic component of said differential input voltage signal.

13. The method of claim 12,
15 wherein the step of driving comprises driving said differential amplifier circuit so that said differential output voltage signal of said differential amplifier circuit includes a scaled fraction of the second-order harmonic component.

14. The method of claim 13,
wherein said differential amplifier circuit includes a differential
20 amplifier including a common mode output voltage signal;
the step of driving said differential amplifier circuit comprises driving the common mode output voltage signal of said differential amplifier in a manner so as to include a scaled fraction of said differential output voltage signal.

said differential amplifier being coupled in a triode-biased circuit
25 configuration including a plurality of MOS transistors coupled to said differential amplifier;

15. The method of claim 13,
wherein said differential amplifier circuit includes a differential
amplifier including a common mode output voltage signal;
30 said differential amplifier being coupled in a triode-biased circuit configuration including a plurality of MOS transistors coupled to said differential amplifier;



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the step of driving said differential amplifier circuit comprises driving the common mode output voltage signal of said differential amplifier in a manner so as to include a scaled fraction of said differential input voltage signal.

16. The method of claim 13,

5 wherein said differential amplifier circuit includes a differential amplifier including a common mode input voltage signal;

said differential amplifier being coupled in a triode-biased circuit configuration including a plurality of MOS transistors coupled to said differential amplifier;

10 the step of driving said differential amplifier circuit comprises driving the common mode input voltage signal of said differential amplifier in a manner so as to include a scaled fraction of said differential input voltage signal.

17. The method of claim 13,

15 wherein said differential amplifier circuit includes a first differential amplifier including a common mode input voltage signal and a second differential amplifier including a differential output voltage signal;

said first differential amplifier being coupled in a triode-biased circuit configuration including a plurality of MOS transistors coupled to said first differential amplifier;

20 the step of driving said differential amplifier circuit comprises driving the common mode input voltage signal of said first differential amplifier in a manner so as to include a scaled fraction of the differential output voltage signal of said second differential amplifier.

18. The method of claim 13,

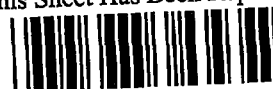
25 wherein said differential amplifier circuit includes a differential amplifier coupled in a triode-biased circuit configuration including a plurality of MOS transistors coupled to said differential amplifier, each MOS transistor in said plurality including a controlling gate voltage;

30 said differential amplifier including a common mode output voltage signal;

said differential amplifier being coupled in said circuit configuration so that the common mode output voltage signal of said differential amplifier includes an adjustable fraction of one of said differential input voltage signal and said



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differential output voltage signal;

wherein the step of driving comprises driving selected controlling gate voltages of said MOS transistors so as to scale the fraction of the second-order harmonic component.

5 19. The method of claim 13,

wherein said differential amplifier circuit includes a differential amplifier coupled in a triode-biased circuit configuration including a plurality of MOS transistors coupled to said differential amplifier, each MOS transistor in said plurality including a controlling gate voltage;

10 the driving step comprising driving selected controlling gate voltages to include a scaled fraction of said differential input voltage signal.

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* C L M S *

**Differential Amplifier Circuit For Use In A
Read Channel For A Magnetic Recording System**

Abstract

Briefly, in accordance with one embodiment of the invention, a circuit
5 comprises: at least one differential amplifier (900). The differential amplifier is
coupled in a circuit configuration so that the differential output voltage signal of the
differential amplifier circuit includes a scalable second-order harmonic component of
the differential input voltage signal applied to the differential amplifier circuit.
Briefly, in accordance with another embodiment of the invention, a method of
10 applying a differential input voltage signal to a differential amplifier circuit to
produce a differential output voltage signal comprises the step of: driving the
differential amplifier circuit so that the differential output voltage signal of the
differential amplifier circuit includes a second-order harmonic component of the
differential input voltage signal.

FIG. 1

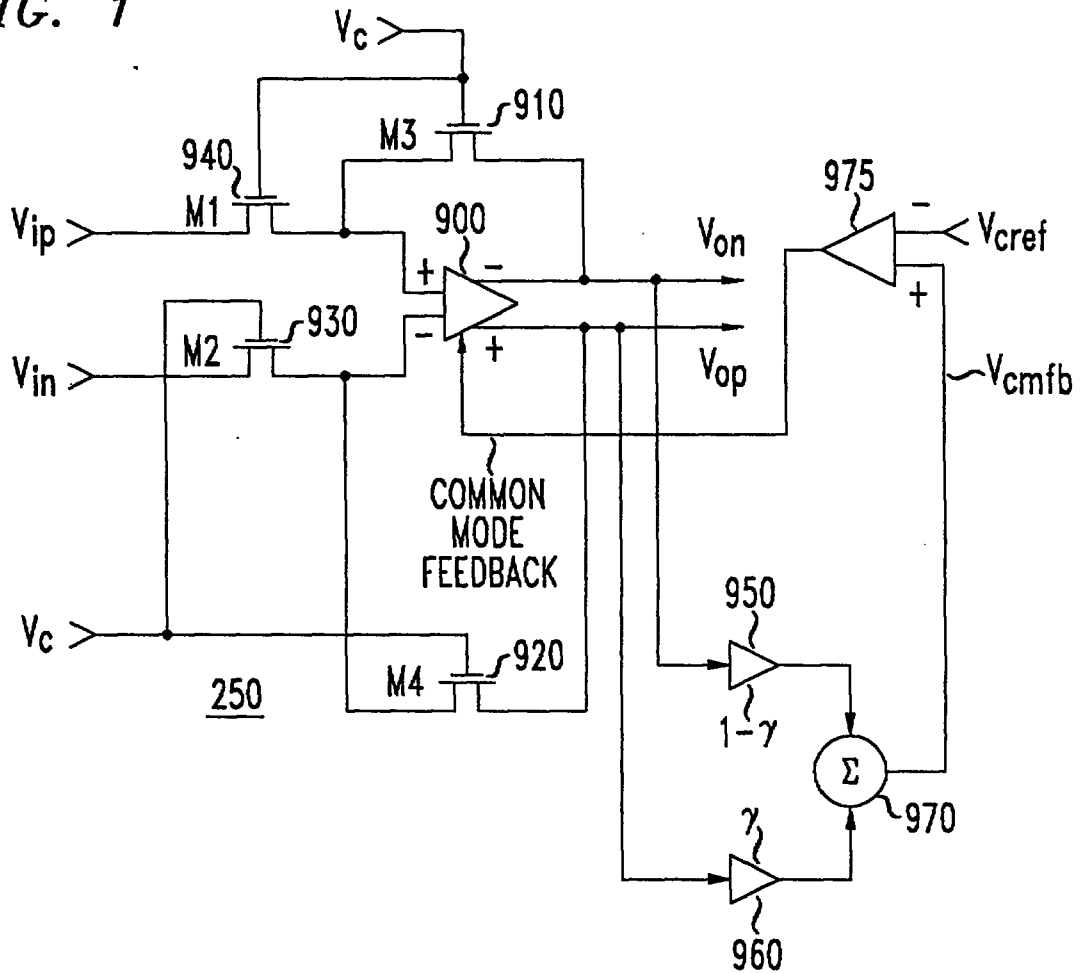
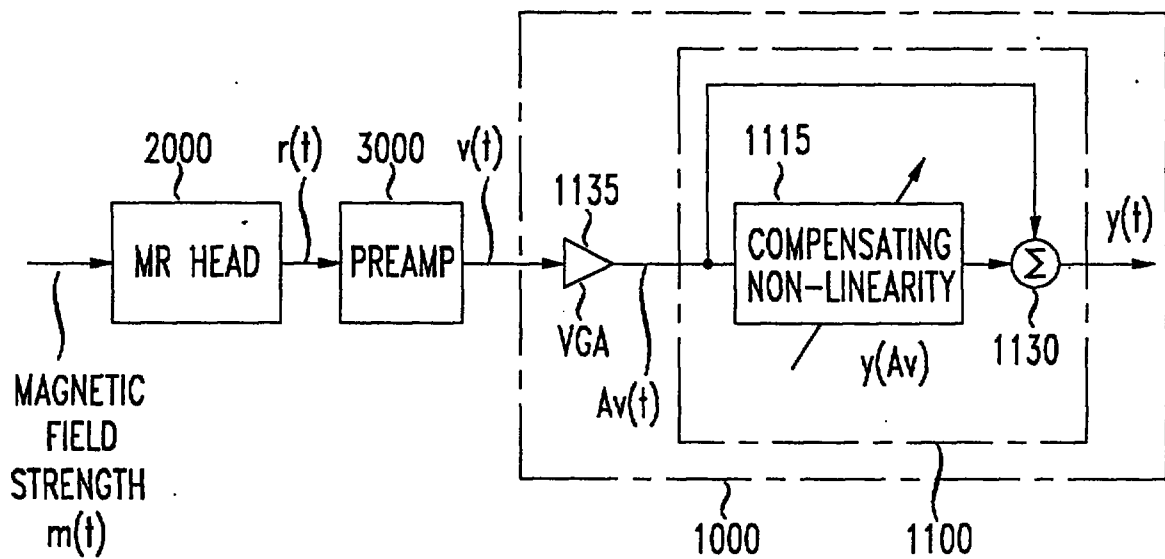


FIG. 2



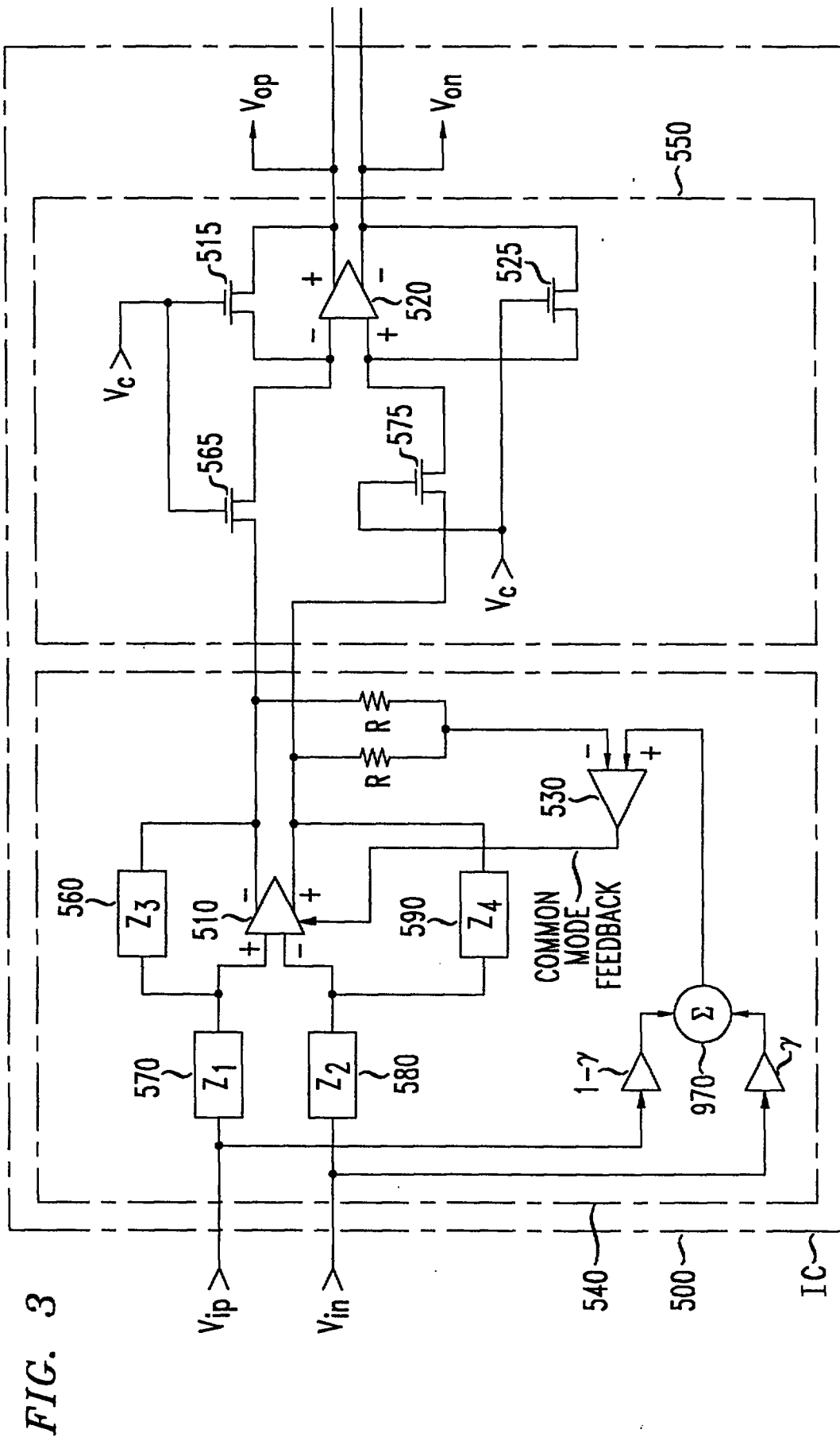


FIG. 4

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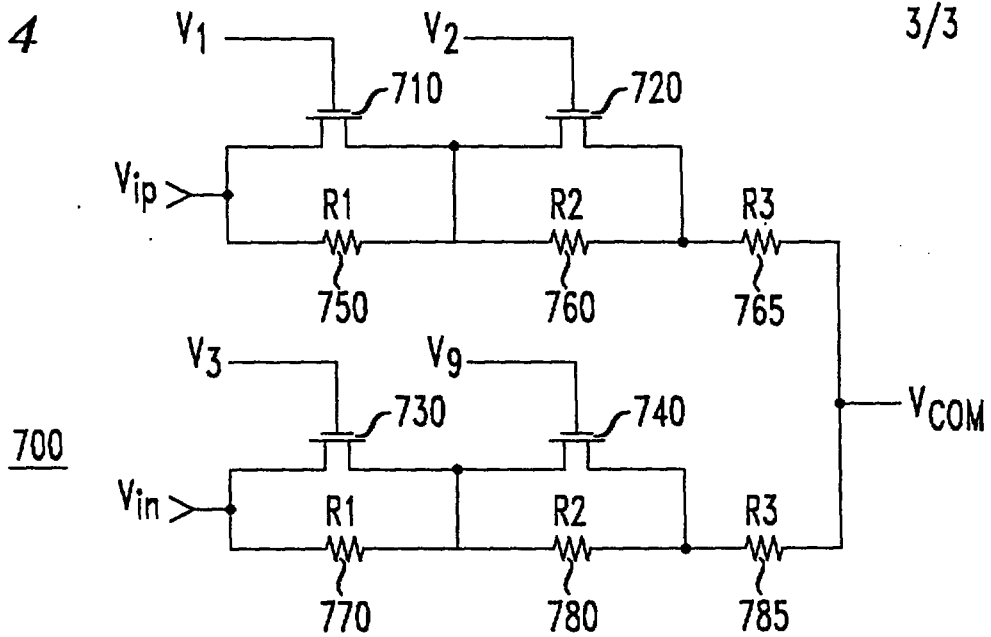


FIG. 5

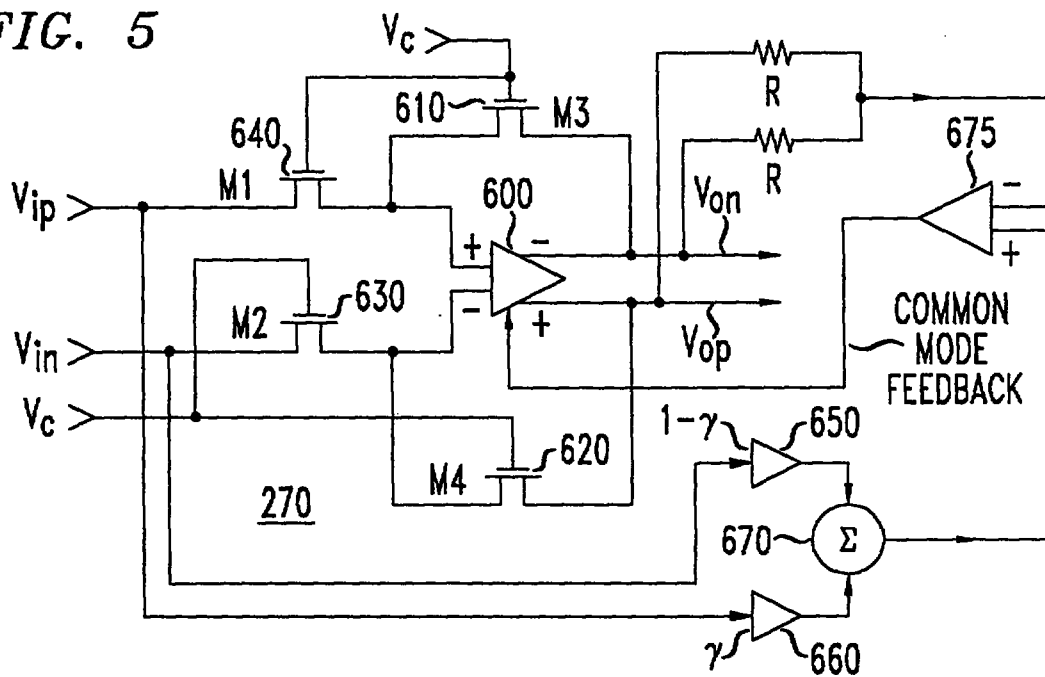
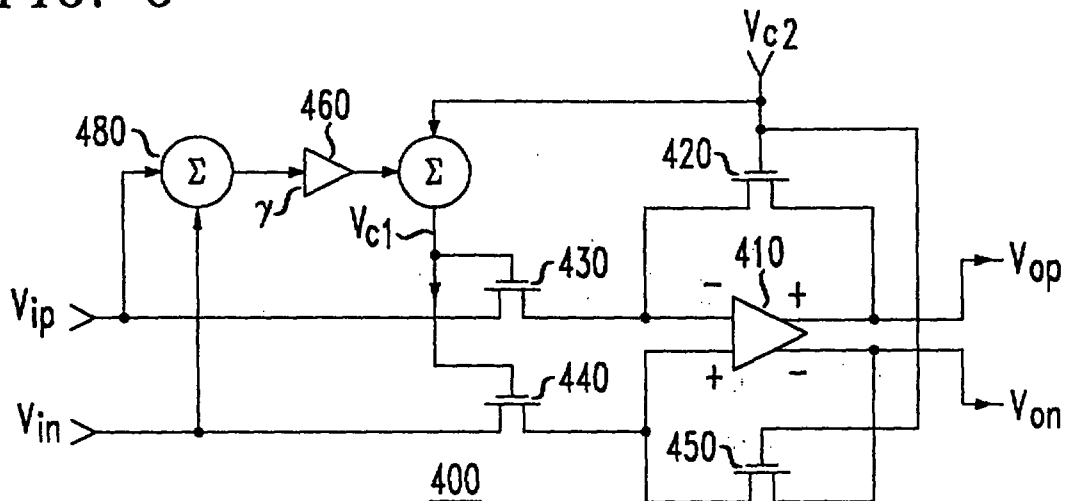


FIG. 6



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REPLACEMENT SHEETS		SG
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Claims:

1. An integrated circuit comprising:
at least one differential amplifier (900);
said differential amplifier being coupled in a differential amplifier
5 circuit configuration so that the differential output voltage signal of said differential
amplifier circuit configuration includes a scaleable second-order harmonic
component of the differential input voltage signal applied to said differential
amplifier circuit.
2. The integrated circuit of claim 1,
10 wherein said differential amplifier includes a common mode output
voltage signal (V_{cmfb});
said common mode output voltage signal including an adjustable
fraction (γ) of said differential output voltage signal.
3. The integrated circuit of claim 2,
15 wherein said differential amplifier includes an inverting and
noninverting output voltage signal (V_{on} , V_{op}), and a common mode feedback
voltage signal;
the circuit configuration being coupled so that adjusting the relative
imbalance between said inverting and noninverting output voltage signals in said
20 common mode feedback voltage signal adjusts the fraction of said differential output
voltage signal included in said common mode output voltage signal.
4. The integrated circuit of claim 2,
wherein said differential amplifier includes respective, inverting and
noninverting, input and output voltage signal ports;
25 a first MOS transistor (940) being coupled to the noninverting input
voltage signal port, a second MOS transistor (930) being coupled to the inverting
input voltage signal port, a third MOS transistor (920) coupling the inverting input
voltage signal port to the noninverting output voltage signal port, and a fourth MOS
transistor (910) coupling the noninverting input voltage signal port to the inverting
30 output voltage signal port.
5. The integrated circuit of claim 4,



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wherein said differential amplifier includes an inverting and noninverting input voltage (V_{in} , V_{ip}), and a common mode feedback voltage signal; the circuit configuration being coupled so that adjusting the relative imbalance between said inverting and noninverting input voltage signals in said
5 common mode feedback voltage signal adjusts the magnitude of said differential input voltage signal included in said common mode output voltage signal.

6. The integrated circuit of claim 1,
wherein said differential amplifier includes a common mode input voltage signal;
10 said common mode input voltage signal including an adjustable fraction of said differential input voltage signal.

7. The integrated circuit of claim 1,
wherein said differential amplifier circuit configuration comprises a first differential amplifier (600) including a common mode input voltage signal;
15 said differential amplifier circuit configuration further comprising a second differential amplifier (675) including a differential output voltage signal (Common Mode Feedback);
said first and second differential amplifiers being coupled in the circuit configuration so that the common mode input voltage signal of said first differential
20 amplifier includes an adjustable fraction (γ) of the differential output voltage signal of said second differential amplifier.

8. The integrated circuit of claim 1,
wherein said differential amplifier includes respective, inverting and noninverting, input and output voltage signal ports and a common mode output
25 voltage signal;
a first MOS transistor (604) being coupled to the noninverting input voltage signal port, a second MOS transistor (630) being coupled to the inverting input voltage signal port, a third MOS transistor (620) coupling the inverting input voltage signal port to the noninverting output voltage signal port, and a fourth MOS
30 transistor (610) coupling the noninverting input voltage signal port to the inverting output voltage signal port;



each of said MOS transistors including a controlling gate voltage;
said differential amplifier being coupled in the circuit configuration so
that said common mode output voltage signal includes an adjustable fraction (γ) of
one of said differential input voltage signal and said differential output voltage
5 signal;

the circuit configuration being adapted (FIG.5) to apply the controlling
gate voltages to said MOS transistors in a manner so that adjusting the controlling
gate voltages scales the amplitude of the second-order harmonic component of said
differential input voltage signal included in said differential output voltage signal.

10 9. The integrated circuit of claim 1,

wherein said differential amplifier includes respective, inverting and
noninverting, input and output voltage signal ports;

a first MOS transistor (440) being coupled to the noninverting input
voltage signal port, a second MOS transistor (430) being coupled to the inverting
15 input voltage signal port, a third MOS transistor (420) coupling the inverting input
voltage signal port to the noninverting output voltage signal port, and a fourth MOS
transistor (450) coupling the noninverting input voltage signal port to the inverting
output voltage signal port;

said differential amplifier being coupled in the circuit configuration
20 (FIG.6) so that adjusting the gain of said differential amplifier scales the amplitude
of the second-order harmonic component of said differential input voltage signal
included in said differential output voltage signal.

10. The integrated circuit of claim 9,

wherein each of said MOS transistors includes a controlling gate
25 voltage;

said differential amplifier being further coupled in the circuit
configuration so that adjusting the controlling gate voltage (V_{c2}) of the third and
fourth MOS transistors scales the amplitude of the second-order harmonic
component of said differential input voltage signal included in said differential
30 output voltage signal.

11. A method of applying a differential input voltage signal applied to a
differential amplifier circuit to produce a differential output voltage signal
comprising the step of:



driving said differential amplifier circuit so that said differential output voltage signal of said differential amplifier circuit includes a second-order harmonic component of said differential input voltage signal,

wherein the step of driving comprises driving said differential amplifier
5 circuit so that said differential output voltage signal of said differential amplifier circuit includes a scaled fraction of the second-order harmonic component.

12. The method of claim 11,

wherein said differential amplifier circuit includes a differential amplifier including a common mode output voltage signal;

10 the step of driving said differential amplifier circuit comprises driving the common mode output voltage signal of said differential amplifier in a manner so as to include a scaled fraction of said differential output voltage signal,

said differential amplifier being coupled in a triode-biased circuit configuration including a plurality of MOS transistors coupled to said differential
15 amplifier;

13. The method of claim 11,

wherein said differential amplifier circuit includes a differential amplifier including a common mode output voltage signal;

said differential amplifier being coupled in a triode-biased circuit
20 configuration including a plurality of MOS transistors coupled to said differential amplifier;

14. The method of claim 11,

wherein said differential amplifier circuit includes a differential amplifier including a common mode input voltage signal;

25 said differential amplifier being coupled in a triode-biased circuit configuration including a plurality of MOS transistors coupled to said differential amplifier;

the step of driving said differential amplifier circuit comprises driving the common mode output voltage signal of said differential amplifier in a manner so
30 as to include a scaled fraction of said differential input voltage signal.

15. The method of claim 11,



wherein said differential amplifier circuit includes a differential amplifier including a common mode input voltage signal and a second differential amplifier including a differential output voltage signal;

5 said first differential amplifier being coupled in a triode-biased circuit configuration including a plurality of MOS transistors coupled to said first differential amplifier;

the step of driving said differential amplifier circuit comprises driving the common mode input voltage signal of said first differential amplifier in a manner so as to include a scaled fraction of the differential output voltage signal of said
10 second differential amplifier.

16. The method of claim 11,

wherein said differential amplifier circuit includes a differential amplifier coupled in a triode-biased circuit configuration including a plurality of MOS transistors coupled to said differential amplifier, each MOS transistor in said
15 plurality including a controlling gate voltage;

said differential amplifier including a common mode output voltage signal;

said differential amplifier being coupled in said circuit configuration so that the common mode output voltage signal of said differential amplifier includes an
20 adjustable fraction of one of said differential input voltage signal and said differential output voltage signal;

wherein the step of driving comprises driving selected controlling gate voltages of said MOS transistors so as to scale the fraction of the second-order harmonic component.

25 **17. The method of claim 11,**

wherein said differential amplifier circuit includes a differential amplifier coupled in a triode-biased circuit configuration including a plurality of MOS transistors coupled to said differential amplifier, each MOS transistor in said plurality including a controlling gate voltage;

30 the driving step comprising driving selected controlling gate voltages to include a scaled fraction of said differential input voltage signal.

