

Fig. 1C

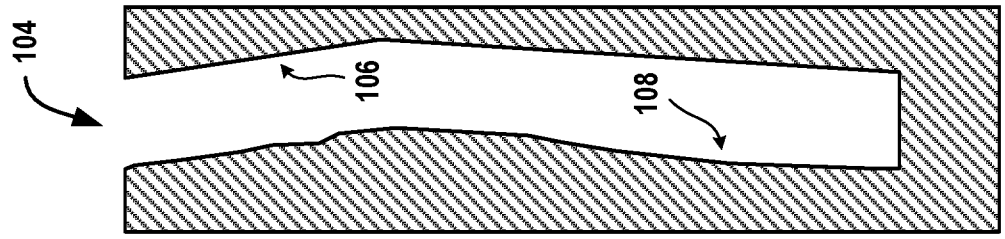

Fig. 1B

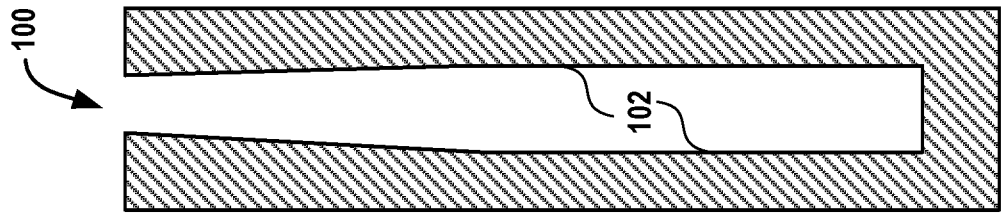

Fig. 1A

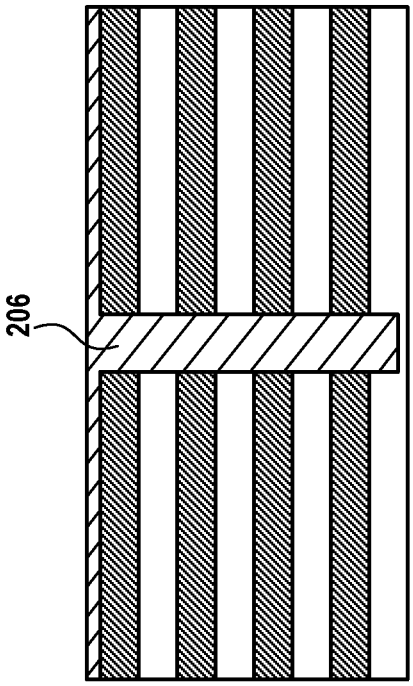

Fig. 2B

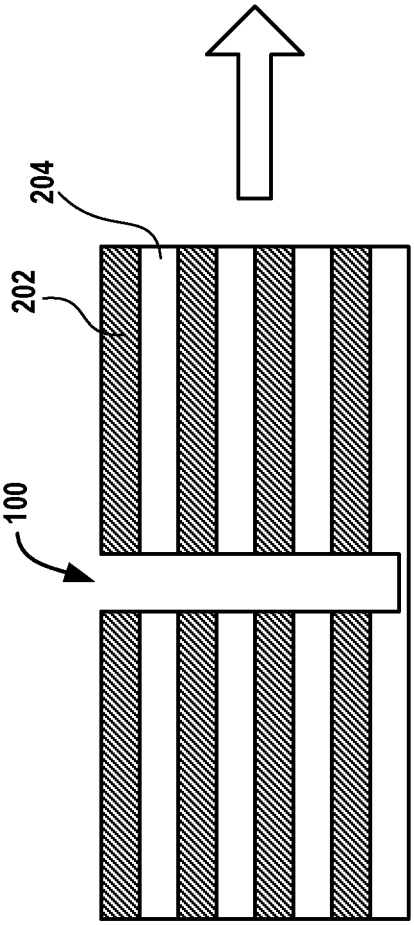

Fig. 2A

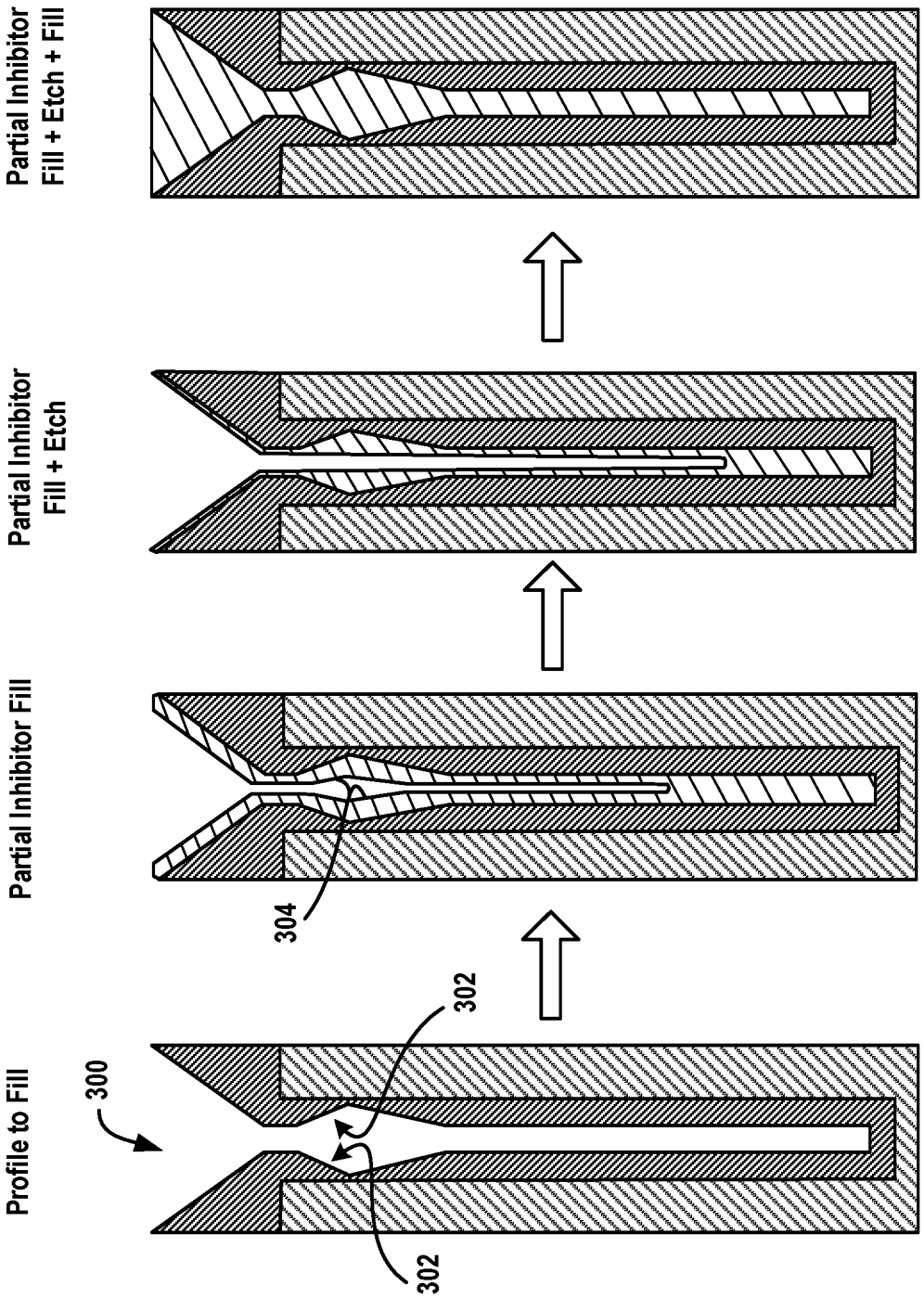

Fig. 3A

Fig. 3B

Fig. 3C

Fig. 3D

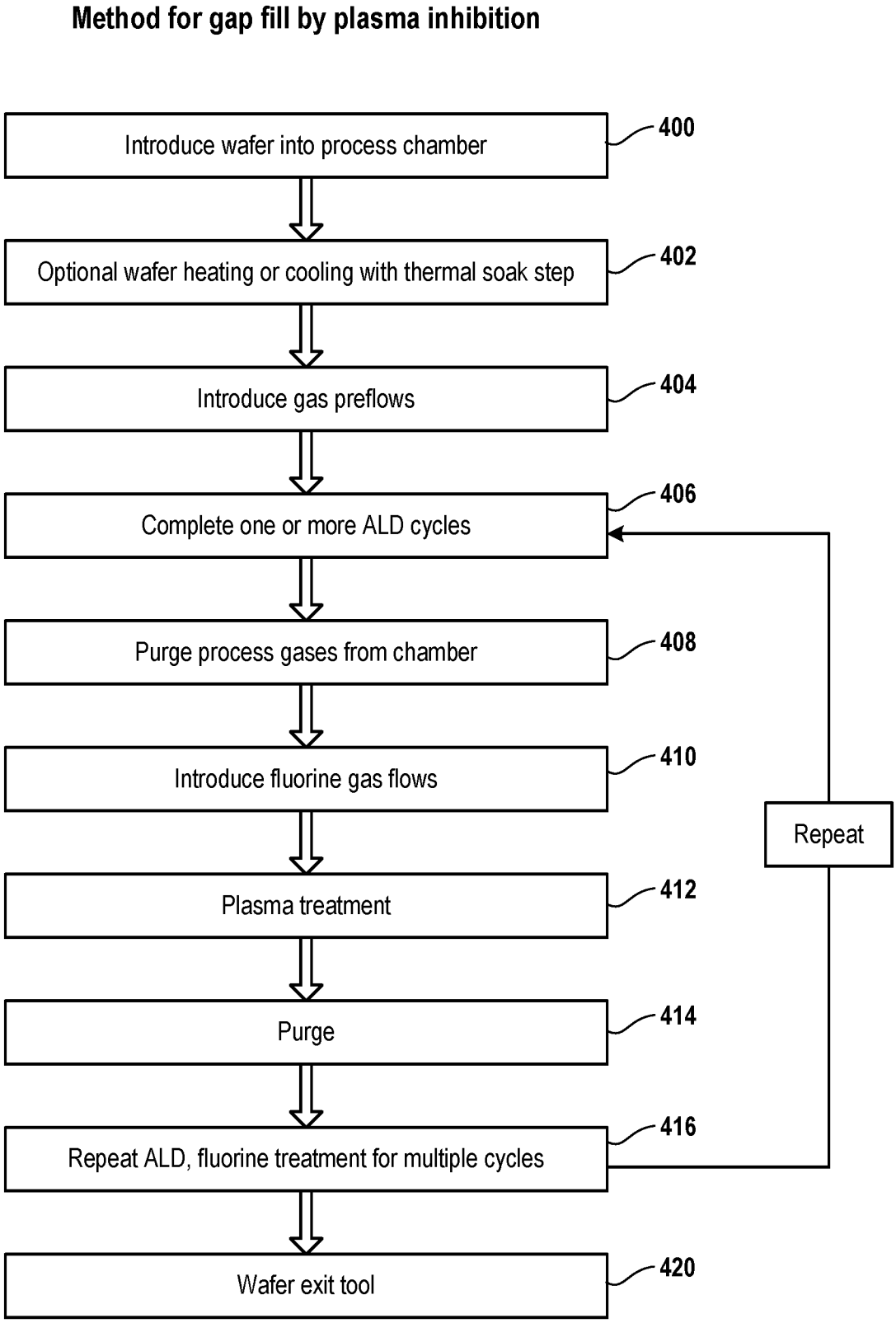
Method for gap fill by plasma inhibition
Introduce wafer into process chamber
400
Optional wafer heating or cooling with thermal soak step
402
Introduce gas preflows
404
Complete one or more ALD cycles
406
Purge process gases from chamber
408
Introduce fluorine gas flows
410
Plasma treatment
412
Purge
414
Repeat ALD, fluorine treatment for multiple cycles
416
Wafer exit tool
420
Repeat

Fig. 4

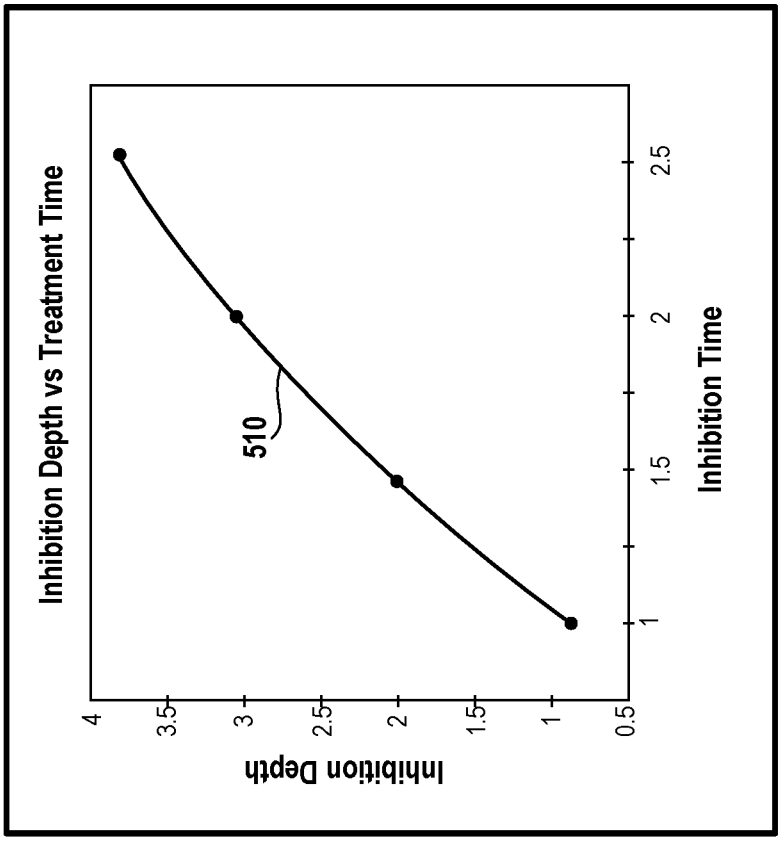
Inhibition Depth vs Treatment Time
Inhibition Depth
4
3.5
3
2.5
2
1.5
1
0.5
Inhibition Time
1
1.5
2
2.5
510

Fig. 5B

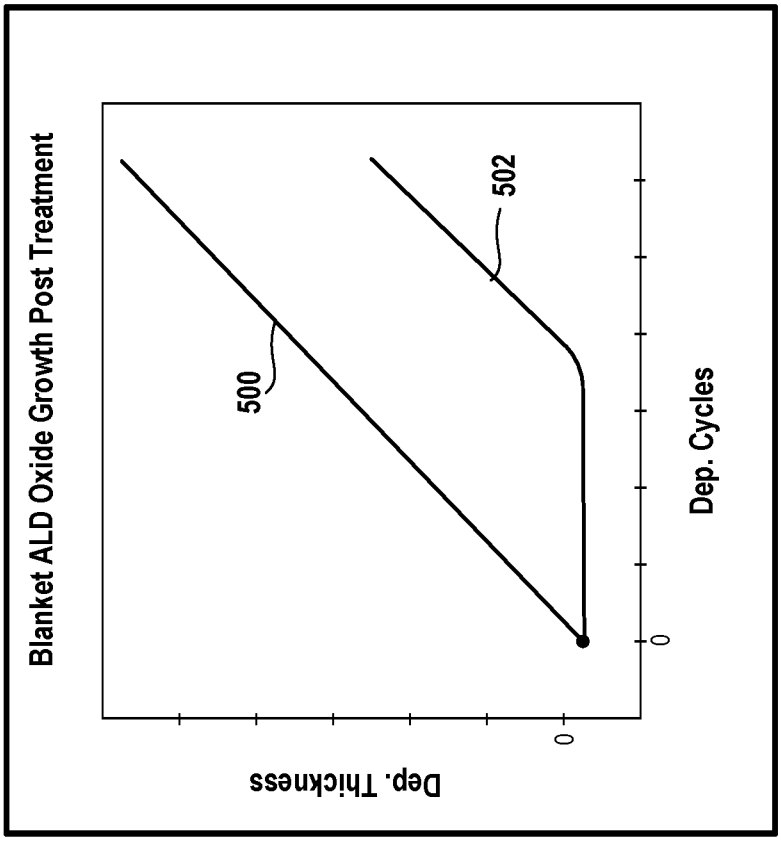
Blanket ALD Oxide Growth Post Treatment
Dep. Thickness
0
Dep. Cycles
0
500
502

Fig. 5A

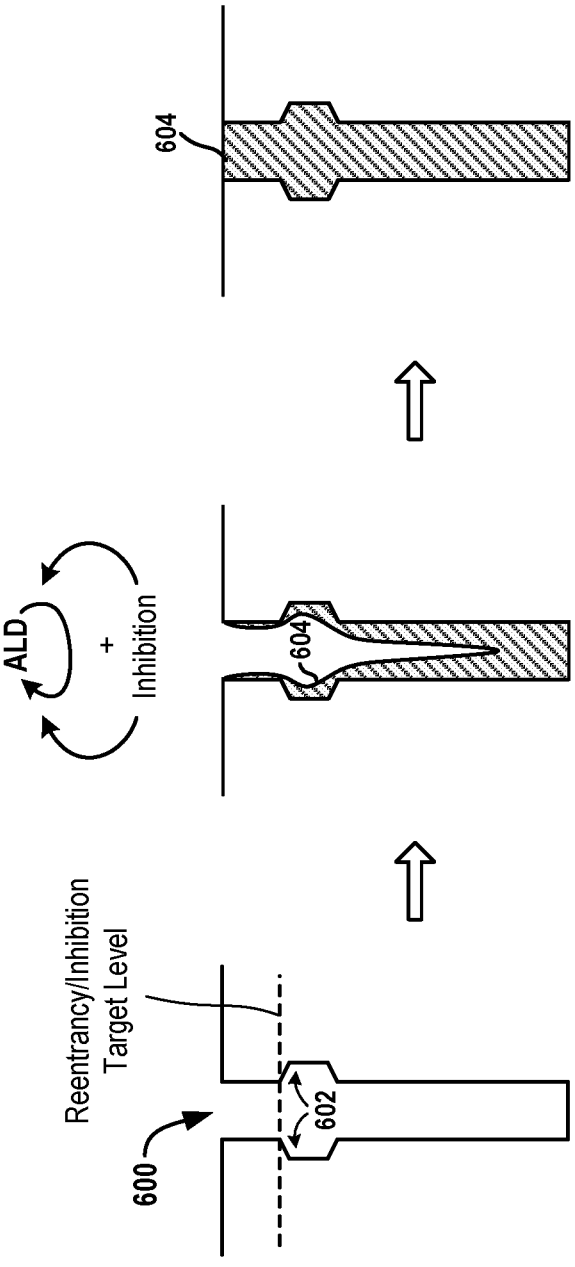

Fig. 6A

Fig. 6B

Fig. 6C

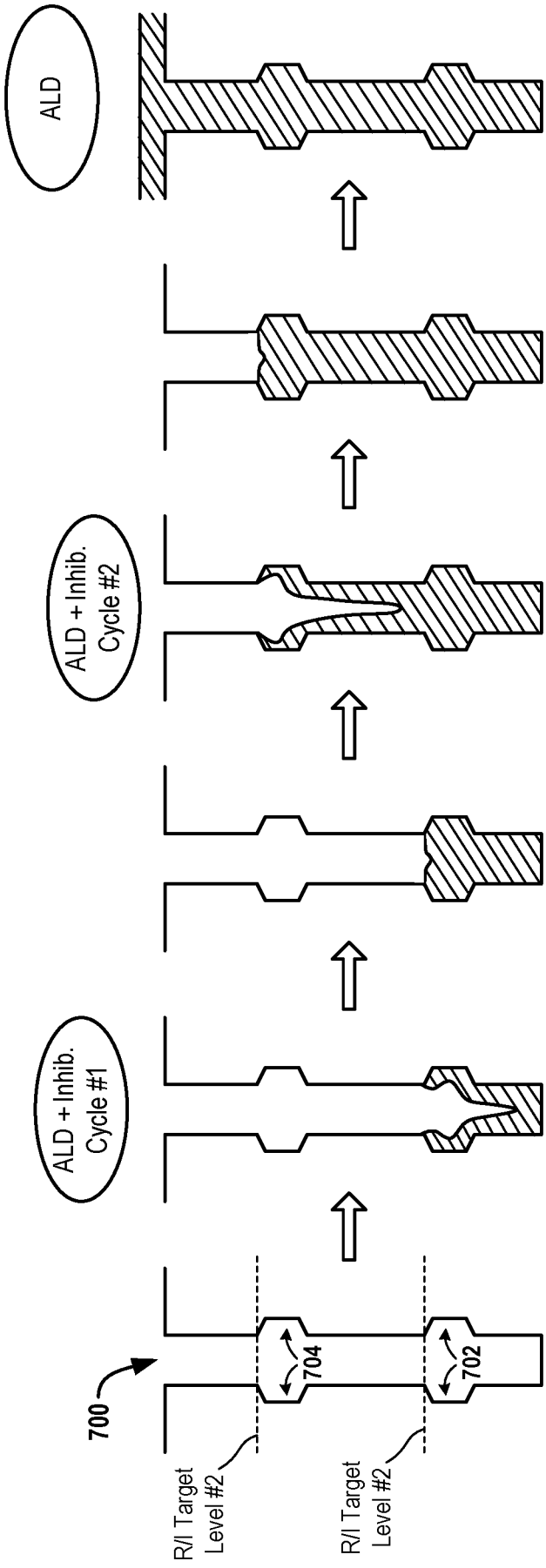

Fig. 7A Fig. 7B Fig. 7C Fig. 7D Fig. 7E Fig. 7F

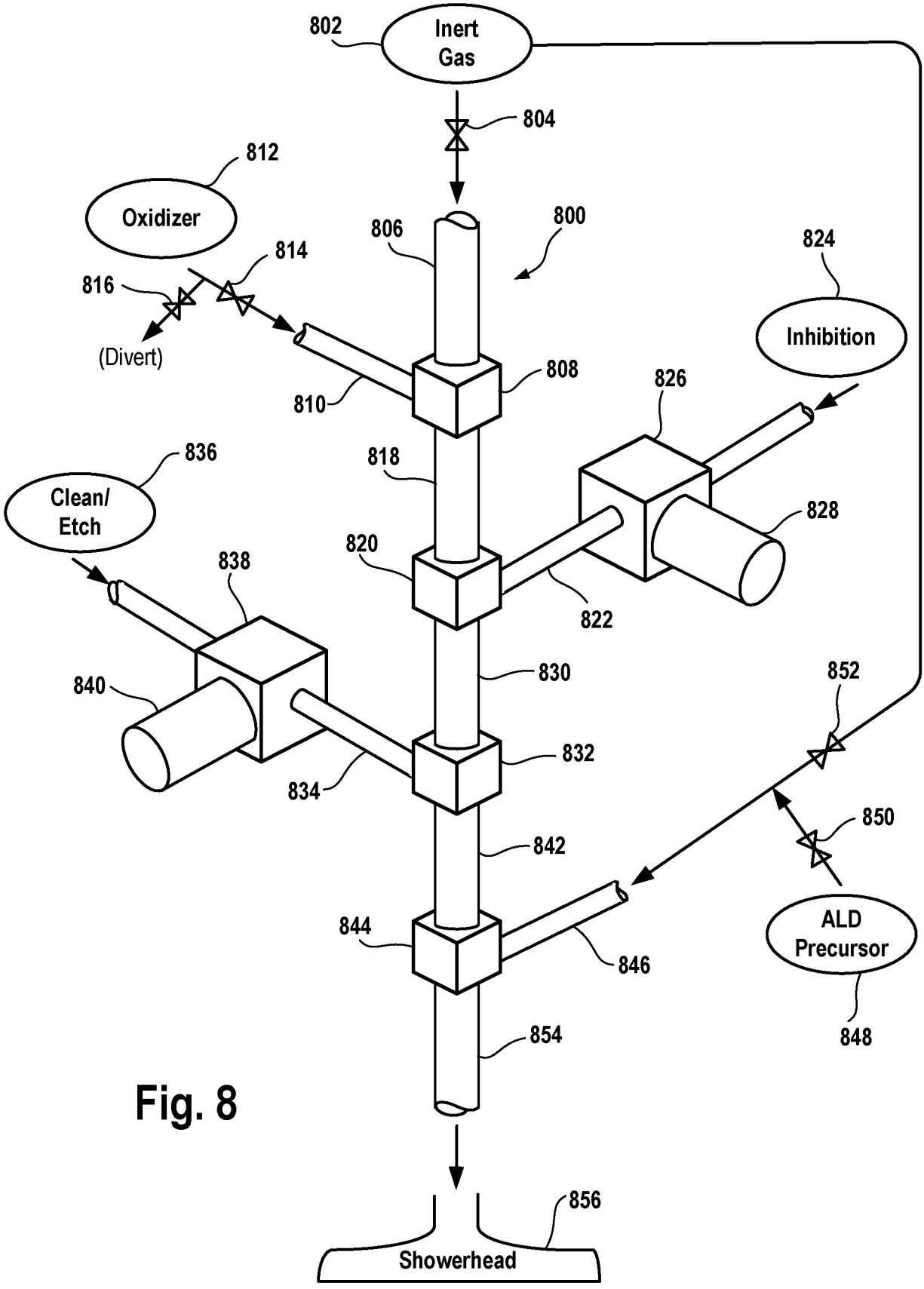
802
Inert Gas
804
812
Oxidizer
800
806
814
816
(Divert)
824
Inhibition
808
810
826
836
Clean/ Etch
818
828
820
838
822
840
830
852
832
834
850
842
844
ALD Precursor
846
848
854
856
Showerhead

Fig. 8

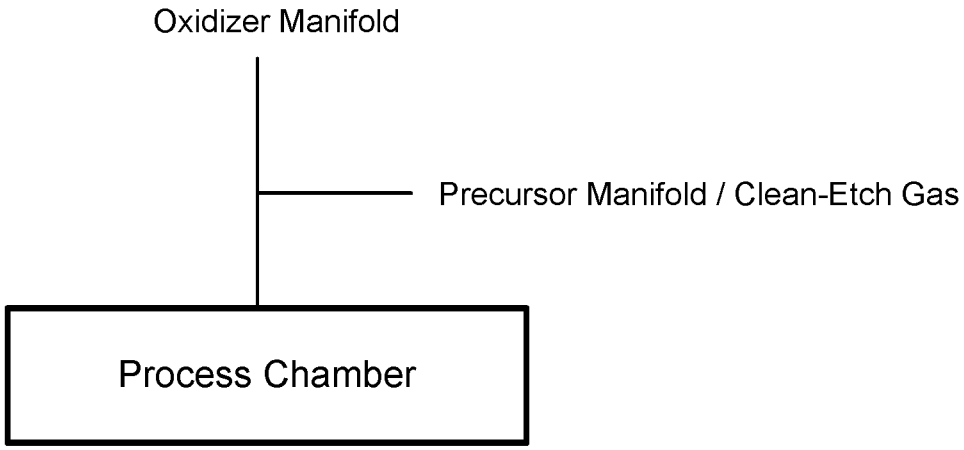
Oxidizer Manifold
Precursor Manifold / Clean-Etch Gas
Process Chamber

Fig. 9A

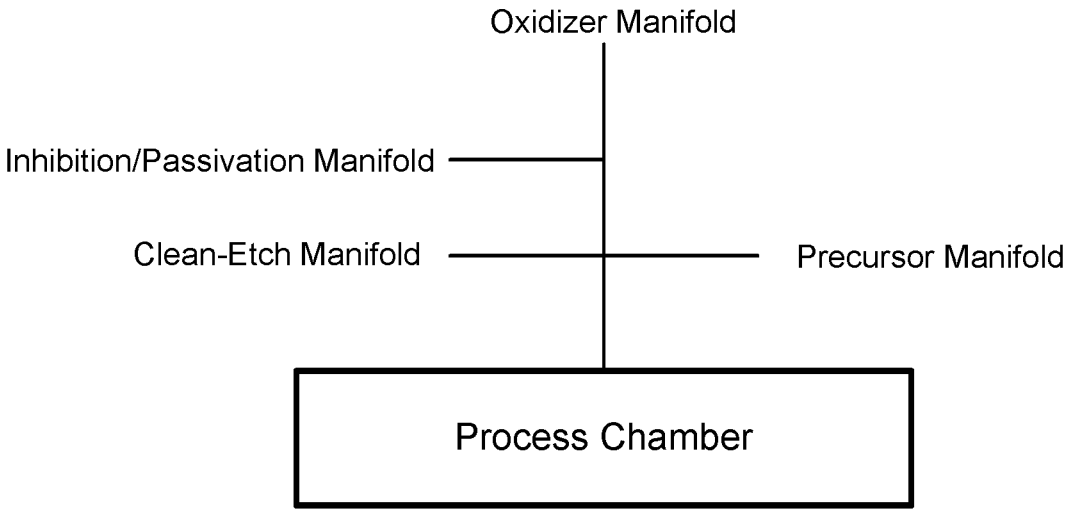
Oxidizer Manifold
Inhibition/Passivation Manifold
Clean-Etch Manifold
Precursor Manifold
Process Chamber

Fig. 9B

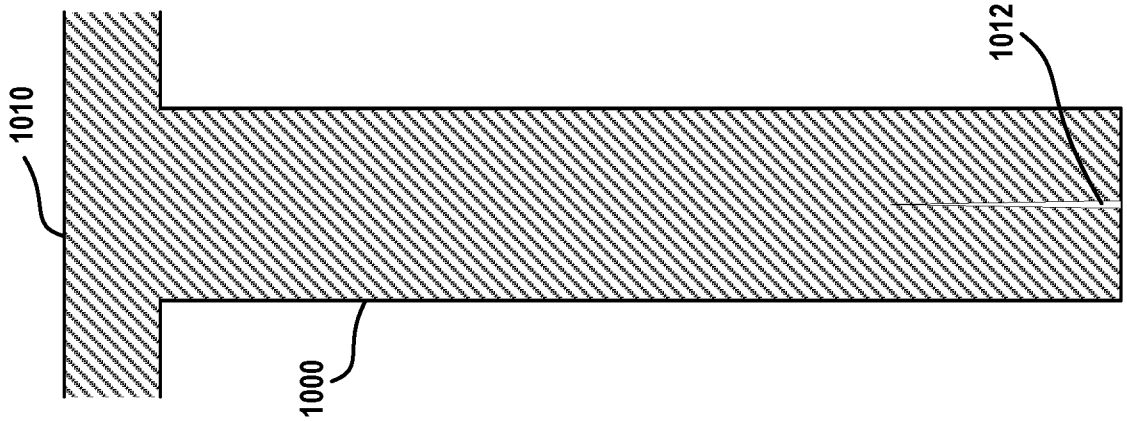

Fig. 10C

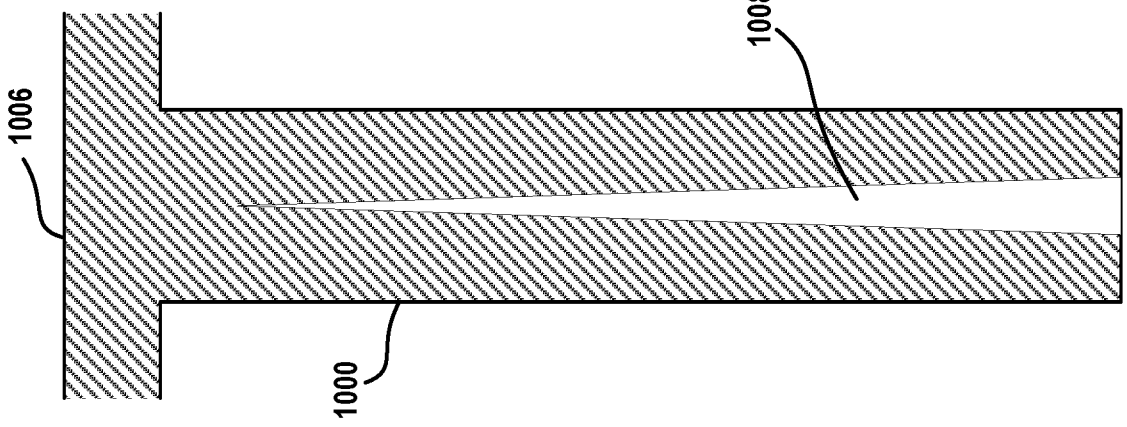

Fig. 10B

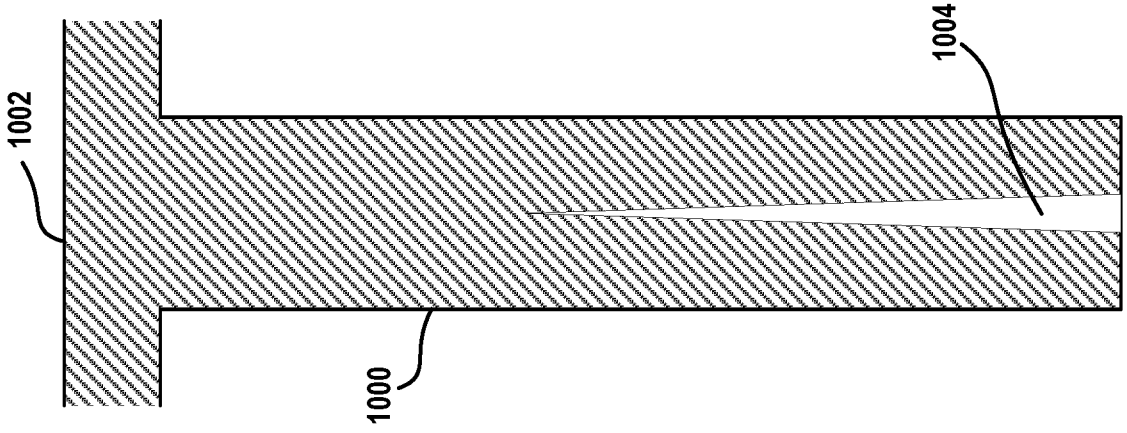

Fig. 10A

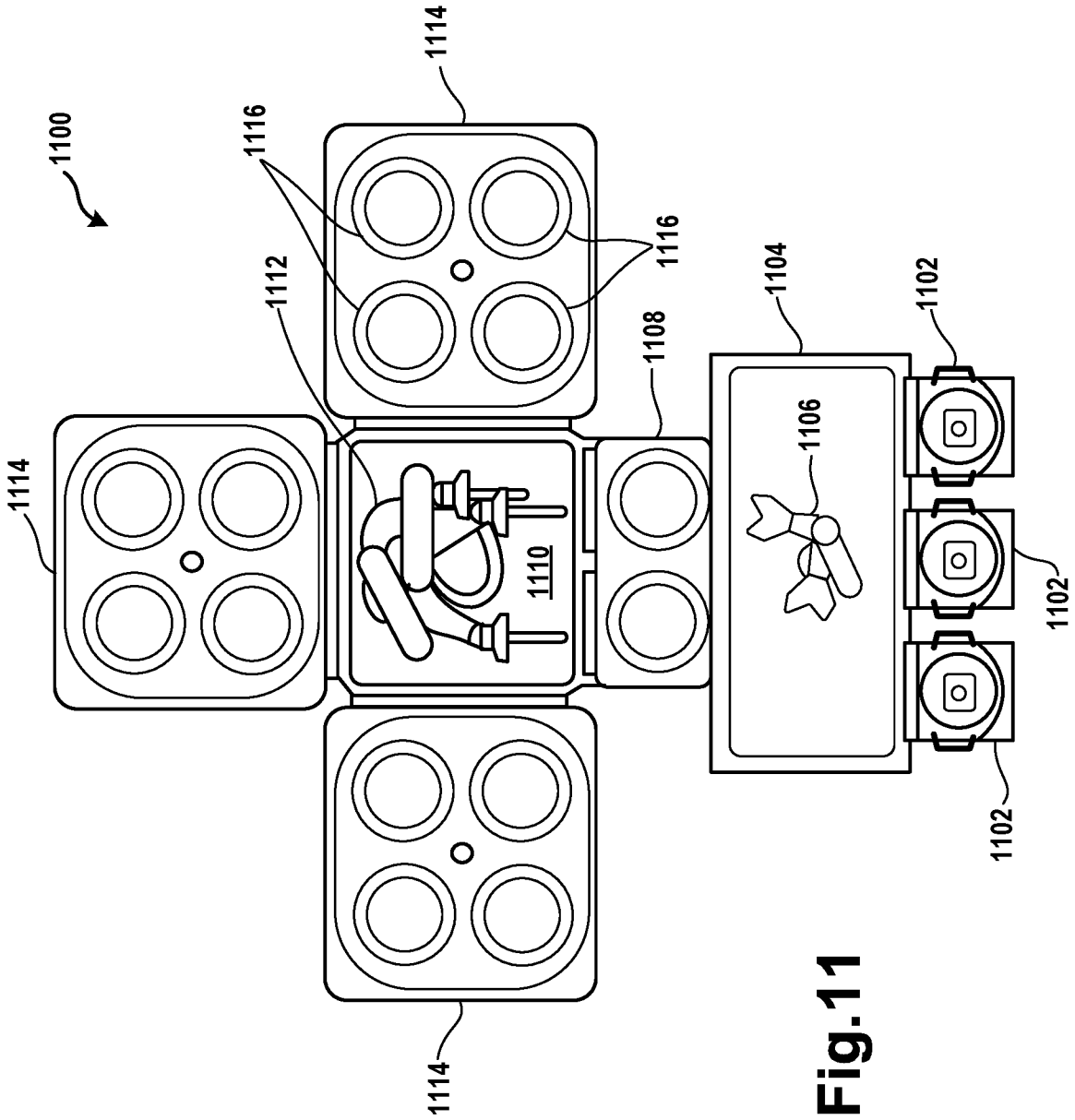
1100
1114
1116
1116
1112
1104
1102
1108
1106
1114
1110
1102
1102
1114

Fig.11

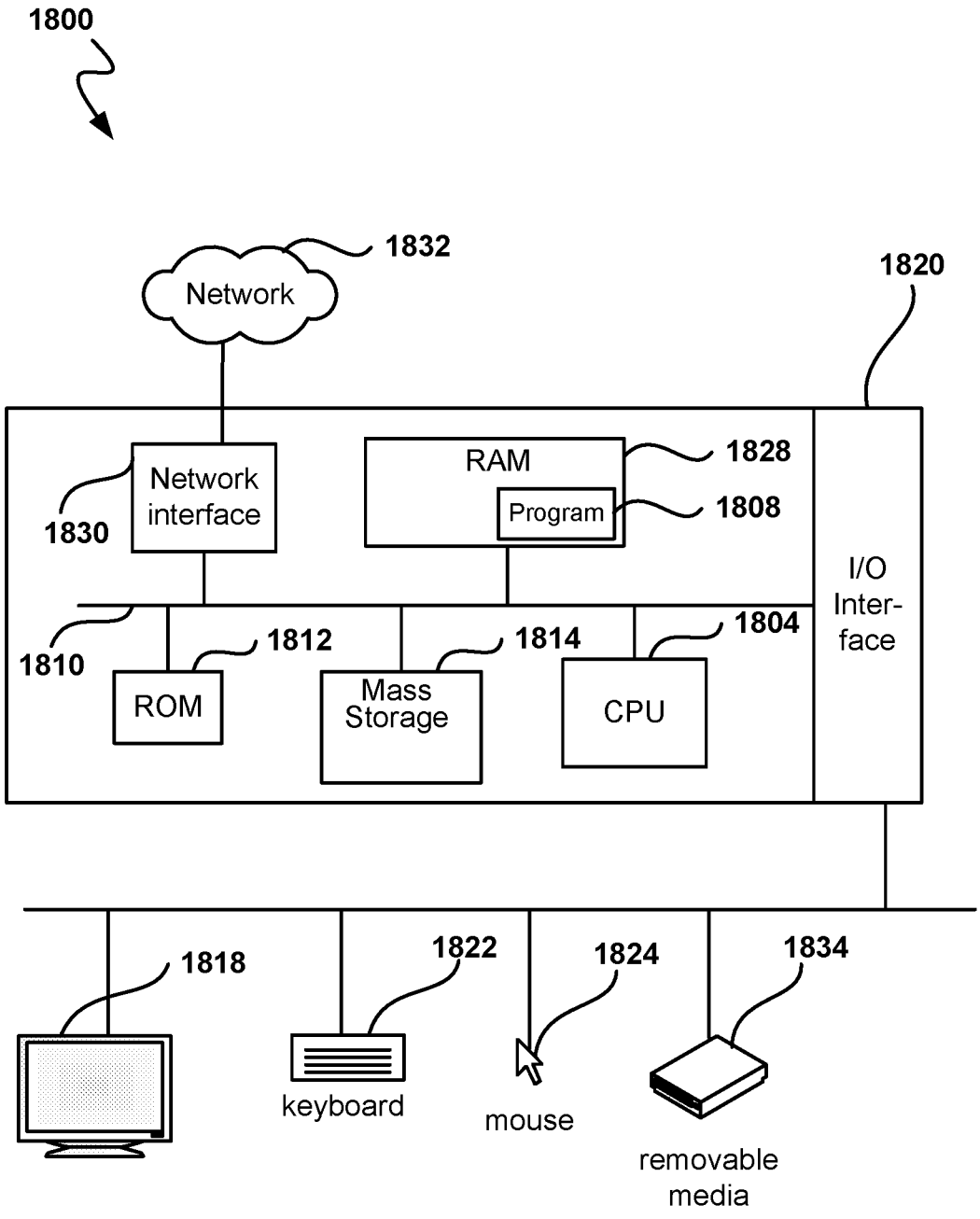
1800
1832
Network
1820
1828
RAM
Program
1808
1830
Network interface
I/O Inter-face
1810
1812
1814
1804
ROM
Mass Storage
CPU
1818
1822
1824
1834
keyboard
mouse
removable media

Fig. 12