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RASTER CORRECTED VERTICAL DEFLECTION CIRCUIT

This invention relates generally to the field of vertical deflection circuits, and in particular, to the field of switched vertical deflection circuits.

5 New generations of color television picture tube-yoke combinations may require North-South pincushion correction. A further requirement can be DC coupling between a vertical deflection amplifier and the deflection yoke, for example when producing a flicker-free AA-BB display. Each field is scanned twice,
 10 consecutively, at twice the normal scanning rate, in such AA-BB displays. It is therefore desirable to have a DC coupled vertical deflection circuit producing vertically modulated horizontal rate waveforms for applying to a simple North-South pincushion correction circuit.

15 Some of these characteristics suggest that a switched vertical deflection circuit may be appropriate. However, switched vertical deflection circuits can have the following disadvantages:

A first kind of switched vertical circuit is the synchronous switched vertical deflection circuit, often referred to as an SSVD,
 20 which employs two thyristors. The thyristors are turned on at modulated instants during the horizontal retrace period. The use of fast thyristors can require a complex control circuit, which can be too expensive. Examples of SSVD circuits are shown in the following U. S. Patents: 4,041,354; 4,079,293; 4,096,415; 4,117,
 25 380; and, 4,338,549.

A second kind of switched vertical circuit is the switched mode vertical deflection circuit, often referred to as an SMVD, which employs two switching transistors. The transistors are turned on at modulated instants during the horizontal trace period.
 30 This produces a strong phase modulation of the horizontal rate waveforms, which therefore cannot be employed for North-South raster correction. An example of an SMVD circuit is shown in U. S. Patent No. 4,174,493.

A third kind of switched vertical circuit is the single switch
 35 vertical deflection circuit, which employs either a thyristor or a transistor switch with antiparallel diode. The phase changes from



horizontal retrace to horizontal trace, from top to bottom. Examples of this third kind of switched vertical circuit are shown in the following U. S. Patents: 4,296,360; 4,544,864; and, (substitute patent number of serial number 515,901, filed April 27, 1990, and
5 allowed). Accordingly, North-South raster correction cannot be obtained.

Moreover, and to further disadvantage, the three circuits described above each require a picture tube protection circuit which shuts down the receiver when one drive signal of the switches is
10 missing, to avoid damage to the picture tube from excessive DC current.

It is an inventive arrangement to provide a new switched vertical deflection system for directly converting horizontal energy into vertical deflection current, wherein a vertically modulated
15 horizontal sawtooth voltage across a vertical deflection yoke can provide North-South pincushion correction. First and second windings are inductively coupled with opposite polarity to a source of horizontal rate retrace pulses from a horizontal deflection circuit. The windings can form part of a horizontal flyback
20 transformer in a horizontal deflection system, operating at a horizontal rate. A circuit energized by the retrace pulses generates modulated currents of opposite polarity. The modulated current generating circuit comprises respective switching networks for directing positively and negatively valued portions of the currents
25 along different paths. The negatively valued portions of the currents are conducted through switches along discharge paths to ground. Modulated quantities of the positively valued portions of the currents are conducted along charging paths through an energy storage device. The energy storage device is responsive to the
30 currents and develops a vertical deflection voltage in phase with the currents for driving a vertical deflection current in a vertical deflection yoke. The vertical deflection voltage reflects a net average charge resulting from charging by the oppositely directed currents. The net average charge is determined by subtracting the
35 positively valued part of one of the currents from the positively valued part of the other current. The vertical deflection voltage is



not subject to phase modulation, as in the prior art switched vertical systems described above. Accordingly, a North-South pincushion correction current in phase with the horizontal deflection circuit is generated by integration of the vertical
5 deflection voltage in the vertical deflection yoke. Horizontal rate waveforms phased correctly for producing North-South raster correction, and for other correction circuits, are provided.

It is another inventive arrangement to provide a switched vertical deflection system which can provide enhanced North-South
10 pincushion correction by use of a pincushion transformer. A pincushion transformer has a first winding capacitively coupled to the energy storage device and a second winding forming part of a horizontal rate resonant circuit coupled in series with the vertical deflection yoke.

15 It is still another inventive arrangement to obviate the need for shutting down the receiver when one drive signal of the switches in a switched vertical deflection system is missing, to avoid damage to the picture tube from excessive DC current. In switched vertical deflection systems in the prior art, the windings of the flyback
20 transformer are DC coupled in series with inductors, which are in turn DC coupled to the switches, or switching networks, and to an energy storage device. In the switched vertical deflection systems taught herein, each inductor can be AC coupled to the respective switch, or switching network, and to the energy storage device by a
25 capacitor.

It is yet another inventive arrangement to provide a plurality of advantageous topological features, which contribute to improved operation of switched vertical deflection systems. The windings of the flyback transformer coupled to the source of horizontal retrace
30 pulses are coupled together at a first junction, and the first junction is coupled to ground. The windings can be separate, substantially identical windings. Alternatively, the windings can be different halves of a substantially centertapped winding, in which case the center tap is coupled to ground. First and second switches,
35 or switching networks, are respectively coupled to the first and second windings and coupled together at a second junction. The



energy storage device for developing the vertical deflection voltage is coupled to the second junction. Respective energy storage devices are coupled to the inductances, which are themselves coupled to the respective windings. The energy storage devices are charged
5 oppositely by respective currents flowing through the windings. The energy storage devices are coupled to the respective switches, or switching networks, providing an access for the current modulating control. The energy storage devices can be embodied as capacitors, which also provide the AC coupling described above.

10 In the Drawings:

FIGURE 1 is a circuit diagram, in partial block form, showing a switched vertical deflection circuit according to an inventive arrangement.

15 FIGURES 2(a)-2(f) are waveforms useful for explaining the operation of the circuit shown in FIGURE 1.

FIGURE 3 is an illustrative vertical deflection circuit in according to an inventive arrangement.

A switched vertical deflection system 10 is shown Figure 1. A horizontal deflection circuit 12, as known in the prior art, is
20 coupled to a winding W1 of flyback transformer T1. Horizontal deflection circuit may operate at a horizontal scanning frequency of f_H , as for conventional interlaced scanning. Scanning at f_H , for example, can correspond to a rate of approximately 15,750 Hz for NTSC interlaced standards. Horizontal deflection circuit 12 may
25 also operate at a multiple thereof, for example $2f_H$, as for progressive noninterlaced scanning. The scanning rates f_H and $2f_H$ will have different values for PAL and SECAM standards.

Flyback transformer T1 has another winding W2, which is inductively coupled to winding W1. Winding W2 has a centertap 16
30 coupled to ground. The center tap 16 defines two windings, or winding portions, W2a and W2b of opposite polarity relative to one another. Accordingly, positive retrace pulses are generated by winding W2a and negative retrace pulses are generated by winding W2b. Windings W2a and W2b receive energy from the horizontal
35 deflection system by means of the retrace pulses. The energy is made available to the switched vertical deflection system 10 for



generating a vertical deflection current in a vertical deflection yoke.

Briefly, and as will be explained in more detail below, the flyback transformer T1 supplies energy from the horizontal deflection system to the vertical yoke by means of currents i_1 and i_2 which follow respective conduction paths between the respective windings W2a and W2b and the storage capacitor C3. Current i_3 , which is the difference of currents i_1 and i_2 , charges storage capacitor C3 at the horizontal rate. Storage capacitor C3 thereby develops a vertical deflection voltage V1. Capacitor C3 discharges into a deflection yoke Lv to produce a vertical deflection current i_4 . A feedback loop including resistor R3 linearizes and stabilizes the deflection circuit. A control circuit 14 generates the base drive signals for switching transistors Q1 and Q2.

The respective conduction paths for currents i_1 and i_2 include: respective storage coils, or inductors, L1 and L2; respective coupling capacitors, or energy storage devices, C1 and C2; and, respective diodes D2 and D3. Diodes D2 and D3 are polarized for conduction of horizontal retrace current.

Diodes D1 and D2 and transistor Q1 form a first switch, or switching network, 18, operatively associated with current i_1 . Diodes D3 and D4 and transistor Q2 form a second switch, or switching network, 20, operatively associated with current i_2 . Diodes D1 and D4 also serve to isolate transistors Q1 and Q2 from reverse voltages appearing at the collectors during horizontal retrace. Switching networks 18 and 20 are responsive to the control circuit 14, the operation of which is explained in more detail in connection with FIGURE 3.

When transistor Q1 is nonconductive, capacitor C1 charges negatively at the junction of diodes D1 and D2, responsive to the positive retrace pulses on winding W2a. When transistor Q2 is nonconductive, capacitor C2 charges positively at the junction of diodes D3 and D4, responsive to the negative retrace pulses on winding W2b. Capacitors C1 and C2 charge to the peak horizontal retrace voltage applied by windings W2a and W2b respectively. When transistors Q1 and Q2 are nonconductive, current i_3 does not



flow, so that capacitor C3 does not receive any charge. The vertical deflection current i_4 in vertical deflection yoke L_v remains zero.

The positive currents i_1 and i_2 are controlled by the amount of discharge of capacitors C1 and C2, respectively. The amount of
5 discharge of capacitors C1 and C2 is controlled by modulating the conduction time of transistors Q1 and Q2, respectively. Transistors Q1 and Q2 are switched on at varying times within the interval t_5 - t_6 in FIGURES 2(a) - 2(f), as explained in more detail below. The transistors Q1 and Q2 are turned off during the horizontal retrace
10 interval when diodes D1 and D4 are reverse biased by horizontal retrace pulses.

Briefly, at the start of vertical trace, transistor Q1 is turned on at time t_5 and transistor Q2 is turned on at time t_6 . This causes a large positive current i_1 to flow until time t_4' , and a small
15 positive current i_2 to flow until time t_3' . The current flow of currents i_1 and i_2 is due to the energy stored during horizontal retrace in coils L1 and L2, respectively. The instant at which transistor Q1 is turned on is progressively retarded from time t_5 to time t_6 during vertical trace. During that same interval, the instant
20 at which transistor Q2 is turned on is progressively advanced from time t_6 to time t_5 . This causes a decreasing amplitude of current i_1 and an increasing amplitude of current i_2 , as shown in the right hand parts of FIGURE 2(b).

A yoke current is obtained when capacitors C1 and C2 are
25 discharged by transistors Q1 and Q2, respectively. A positive yoke current is obtained when transistor Q1 is in saturation. The positive retrace voltage generates a charge current flowing through inductor L1, capacitor C1, diode D2 and capacitor C3 to ground, resulting in a positive voltage across capacitor C3. When the charge current falls
30 to zero during the first half of the horizontal trace interval, then the charge, or voltage, across capacitor C1 causes diode D2 to become back biased and diode D1 to become forward biased. Capacitor C1 starts to discharge through diode D1 and saturated transistor Q1 during the second half of the horizontal trace time.

35 A negative yoke current is obtained when transistor Q2 is in saturation. The negative retrace voltage generates a charge current



flowing from ground through capacitor C3, diode D3, capacitor C2 and inductor L2, resulting in a negative voltage across capacitor C3. When the charge current falls to zero during the first half of the horizontal trace interval, then the charge, or voltage, across
5 capacitor C2 causes diode D3 to become back biased and diode D4 to become forward biased. Capacitor C2 starts to discharge through diode D4 and saturated transistor Q1 during the second half of the horizontal trace time.

Thus, the amount and polarity of the deflection current i_4 is
10 determined by the amount of discharge current flowing through transistors Q1 and Q2. Transistors Q1 and Q2 may operate in a switched manner, or even in class A, providing a current sink or current source. Bipolar transistors Q1 and Q2 as shown in FIGURE 1 may be replaced by any other device providing a controllable
15 discharge path. In the following description, transistors Q1 and Q2 operate in a switched manner to minimize dissipation.

A number of waveforms useful in explaining operation of the switched vertical deflection system 10 are shown in the various parts of FIGURE 2. The left hand side of each part in FIGURE 2 shows
20 horizontal rate waveforms. The right hand side of each part shows the corresponding vertical rate waveforms. The time lines of the vertical rate waveforms are marked with respect to the TOP, CENTER and BOTTOM of the display, or field. The vertical retrace interval is between the BOTTOM of a field and the TOP of the next successive
25 field. FIGURE 2(a) shows only horizontal rate retrace pulses. FIGURE 2(b) shows separate vertical rate waveforms for currents i_1 and i_2 , shown together at the horizontal rate. The upper parts of each of the vertical rate waveforms for currents i_1 and i_2 show the positively valued portions of currents i_1 and i_2 respectively,
30 flowing through diodes D2 and D3 respectively. The lower parts of each of the vertical rate waveforms for currents i_1 and i_2 show the negatively valued portions of currents i_1 and i_2 respectively, flowing through transistors Q1 and Q2 respectively. FIGURE 2(c) shows current i_3 . FIGURE 2(d) shows voltage V1. FIGURE 2(e) shows
35 voltage V2. FIGURE 2(f) shows only the vertical rate current i_4 .



In operation, deflection current i_4 starts with positive peak amplitude at the start, or TOP, of the vertical trace. At the TOP, transistor Q1 is switched into saturation at time t_5 and substantially discharges C1. This causes a large amplitude of charge current i_1 flowing through diode D2. Stored horizontal retrace energy in coil L1 causes positive current i_1 to flow until time t_4' . Transistor Q2 is turned on at time t_6 producing a small discharge current i_2 and consequently a small charge current i_2 which flows through diode D3 until time t_3' . The vertical yoke is driven by current i_3 which is the difference of positively valued portion of current i_1 minus the positively valued portion of current i_2 . Current i_3 , the waveform shown in FIGURE 2(c), charges capacitor C3 producing voltage V1, the waveform shown in FIGURE 2(d). Voltage V1 increases until the amplitude of current i_3 becomes smaller than the amplitude of the deflection current i_4 .

Deflection current i_4 , the waveform shown in FIGURE 2(f), is obtained by discharging capacitor C3 through the vertical deflection yoke L_v and current sampling resistor R_s . The deflection yoke L_v integrates the horizontal rate voltage across capacitor C3 to a substantially sawtooth current at the vertical rate. Due to the large inductance of the deflection winding, the discharge current cannot follow the roughly triangular horizontal rate voltage across capacitor C3. Consequently, the current i_4 through the deflection winding results from the average of the voltage across the capacitor C3. Therefore, the deflection winding acts as a current sink to discharge capacitor C3. The parallel resonant frequency of the capacitor C3 and the deflection winding determines the vertical retrace interval. The sawtooth shaped voltage V1, as integrated by the high inductance of the deflection yoke L_v , produces at least some parabolic North-South raster correction current. A deflection current sample across sampling resistor R_s is fed back to the control circuit 14 to linearize the operation of the deflection circuit.

During the first half of vertical trace, that is from the TOP to the CENTER, the turn on time of transistor Q1 is progressively retarded from time t_5 , toward time t_6 . During the same interval,



the turn on time of transistor Q2 is progressively advanced from time t_6 , toward time t_5 . This causes a progressively decreasing amplitude of current i_1 and a progressively increasing amplitude of current i_2 . The amplitude of current i_3 , which is the difference of
5 the positively valued portion of current i_1 minus the positively valued portion of current i_2 , also progressively decreases. As a result, the amplitudes of voltage V_1 and vertical deflection current i_4 also progressively decrease. The amplitudes of the positively valued portions of currents i_1 and i_2 are equal at the CENTER of
10 vertical trace. Consequently, current i_3 , voltage V_1 and current i_4 are zero. Current i_1 flows through diode D2 and transistor Q1 and current i_2 flows through diode D3 and transistor Q2.

During the second half of vertical trace, Q1 continues to be turned on progressively retarded from time t_5 , toward time t_6 .
15 Transistor Q2 continues to be turned on progressively advanced from time t_6 , toward time t_5 . This causes a further progressive decrease of current i_1 and a further progressive increase of current i_2 . As a result, current i_3 , voltage V_1 and current i_4 progressively increase in the negative direction.

20 Vertical retrace starts when the turn on time of transistor Q1 is quickly shifted from back from time t_6 to time t_5 , and transistor Q2 is held in cut off. This causes a retrace resonance of one half cycle between vertical deflection yoke L_v and capacitor C3, causing a rapid and loss free reversal of the deflection current i_4 . As
25 vertical deflection current i_4 changes its direction rapidly, a large but narrow retrace voltage pulse is produced, evident in the righthand portion of waveform 2(d) showing voltage V_1 . As explained above, the turn on times of transistors Q1 and Q2 are modulated during the interval from time t_5 to time t_6 to obtain a
30 modulated current i_3 , which starts to flow at the CENTER of horizontal retrace and ends at time t_4' . Transistors Q1 and Q2 are turned off during the second half of retrace when diodes D1 and D4 are non-conductive.

The circuit requires some overlap of currents i_1 and i_2 to
35 avoid deflection current distortions or discontinuities. This is illustrated by vertical rate waveforms of currents i_1 and i_2 .



Overlap current is highest at the CENTER of the vertical trace when current i_3 is zero. The overlap current decreases from the CENTER toward TOP and BOTTOM. The overlap current can be determined by subtracting current i_3 from current i_1 during the first half of trace, and by subtracting current i_3 from current i_2 during the second half of trace.

The time duration of the envelope of current i_3 is not modulated because current i_3 is formed by the difference of the positively valued portions of currents i_1 and i_2 . This causes horizontal sawtooth voltage V_1 to be in phase with the horizontal retrace pulses. The peaks of voltage V_1 appear always at time t_4 , where current i_3 decreases to zero. This allows a North-South pincushion correction circuit 22 to be driven by voltage V_1 , as shown in FIGURE 1. A pincushion transformer T2 has a primary winding W3 coupled to capacitor C3 through capacitor C4. A secondary winding W4 forms a line frequency resonant circuit with a capacitor C5, producing the vertically modulated sine wave voltage V_2 , shown in FIGURE 2(e), at the low side of the deflection yoke L_v . Voltage V_2 generates a cosine wave (90 degrees phase shifted) raster correction current in vertical deflection yoke L_v as it is required for raster correction. In other words, the horizontal rate sawtooth voltage V_1 is applied to the primary winding W3 of transformer T2 through capacitor C4. The secondary winding W4 forms a horizontal rate resonant circuit together with capacitor C5 to produce the modulated sine wave voltage V_2 . Sine wave voltage V_2 injects a cosine current into the yoke winding, as required for North-South raster correction. The zero-crossings of the horizontal rate envelope of voltage V_2 are not modulated. Further, the zero-crossing is always at the center of the horizontal retrace interval. Voltage V_1 , being in phase with horizontal rate waveforms, may be employed by other circuits for correcting moustache and gullwing distortion and for dynamic convergence.

Vertical deflection deflection yoke L_v is DC coupled to switching transistors Q1 and Q2 and to the control circuit 14. This permits the use of this circuit in receivers with AA-BB display or other features requiring dynamic raster shift. Flyback transformer



winding W2 is AC coupled to the vertical deflection circuit by capacitors C1 and C2. The AC coupling allows operation of the deflection circuit without a picture tube protection circuit. The absence of base drive for either or both of transistors Q1 and Q2
5 does not produce excessive DC current in vertical deflection yoke Lv, such as may damage the picture tube.

The value of capacitor C3 is matched to the inductance of vertical deflection yoke Lv to produce a correct vertical retrace time. Further, voltage V1 should decrease to about ground potential
10 at time t1'. The averaged horizontal retrace voltage, or the trace voltage across winding sections W2a and W2b, should be twice the required peak voltage across vertical deflection yoke Lv. Inductors L1 and L2, and capacitors C1 and C2 are equal in value. The component values are selected to obtain the necessary amplitude and
15 shape of currents i1 and i2.

FIGURE 3 shows a more complete circuit schematic for the switched vertical deflection circuit 10, adapted for operation with a Videocolor 110° SP picture tube type A68 EAU00X01. The various operational waveforms are similar to those shown in FIGURE 2. Peak
20 to peak values of currents and voltages are noted directly, as are some additional waveforms.

The control circuit employs a quad voltage comparator U1. Each output transistor Q1, Q2 is driven by two comparators U1a, U1b or U1c, U1d connected in parallel, for obtaining adequate base drive.
25 Nonlinear horizontal ramp voltage V3 is produced by network 24, including resistor R14, capacitor C11 and capacitor C12. Negative retrace pulses from winding W2b are an input to network 24. Nonlinear horizontal ramp voltage V4 is produced by network 26, including resistor R16, capacitor C13 and capacitor C14. Positive
30 retrace pulses from winding W2a are an input to network 26. Voltage waveforms V3 and V4 are shown in FIGURE 3, upper right. A voltage divider formed by resistor R12 and adjustable resistor R13 provide centering control.

A vertical sawtooth input current i5 is combined with vertical
35 feedback current i6 at the junction of resistors R3 and R4, resulting in vertical drive voltage V5. Vertical drive voltage V5 is compared



with each of ramp voltages V3 and V4 for producing transistor switching pulses modulated in the time interval t_5 - t_6 . The non-linearity of the horizontal ramp voltages V3 and V4 avoids instabilities during vertical retrace, and in particular, during the sharp negative peak of voltage V5. Without the non-linearity shown, transistor Q1 can turn on too early and produce some ringing at the very TOP of the raster.

The overlapping operation of the output stage, explained above in connection with FIGURES 1 and 2, is obtained by the overlap of the horizontal ramp voltages V3 and V4, clear from the illustration in FIGURE 3. The overlapping is controlled by network 24, wherein resistor R15 and diode D7 charge capacitor C12 negatively, to reduce the natural overlap of ramp voltages V3 and V4. More particularly, network 24 sets the DC level of ramp voltage V3.

The peak collector voltages on transistors Q1 and Q2 are approximately 70 volts during vertical trace. During vertical retrace, the collector voltage of transistor Q2 increases to approximately 150 volts because capacitor C2 is clamped by diode D3 to the vertical deflection yoke retrace voltage. A Zener diode D5 is connected across transistor Q2 for protection during retrace. The Zener diode D5 limits the collector voltage on transistor Q2 to approximately 120 volts. The peak to peak pincushion correction current in deflection yoke L_v is approximately 100 mA, corresponding to a pincushion distortion of approximately 14%.

The loading of the flyback transformer T1 is symmetrical, in contrast to other switched vertical deflection circuits. This avoids horizontal raster distortion in the East-West direction. No DC power supply is needed. The AC coupling between the flyback transformer and the deflection circuit, provided by capacitors C1 and C2, protects the picture tube against excessive yoke currents in the absence of base drive for transistors Q1 and/or Q2. The circuit may be adapted to different yoke impedances by changing component values. Operation without North-South raster correction can be implemented by omitting transformer T2 and the associated components. The DC yoke coupling allows $2f_H$, 100 Hz field



sequential (AA-BB) operation. The components determining the frequency must be changed for operation at $2f_H$ and 100 Hz.

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CLAIMS:

1. A switched vertical deflection system, comprising:
first (W2a) and second (W2b) windings inductively coupled with opposite polarity to a source of horizontal rate retrace pulses from a horizontal deflection circuit (12);
means (L1,L2) energized by said retrace pulses for generating modulated currents of opposite polarity;
a vertical deflection yoke (LV); and,
energy storage means (C3) responsive to said currents for developing a vertical deflection voltage (V1) in phase with said currents for driving a vertical deflection current (i4) in said vertical yoke, characterized by a North-South pincushion correction current in phase with said horizontal deflection circuit (12) being generated by integration of said vertical deflection voltage (V1) in said vertical deflection yoke (LV).
2. The system of claim 1, characterized in that said vertical deflection voltage (V1) is related to an amplitude difference between said currents.
3. The system of claim 1, characterized in that said vertical deflection current (i4) is related to an amplitude difference between positively valued portions of said currents.
4. The system of claim 1, characterized in that said windings (W2a,W2b) are AC coupled to said modulated current generating means (L1,L2) and to said energy storage means (C3).
5. The system of claim 1, characterized in that said modulated current generating means comprises respective means (Q1,Q2) for diverting negatively valued portions of said currents from flowing through said energy storage means (C3).





6. The system of claim 1, characterized in that said modulated current generating means (L1,L2) comprises respective means (Q1,Q2) for directing positively and negatively valued portions of said currents along different paths.

7. The system of claim 6, characterized in that each of said directing means comprises a switch (Q1,Q2) and two diodes (D1,D2; D3,D4), one of said diodes (D1,D2) conducting positively valued portions of said respective current through said energy storage means (C3) and the other of said diodes (D3,D4) conducting negatively valued portions of said respective current through said switch (Q1,Q2).

8. The system of claim 7, characterized in that said diodes (D1,D2,D3,D4) are coupled in series at a junction (D2,D3), said positively and negatively valued portions of said respective current being present at said junction.

9. The system of claim 5 or 8, characterized in that said respective directing means (Q1,Q2) are coupled to one another at a second junction (ground), and said second junction is coupled to said energy storage means (C3).

10. The system of claim 1 or 9, characterized by a pincushion transformer (T2) having a first winding (W3) capacitively coupled to said energy storage means (C3) and a second winding (W4) forming part of a horizontal rate resonant circuit coupled in series with said vertical deflection yoke (LV).

11. The system of claim 6, wherein each of said directing means comprises:

a current discharge path (Q1,Q2);

means for conducting positively valued portions of said respective current through said energy storage means (C3) and for conducting negatively valued portions of said respective current through said current discharge path (Q1,Q2).





12. The system of claim 11, characterized in that only positively valued portions of said respective current are conducted through said energy storage means (C3) and only negatively valued portions of said respective current are conducted through said discharge path (Q1,Q2).

13. The system of claim 6, wherein each of said directing means comprises:

a current discharge path (Q1,Q2);

first means (D2,D3) for conducting positively valued portions of said respective current through said energy storage means (C3) and for blocking negatively valued portions of said respective current from flowing through said energy storage means; and,

second means (D3,D2) for conducting negatively valued portions of said respective current through said current discharge path (Q1,Q2) and for blocking positively valued portions of said respective current from flowing through said current discharge path.

14. The system of claim 11, characterized in that both said diverting means comprise a first semiconductor switch (Q2) defining one of said discharge paths, four similarly poled diodes (D1-D4) and a second semiconductor switch (Q1) defining another of said discharge paths, all coupled in series between two sources of ground potential.

15. The system of claim 14, characterized in that said first semiconductor switch (Q2) has an emitter-collector junction and said second semiconductor switch (Q1) has a collector-emitter junction, each poled similarly to said diodes (D1-D4).

16. A deflection system, comprising:

a plurality of windings (W2a,W2b) of opposite polarity transformer coupled to a source (12) of a first deflection current; respective inductances (L1,L2) coupled to said transformer coupled windings;





respective energy storage means (C1,C2) coupled to said inductances (L1,L2) and charged oppositely by respective currents flowing through said windings;

further energy storage means (C3) coupled to said respective energy storage means (C1,C2);

a deflection yoke (LV) for conducting a second deflection current driven by said further energy storage means (C3);

respective switching means (Q1,Q2) coupled to said respective energy storage means (C1,C2) for controlling respective conduction paths between said respective energy storage means and said further energy storage means (C3) to transfer respective quantities of energy; and,

means (14) for controlling said respective switching means.

17. The system of claim 16, characterized in that said windings (W2a,W2b) are coupled at a junction, and said junction is coupled to ground.

18. The system of claim 16, characterized in that said windings (W2a,W2b) are different parts of a substantially centertapped winding, said centertap (16) being coupled to ground.

19. The system of claim 16 or 17, characterized in that said respective inductances and respective energy storage means comprise an inductor (L1,L2) coupled between each of said windings (W2a,W2b) and a capacitor (C1,C2).

20. The system of claim 16 or 19, characterized in that each of said respective switching means comprises:

a switch (Q1,Q2) responsive to said controlling means (14);

a first diode (D1,D4) coupled to said switch (Q1,Q2) and coupled to said respective energy storage means (C1,C2); and,

a second diode (D2,D3) coupled to said respective energy storage means (L1,L2), coupled to said first diode (D1,D4) and coupled to said further energy storage means (C3).





21. A deflection system, comprising:
first (W2a) and second (W2b) windings transformer coupled to a source (12) of a first deflection current;
first (Q1) and second (Q2) switching means respectively coupled to said first and second windings and coupled together at a first junction (D2,D3);
means (22) for developing a control voltage coupled to said first junction;
a deflection yoke (LV) coupled to said control voltage developing means(22); and,
means (14) for controlling said first and second switching means (Q1,Q2) to modulate said control voltage for generating a second deflection current in said deflection yoke (LV).

22. The system of claim 21, characterized in that said first (W2a) and second (W2b) windings are coupled together at a second junction (ground), and said second junction is coupled to ground.

23. The system of claim 21, characterized by:
first (L1) and second (L2) inductances respectively coupled to said transformer coupled windings (W2a,W2b); and,
first (C1) and second (C2) energy storage means respectively coupled to said first and second inductances and to said first (Q1) and second (Q2) switching means, and charged oppositely by respective currents flowing through said windings.

24. A deflection system, comprising:
first (W2a) and second (W2b) windings transformer coupled to a source (12) of a first deflection current, said first and second windings being coupled together at a junction (ground);
first (Q1) and second (Q2) switching means respectively coupled to said first and second windings;
means (22) for developing a control voltage respectively coupled to said first and second switching means; characterized in that said junction being coupled to ground;





a deflection yoke (LV) coupled to said control voltage developing means (22); and,

means (C4) for controlling said first and second switching means to modulate said control voltage for generating a second deflection current in said deflection yoke.

25. The system of claim 24, characterized in that said windings (W2a,W2b) are different parts of a substantially centertapped winding.

26. The system of claim 24, characterized by:

first (L1) and second (L2) inductances respectively coupled to said transformer coupled windings (W2a,W2b); and,

first (C1) and second (C2) energy storage means respectively coupled to said first and second inductances and to said first (Q1) and second (Q2) switching means, and charged oppositely by respective currents flowing through said windings.

27. The system of claim 21, 23, 26 or 28, characterized in that each of said first (Q1) and second (Q2) switching means comprises:

a switch (Q1,Q2) responsive to said controlling means (C4);

a first diode (D1,D4) coupled to said switch (Q1,Q2) and coupled to said respective energy storage means (C1,C2); and,

a second diode (D2,D3) coupled to said respective energy storage means (C1,C2), coupled to said first diode (D1,D4) and coupled to said control voltage developing means (22).

28. The system of claim 27, characterized in that said first (W2a) and second (W2b) windings are coupled together at a second junction, and said second junction is coupled to ground.

29. A vertical deflection system, comprising:

first means (T1) for generating first and second currents modulated at a horizontal rate;





second means (D2,D3) for generating a third current indicative of a difference between said first and second modulated horizontal rate currents; and,

means (LV) for integrating said third current to generate a vertical deflection current in a vertical deflection yoke, characterized by

a pincushion transformer (T2) having a first winding (W3) capacitively coupled to said integrating means and a second winding (W4) forming part of a horizontal rate resonant circuit coupled in series with said vertical deflection yoke (LV).



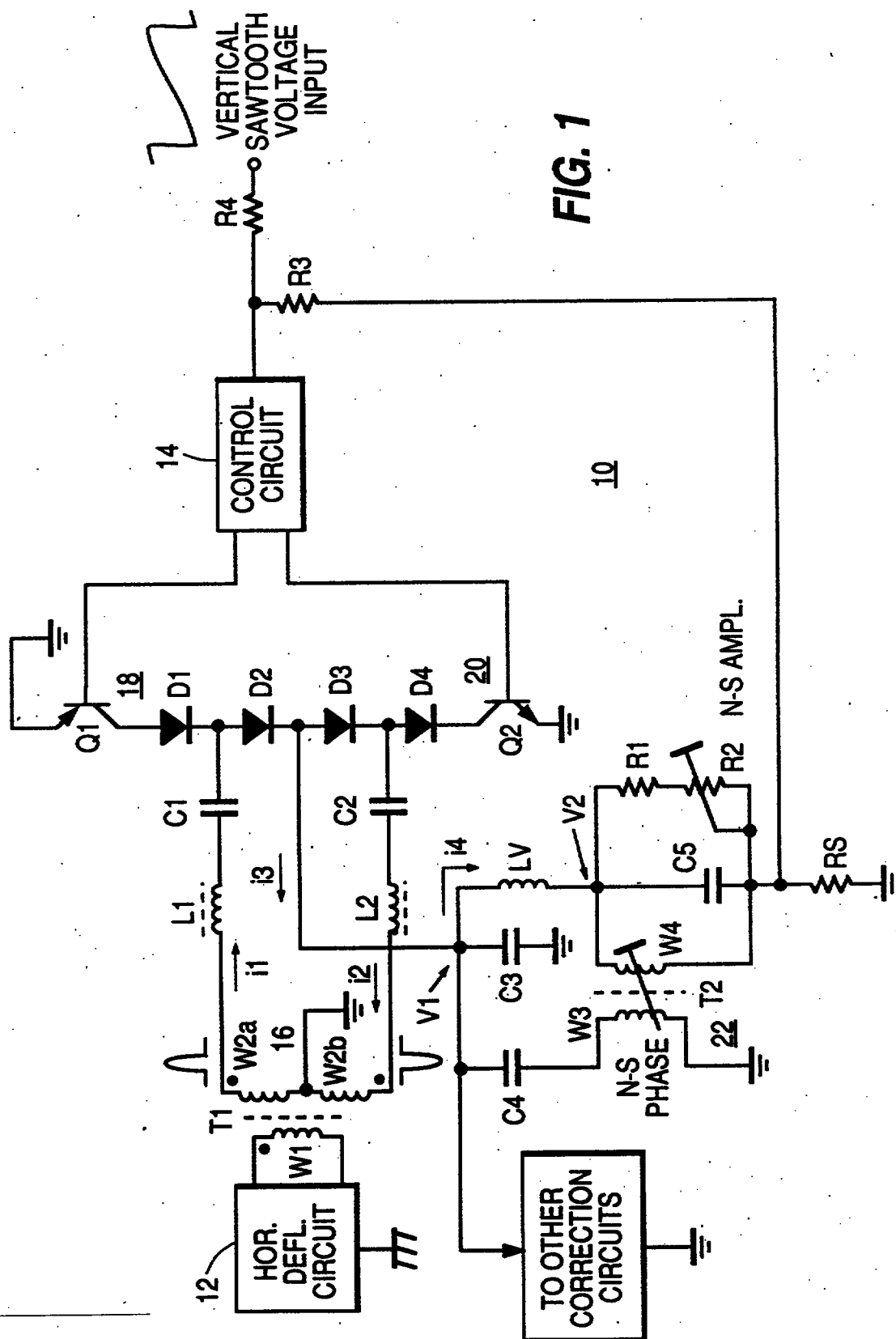
RASTER CORRECTED VERTICAL DEFLECTION CIRCUIT
ABSTRACT

Two windings (W2a,W2b) of a flyback transformer (T1) in a horizontal deflection circuit are inductively coupled with opposite polarity to a source of horizontal rate retrace pulses (12). The windings have a common junction coupled to ground. A circuit (L1,C1,L2,C2) energized by the retrace pulses generates modulated currents of opposite polarity. Conduction of each current is controlled by a switch circuit (18,20) including a semiconductor switch (Q1,Q2) and two diodes (D1-D4). The switch circuits are coupled to one another at a junction, and the junction is coupled to an energy storage capacitance (C3). One of the diodes conducts positively valued portions of the respective current through the energy storage capacitance and the other of the diodes conducts negatively valued portions of the respective current through the semiconductor switch. Each semiconductor switch is a current discharge path. The energy storage capacitance is responsive to the currents for developing a vertical deflection voltage in phase with the currents at the horizontal rate for driving a vertical deflection current in a vertical deflection yoke (LV). The vertical deflection current is related to the difference in amplitude between positively valued portions of the currents. A North-South pincushion correction current in phase with the horizontal deflection is generated by integration of the vertical deflection voltage (V1) in the vertical deflection yoke. A North-South pincushion transformer (T2) has a first winding capacitively coupled to the energy storage capacitance (C3) and a second winding (W4) forming part of a horizontal rate resonant circuit coupled in series with the vertical deflection yoke (LV).

FIG.1

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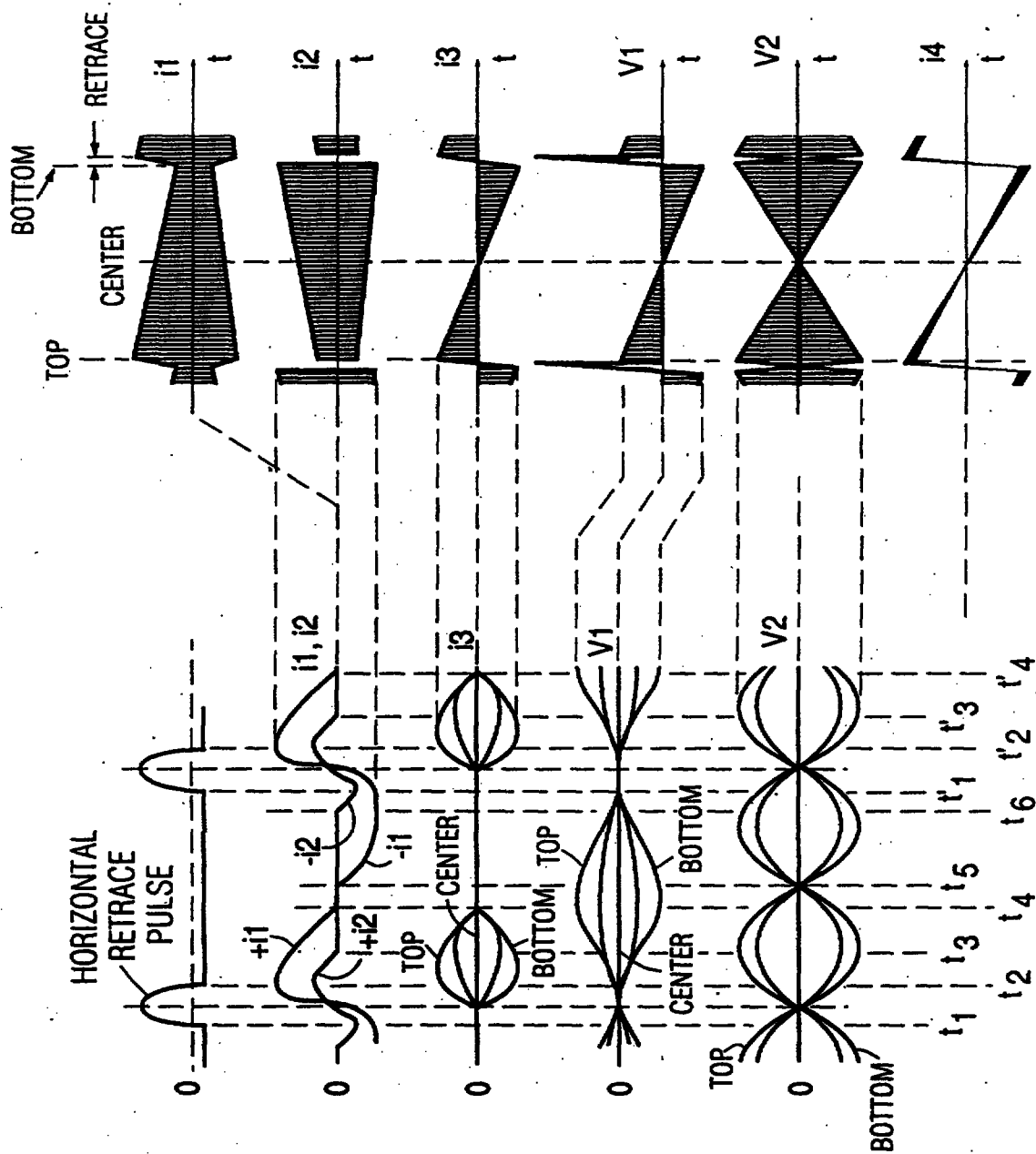


FIG. 2(a)

FIG. 2(b)

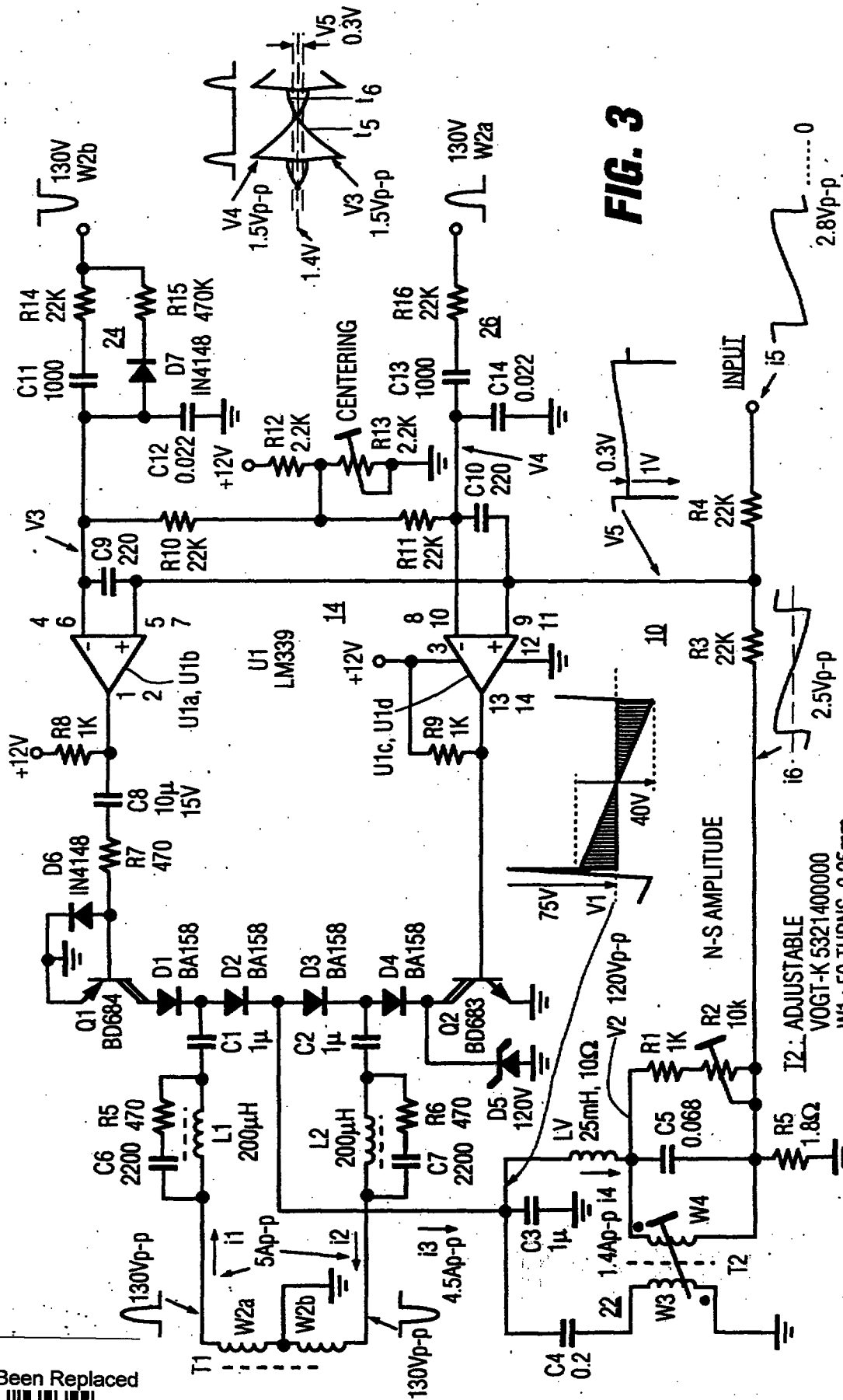
FIG. 2(c)

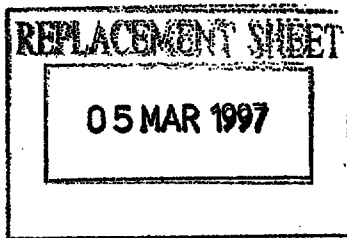
FIG. 2(d)

FIG. 2(e)

FIG. 2(f)







REPLACEMENT SHEETS		SG
☒ Description	: paged 1 to paged 13	13
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RASTER CORRECTED VERTICAL DEFLECTION CIRCUIT

This invention relates generally to the field of vertical deflection circuits, and in particular, to the field of switched vertical deflection circuits.

New generations of color television picture tube-yoke combinations may require North-South pincushion correction. A further requirement can be DC coupling between a vertical deflection amplifier and the deflection yoke, for example when producing a flicker-free AA-BB display. Each field is scanned twice, consecutively, at twice the normal scanning rate, in such AA-BB displays. It is therefore desirable to have a DC coupled vertical deflection circuit producing vertically modulated horizontal rate waveforms for applying to a simple North-South pincushion correction circuit.

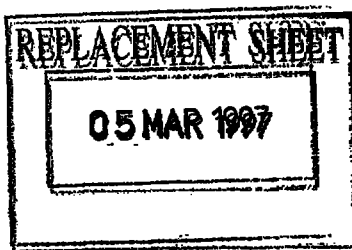
Some of these characteristics suggest that a switched vertical deflection circuit may be appropriate. However, switched vertical deflection circuits can have the following disadvantages:

A first kind of switched vertical circuit is the synchronous switched vertical deflection circuit, often referred to as an SSVD, which employs two thyristors. The thyristors are turned on at modulated instants during the horizontal retrace period. The use of fast thyristors can require a complex control circuit, which can be too expensive. Examples of SSVD circuits are shown in the following U. S. Patents: 4,041,354; 4,079,293; 4,096,415; 4,117,380; and, 4,338,549.

A second kind of switched vertical circuit is the switched mode vertical deflection circuit, often referred to as an SMVD, which employs two switching transistors. The transistors are turned on at modulated instants during the horizontal trace period. This produces a strong phase modulation of the horizontal rate waveforms, which therefore cannot be employed for North-South raster correction. An example of an SMVD circuit is shown in U. S. Patent No. 4,174,493.

A third kind of switched vertical circuit is the single switch vertical deflection circuit, which employs either a thyristor or a transistor switch with antiparallel diode. The phase changes from

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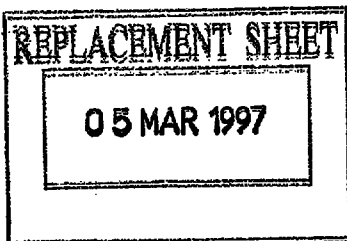


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horizontal retrace to horizontal trace, from top to bottom. Examples of this third kind of switched vertical circuit are shown in the following U. S. Patents: 4,296,360; 4,544,864; and, (substitute patent number of serial number 515,901, filed April 27, 1990, and allowed). Accordingly, North-South raster correction cannot be obtained.

Moreover, and to further disadvantage, the three circuits described above each require a picture tube protection circuit which shuts down the receiver when one drive signal of the switches is missing, to avoid damage to the picture tube from excessive DC current.

It is an inventive arrangement to provide a new switched vertical deflection system for directly converting horizontal energy into vertical deflection current, wherein a vertically modulated horizontal sawtooth voltage across a vertical deflection yoke can provide North-South pincushion correction. First and second windings are inductively coupled with opposite polarity to a source of horizontal rate retrace pulses from a horizontal deflection circuit. The windings can form part of a horizontal flyback transformer in a horizontal deflection system, operating at a horizontal rate. A circuit energized by the retrace pulses generates modulated currents of opposite polarity. The modulated current generating circuit comprises respective switching networks for directing positively and negatively valued portions of the currents along different paths. The negatively valued portions of the currents are conducted through switches along discharge paths to ground. Modulated quantities of the positively valued portions of the currents are conducted along charging paths through an energy storage device. The energy storage device is responsive to the currents and develops a vertical deflection voltage in phase with the currents for driving a vertical deflection current in a vertical deflection yoke. The vertical deflection voltage reflects a net average charge resulting from charging by the oppositely directed currents. The net average charge is determined by subtracting the positively valued part of one of the currents from the positively valued part of the other current. The vertical deflection voltage is



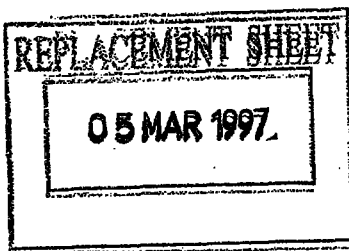
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not subject to phase modulation, as in the prior art switched vertical systems described above. Accordingly, a North-South pincushion correction current in phase with the horizontal deflection circuit is generated by integration of the vertical deflection voltage in the vertical deflection yoke. Horizontal rate waveforms phased correctly for producing North-South raster correction, and for other correction circuits, are provided.

It is another inventive arrangement to provide a switched vertical deflection system which can provide enhanced North-South pincushion correction by use of a pincushion transformer. A pincushion transformer has a first winding capacitively coupled to the energy storage device and a second winding forming part of a horizontal rate resonant circuit coupled in series with the vertical deflection yoke.

It is still another inventive arrangement to obviate the need for shutting down the receiver when one drive signal of the switches in a switched vertical deflection system is missing, to avoid damage to the picture tube from excessive DC current. In switched vertical deflection systems in the prior art, the windings of the flyback transformer are DC coupled in series with inductors, which are in turn DC coupled to the switches, or switching networks, and to an energy storage device. In the switched vertical deflection systems taught herein, each inductor can be AC coupled to the respective switch, or switching network, and to the energy storage device by a capacitor.

It is yet another inventive arrangement to provide a plurality of advantageous topological features, which contribute to improved operation of switched vertical deflection systems. The windings of the flyback transformer coupled to the source of horizontal retrace pulses are coupled together at a first junction, and the first junction is coupled to ground. The windings can be separate, substantially identical windings. Alternatively, the windings can be different halves of a substantially centertapped winding, in which case the center tap is coupled to ground. First and second switches, or switching networks, are respectively coupled to the first and second windings and coupled together at a second junction. The



energy storage device for developing the vertical deflection voltage is coupled to the second junction. Respective energy storage devices are coupled to the inductances, which are themselves coupled to the respective windings. The energy storage devices are charged oppositely by respective currents flowing through the windings. The energy storage devices are coupled to the respective switches, or switching networks, providing an access for the current modulating control. The energy storage devices can be embodied as capacitors, which also provide the AC coupling described above.

In the Drawings:

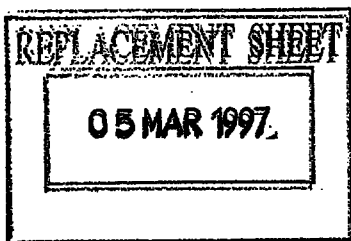
FIGURE 1 is a circuit diagram, in partial block form, showing a switched vertical deflection circuit according to an inventive arrangement.

FIGURES 2(a)-2(f) are waveforms useful for explaining the operation of the circuit shown in FIGURE 1.

FIGURE 3 is an illustrative vertical deflection circuit in according to an inventive arrangement.

A switched vertical deflection system 10 is shown Figure 1. A horizontal deflection circuit 12, as known in the prior art, is coupled to a winding W1 of flyback transformer T1. Horizontal deflection circuit may operate at a horizontal scanning frequency of f_H , as for conventional interlaced scanning. Scanning at f_H , for example, can correspond to a rate of approximately 15,750 Hz for NTSC interlaced standards. Horizontal deflection circuit 12 may also operate at a multiple thereof, for example $2f_H$, as for progressive noninterlaced scanning. The scanning rates f_H and $2f_H$ will have different values for PAL and SECAM standards.

Flyback transformer T1 has another winding W2, which is inductively coupled to winding W1. Winding W2 has a centertap 16 coupled to ground. The center tap 16 defines two windings, or winding portions, W2a and W2b of opposite polarity relative to one another. Accordingly, positive retrace pulses are generated by winding W2a and negative retrace pulses are generated by winding W2b. Windings W2a and W2b receive energy from the horizontal deflection system by means of the retrace pulses. The energy is made available to the switched vertical deflection system 10 for



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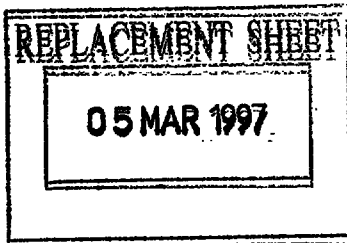
generating a vertical deflection current in a vertical deflection yoke.

Briefly, and as will be explained in more detail below, the flyback transformer T1 supplies energy from the horizontal deflection system to the vertical yoke by means of currents i_1 and i_2 which follow respective conduction paths between the respective windings W2a and W2b and the storage capacitor C3. Current i_3 , which is the difference of currents i_1 and i_2 , charges storage capacitor C3 at the horizontal rate. Storage capacitor C3 thereby develops a vertical deflection voltage V1. Capacitor C3 discharges into a deflection yoke Lv to produce a vertical deflection current i_4 . A feedback loop including resistor R3 linearizes and stabilizes the deflection circuit. A control circuit 14 generates the base drive signals for switching transistors Q1 and Q2.

The respective conduction paths for currents i_1 and i_2 include: respective storage coils, or inductors, L1 and L2; respective coupling capacitors, or energy storage devices, C1 and C2; and, respective diodes D2 and D3. Diodes D2 and D3 are polarized for conduction of horizontal retrace current.

Diodes D1 and D2 and transistor Q1 form a first switch, or switching network, 18, operatively associated with current i_1 . Diodes D3 and D4 and transistor Q2 form a second switch, or switching network, 20, operatively associated with current i_2 . Diodes D1 and D4 also serve to isolate transistors Q1 and Q2 from reverse voltages appearing at the collectors during horizontal retrace. Switching networks 18 and 20 are responsive to the control circuit 14, the operation of which is explained in more detail in connection with FIGURE 3.

When transistor Q1 is nonconductive, capacitor C1 charges negatively at the junction of diodes D1 and D2, responsive to the positive retrace pulses on winding W2a. When transistor Q2 is nonconductive, capacitor C2 charges positively at the junction of diodes D3 and D4, responsive to the negative retrace pulses on winding W2b. Capacitors C1 and C2 charge to the peak horizontal retrace voltage applied by windings W2a and W2b respectively. When transistors Q1 and Q2 are nonconductive, current i_3 does not



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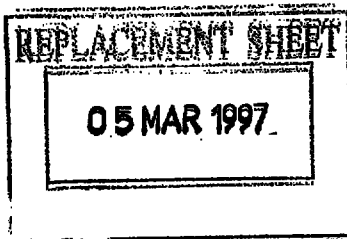
flow, so that capacitor C3 does not receive any charge. The vertical deflection current i_4 in vertical deflection yoke L_v remains zero.

The positive currents i_1 and i_2 are controlled by the amount of discharge of capacitors C1 and C2, respectively. The amount of discharge of capacitors C1 and C2 is controlled by modulating the conduction time of transistors Q1 and Q2, respectively. Transistors Q1 and Q2 are switched on at varying times within the interval t_5 - t_6 in FIGURES 2(a) - 2(f), as explained in more detail below. The transistors Q1 and Q2 are turned off during the horizontal retrace interval when diodes D1 and D4 are reverse biased by horizontal retrace pulses.

Briefly, at the start of vertical trace, transistor Q1 is turned on at time t_5 and transistor Q2 is turned on at time t_6 . This causes a large positive current i_1 to flow until time t_4' , and a small positive current i_2 to flow until time t_3' . The current flow of currents i_1 and i_2 is due to the energy stored during horizontal retrace in coils L1 and L2, respectively. The instant at which transistor Q1 is turned on is progressively retarded from time t_5 to time t_6 during vertical trace. During that same interval, the instant at which transistor Q2 is turned on is progressively advanced from time t_6 to time t_5 . This causes a decreasing amplitude of current i_1 and an increasing amplitude of current i_2 , as shown in the right hand parts of FIGURE 2(b).

A yoke current is obtained when capacitors C1 and C2 are discharged by transistors Q1 and Q2, respectively. A positive yoke current is obtained when transistor Q1 is in saturation. The positive retrace voltage generates a charge current flowing through inductor L1, capacitor C1, diode D2 and capacitor C3 to ground, resulting in a positive voltage across capacitor C3. When the charge current falls to zero during the first half of the horizontal trace interval, then the charge, or voltage, across capacitor C1 causes diode D2 to become back biased and diode D1 to become forward biased. Capacitor C1 starts to discharge through diode D1 and saturated transistor Q1 during the second half of the horizontal trace time.

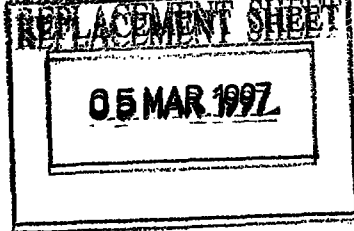
A negative yoke current is obtained when transistor Q2 is in saturation. The negative retrace voltage generates a charge current



flowing from ground through capacitor C3, diode D3, capacitor C2 and inductor L2, resulting in a negative voltage across capacitor C3. When the charge current falls to zero during the first half of the horizontal trace interval, then the charge, or voltage, across capacitor C2 causes diode D3 to become back biased and diode D4 to become forward biased. Capacitor C2 starts to discharge through diode D4 and saturated transistor Q1 during the second half of the horizontal trace time.

Thus, the amount and polarity of the deflection current i_4 is determined by the amount of discharge current flowing through transistors Q1 and Q2. Transistors Q1 and Q2 may operate in a switched manner, or even in class A, providing a current sink or current source. Bipolar transistors Q1 and Q2 as shown in FIGURE 1 may be replaced by any other device providing a controllable discharge path. In the following description, transistors Q1 and Q2 operate in a switched manner to minimize dissipation.

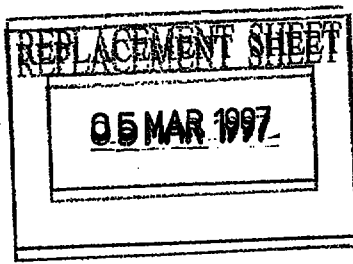
A number of waveforms useful in explaining operation of the switched vertical deflection system 10 are shown in the various parts of FIGURE 2. The left hand side of each part in FIGURE 2 shows horizontal rate waveforms. The right hand side of each part shows the corresponding vertical rate waveforms. The time lines of the vertical rate waveforms are marked with respect to the TOP, CENTER and BOTTOM of the display, or field. The vertical retrace interval is between the BOTTOM of a field and the TOP of the next successive field. FIGURE 2(a) shows only horizontal rate retrace pulses. FIGURE 2(b) shows separate vertical rate waveforms for currents i_1 and i_2 , shown together at the horizontal rate. The upper parts of each of the vertical rate waveforms for currents i_1 and i_2 show the positively valued portions of currents i_1 and i_2 respectively, flowing through diodes D2 and D3 respectively. The lower parts of each of the vertical rate waveforms for currents i_1 and i_2 show the negatively valued portions of currents i_1 and i_2 respectively, flowing through transistors Q1 and Q2 respectively. FIGURE 2(c) shows current i_3 . FIGURE 2(d) shows voltage V1. FIGURE 2(e) shows voltage V2. FIGURE 2(f) shows only the vertical rate current i_4 .



In operation, deflection current i_4 starts with positive peak amplitude at the start, or TOP, of the vertical trace. At the TOP, transistor Q1 is switched into saturation at time t_5 and substantially discharges C1. This causes a large amplitude of charge current i_1 flowing through diode D2. Stored horizontal retrace energy in coil L1 causes positive current i_1 to flow until time t_4' . Transistor Q2 is turned on at time t_6 producing a small discharge current i_2 and consequently a small charge current i_2 which flows through diode D3 until time t_3' . The vertical yoke is driven by current i_3 which is the difference of positively valued portion of current i_1 minus the positively valued portion of current i_2 . Current i_3 , the waveform shown in FIGURE 2(c), charges capacitor C3 producing voltage V1, the waveform shown in FIGURE 2(d). Voltage V1 increases until the amplitude of current i_3 becomes smaller than the amplitude of the deflection current i_4 .

Deflection current i_4 , the waveform shown in FIGURE 2(f), is obtained by discharging capacitor C3 through the vertical deflection yoke L_v and current sampling resistor R_s . The deflection yoke L_v integrates the horizontal rate voltage across capacitor C3 to a substantially sawtooth current at the vertical rate. Due to the large inductance of the deflection winding, the discharge current cannot follow the roughly triangular horizontal rate voltage across capacitor C3. Consequently, the current i_4 through the deflection winding results from the average of the voltage across the capacitor C3. Therefore, the deflection winding acts as a current sink to discharge capacitor C3. The parallel resonant frequency of the capacitor C3 and the deflection winding determines the vertical retrace interval. The sawtooth shaped voltage V1, as integrated by the high inductance of the deflection yoke L_v , produces at least some parabolic North-South raster correction current. A deflection current sample across sampling resistor R_s is fed back to the control circuit 14 to linearize the operation of the deflection circuit.

During the first half of vertical trace, that is from the TOP to the CENTER, the turn on time of transistor Q1 is progressively retarded from time t_5 , toward time t_6 . During the same interval,

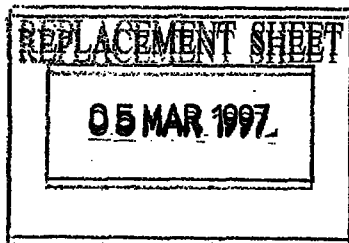


the turn on time of transistor Q2 is progressively advanced from time t_6 , toward time t_5 . This causes a progressively decreasing amplitude of current i_1 and a progressively increasing amplitude of current i_2 . The amplitude of current i_3 , which is the difference of the positively valued portion of current i_1 minus the positively valued portion of current i_2 , also progressively decreases. As a result, the amplitudes of voltage V_1 and vertical deflection current i_4 also progressively decrease. The amplitudes of the positively valued portions of currents i_1 and i_2 are equal at the CENTER of vertical trace. Consequently, current i_3 , voltage V_1 and current i_4 are zero. Current i_1 flows through diode D2 and transistor Q1 and current i_2 flows through diode D3 and transistor Q2.

During the second half of vertical trace, Q1 continues to be turned on progressively retarded from time t_5 , toward time t_6 . Transistor Q2 continues to be turned on progressively advanced from time t_6 , toward time t_5 . This causes a further progressive decrease of current i_1 and a further progressive increase of current i_2 . As a result, current i_3 , voltage V_1 and current i_4 progressively increase in the negative direction.

Vertical retrace starts when the turn on time of transistor Q1 is quickly shifted from back from time t_6 to time t_5 , and transistor Q2 is held in cut off. This causes a retrace resonance of one half cycle between vertical deflection yoke L_v and capacitor C3, causing a rapid and loss free reversal of the deflection current i_4 . As vertical deflection current i_4 changes its direction rapidly, a large but narrow retrace voltage pulse is produced, evident in the righthand portion of waveform 2(d) showing voltage V_1 . As explained above, the turn on times of transistors Q1 and Q2 are modulated during the interval from time t_5 to time t_6 to obtain a modulated current i_3 , which starts to flow at the CENTER of horizontal retrace and ends at time t_4' . Transistors Q1 and Q2 are turned off during the second half of retrace when diodes D1 and D4 are non-conductive.

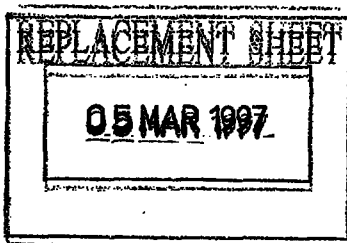
The circuit requires some overlap of currents i_1 and i_2 to avoid deflection current distortions or discontinuities. This is illustrated by vertical rate waveforms of currents i_1 and i_2 .



Overlap current is highest at the CENTER of the vertical trace when current i_3 is zero. The overlap current decreases from the CENTER toward TOP and BOTTOM. The overlap current can be determined by subtracting current i_3 from current i_1 during the first half of trace, and by subtracting current i_3 from current i_2 during the second half of trace.

The time duration of the envelope of current i_3 is not modulated because current i_3 is formed by the difference of the positively valued portions of currents i_1 and i_2 . This causes horizontal sawtooth voltage V_1 to be in phase with the horizontal retrace pulses. The peaks of voltage V_1 appear always at time t_4 , where current i_3 decreases to zero. This allows a North-South pincushion correction circuit 22 to be driven by voltage V_1 , as shown in FIGURE 1. A pincushion transformer T2 has a primary winding W3 coupled to capacitor C3 through capacitor C4. A secondary winding W4 forms a line frequency resonant circuit with a capacitor C5, producing the vertically modulated sine wave voltage V_2 , shown in FIGURE 2(e), at the low side of the deflection yoke L_v . Voltage V_2 generates a cosine wave (90 degrees phase shifted) raster correction current in vertical deflection yoke L_v as it is required for raster correction. In other words, the horizontal rate sawtooth voltage V_1 is applied to the primary winding W3 of transformer T2 through capacitor C4. The secondary winding W4 forms a horizontal rate resonant circuit together with capacitor C5 to produce the modulated sine wave voltage V_2 . Sine wave voltage V_2 injects a cosine current into the yoke winding, as required for North-South raster correction. The zero-crossings of the horizontal rate envelope of voltage V_2 are not modulated. Further, the zero-crossing is always at the center of the horizontal retrace interval. Voltage V_1 , being in phase with horizontal rate waveforms, may be employed by other circuits for correcting moustache and gullwing distortion and for dynamic convergence.

Vertical deflection deflection yoke L_v is DC coupled to switching transistors Q1 and Q2 and to the control circuit 14. This permits the use of this circuit in receivers with AA-BB display or other features requiring dynamic raster shift. Flyback transformer



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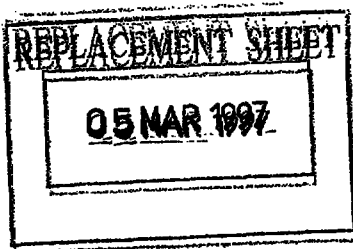
winding W2 is AC coupled to the vertical deflection circuit by capacitors C1 and C2. The AC coupling allows operation of the deflection circuit without a picture tube protection circuit. The absence of base drive for either or both of transistors Q1 and Q2 does not produce excessive DC current in vertical deflection yoke Lv, such as may damage the picture tube.

The value of capacitor C3 is matched to the inductance of vertical deflection yoke Lv to produce a correct vertical retrace time. Further, voltage V1 should decrease to about ground potential at time t1'. The averaged horizontal retrace voltage, or the trace voltage across winding sections W2a and W2b, should be twice the required peak voltage across vertical deflection yoke Lv. Inductors L1 and L2, and capacitors C1 and C2 are equal in value. The component values are selected to obtain the necessary amplitude and shape of currents i1 and i2.

FIGURE 3 shows a more complete circuit schematic for the switched vertical deflection circuit 10, adapted for operation with a Videocolor 110° SP picture tube type A68 EAU00X01. The various operational waveforms are similar to those shown in FIGURE 2. Peak to peak values of currents and voltages are noted directly, as are some additional waveforms.

The control circuit employs a quad voltage comparator U1. Each output transistor Q1, Q2 is driven by two comparators U1a, U1b or U1c, U1d connected in parallel, for obtaining adequate base drive. Nonlinear horizontal ramp voltage V3 is produced by network 24, including resistor R14, capacitor C11 and capacitor C12. Negative retrace pulses from winding W2b are an input to network 24. Nonlinear horizontal ramp voltage V4 is produced by network 26, including resistor R16, capacitor C13 and capacitor C14. Positive retrace pulses from winding W2a are an input to network 26. Voltage waveforms V3 and V4 are shown in FIGURE 3, upper right. A voltage divider formed by resistor R12 and adjustable resistor R13 provide centering control.

A vertical sawtooth input current i5 is combined with vertical feedback current i6 at the junction of resistors R3 and R4, resulting in vertical drive voltage V5. Vertical drive voltage V5 is compared



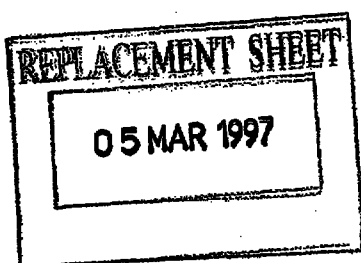
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with each of ramp voltages V3 and V4 for producing transistor switching pulses modulated in the time interval t5-t6. The non-linearity of the horizontal ramp voltages V3 and V4 avoids instabilities during vertical retrace, and in particular, during the sharp negative peak of voltage V5. Without the non-linearity shown, transistor Q1 can turn on too early and produce some ringing at the very TOP of the raster.

The overlapping operation of the output stage, explained above in connection with FIGURES 1 and 2, is obtained by the overlap of the horizontal ramp voltages V3 and V4, clear from the illustration in FIGURE 3. The overlapping is controlled by network 24, wherein resistor R15 and diode D7 charge capacitor C12 negatively, to reduce the natural overlap of ramp voltages V3 and V4. More particularly, network 24 sets the DC level of ramp voltage V3.

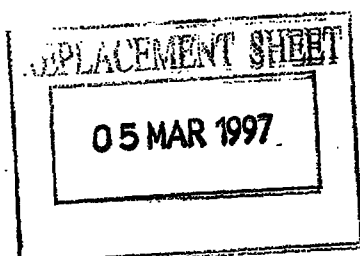
The peak collector voltages on transistors Q1 and Q2 are approximately 70 volts during vertical trace. During vertical retrace, the collector voltage of transistor Q2 increases to approximately 150 volts because capacitor C2 is clamped by diode D3 to the vertical deflection yoke retrace voltage. A Zener diode D5 is connected across transistor Q2 for protection during retrace. The Zener diode D5 limits the collector voltage on transistor Q2 to approximately 120 volts. The peak to peak pincushion correction current in deflection yoke Lv is approximately 100 mA, corresponding to a pincushion distortion of approximately 14%.

The loading of the flyback transformer T1 is symmetrical, in contrast to other switched vertical deflection circuits. This avoids horizontal raster distortion in the East-West direction. No DC power supply is needed. The AC coupling between the flyback transformer and the deflection circuit, provided by capacitors C1 and C2, protects the picture tube against excessive yoke currents in the absence of base drive for transistors Q1 and/or Q2. The circuit may be adapted to different yoke impedances by changing component values. Operation without North-South raster correction can be implemented by omitting transformer T2 and the associated components. The DC yoke coupling allows $2f_H$, 100 Hz field



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sequential (AA-BB) operation. The components determining the frequency must be changed for operation at $2f_H$ and 100 Hz.

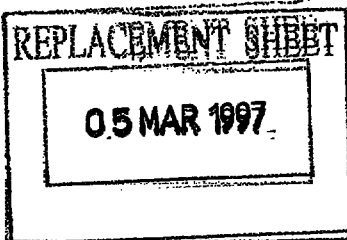


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CLAIMS:

1. A switched vertical deflection system, comprising:
first (W2a) and second (W2b) windings inductively coupled with opposite polarity to a source of horizontal rate retrace pulses from a horizontal deflection circuit (12);
means (L1,L2) energized by said retrace pulses for generating modulated currents of opposite polarity;
a vertical deflection yoke (LV); and,
energy storage means (C3) responsive to said currents for developing a vertical deflection voltage (V1) in phase with said currents for driving a vertical deflection current (i4) in said vertical yoke, characterized by a North-South pincushion correction current in phase with said horizontal deflection circuit (12) being generated by integration of said vertical deflection voltage (V1) in said vertical deflection yoke (LV).
2. The system of claim 1, characterized in that said vertical deflection voltage (V1) is related to an amplitude difference between said currents.
3. The system of claim 1, characterized in that said vertical deflection current (i4) is related to an amplitude difference between positively valued portions of said currents.
4. The system of claim 1, characterized in that said windings (W2a,W2b) are AC coupled to said modulated current generating means (L1,L2) and to said energy storage means (C3).
5. The system of claim 1, characterized in that said modulated current generating means comprises respective means (Q1,Q2) for diverting negatively valued portions of said currents from flowing through said energy storage means (C3).





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6. The system of claim 1, characterized in that said modulated current generating means (L1,L2) comprises respective means (Q1,Q2) for directing positively and negatively valued portions of said currents along different paths.

7. The system of claim 6, characterized in that each of said directing means comprises a switch (Q1,Q2) and two diodes (D1,D2; D3,D4), one of said diodes (D1,D2) conducting positively valued portions of said respective current through said energy storage means (C3) and the other of said diodes (D3,D4) conducting negatively valued portions of said respective current through said switch (Q1,Q2).

8. The system of claim 7, characterized in that said diodes (D1,D2,D3,D4) are coupled in series at a junction (D2,D3), said positively and negatively valued portions of said respective current being present at said junction.

9. The system of claim 5 or 8, characterized in that said respective directing means (Q1,Q2) are coupled to one another at a second junction (ground), and said second junction is coupled to said energy storage means (C3).

10. The system of claim 1 or 9, characterized by a pincushion transformer (T2) having a first winding (W3) capacitively coupled to said energy storage means (C3) and a second winding (W4) forming part of a horizontal rate resonant circuit coupled in series with said vertical deflection yoke (LV).

11. The system of claim 6, wherein each of said directing means comprises:

a current discharge path (Q1,Q2);

means for conducting positively valued portions of said respective current through said energy storage means (C3) and for conducting negatively valued portions of said respective current through said current discharge path (Q1,Q2).



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12. The system of claim 11, characterized in that only positively valued portions of said respective current are conducted through said energy storage means (C3) and only negatively valued portions of said respective current are conducted through said discharge path (Q1,Q2).

13. The system of claim 6, wherein each of said directing means comprises:

a current discharge path (Q1,Q2);

first means (D2,D3) for conducting positively valued portions of said respective current through said energy storage means (C3) and for blocking negatively valued portions of said respective current from flowing through said energy storage means; and,

second means (D3,D2) for conducting negatively valued portions of said respective current through said current discharge path (Q1,Q2) and for blocking positively valued portions of said respective current from flowing through said current discharge path.

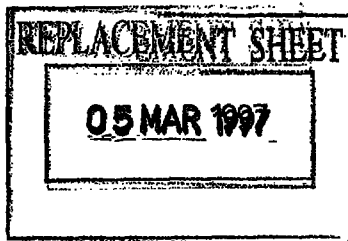
14. The system of claim 11, characterized in that both said diverting means comprise a first semiconductor switch (Q2) defining one of said discharge paths, four similarly poled diodes (D1-D4) and a second semiconductor switch (Q1) defining another of said discharge paths, all coupled in series between two sources of ground potential.

15. The system of claim 14, characterized in that said first semiconductor switch (Q2) has an emitter-collector junction and said second semiconductor switch (Q1) has a collector-emitter junction, each poled similarly to said diodes (D1-D4).

16. A deflection system, comprising:

a plurality of windings (W2a,W2b) of opposite polarity transformer coupled to a source (12) of a first deflection current; respective inductances (L1,L2) coupled to said transformer coupled windings;





respective energy storage means (C1,C2) coupled to said inductances (L1,L2) and charged oppositely by respective currents flowing through said windings;

further energy storage means (C3) coupled to said respective energy storage means (C1,C2);

a deflection yoke (LV) for conducting a second deflection current driven by said further energy storage means (C3);

respective switching means (Q1,Q2) coupled to said respective energy storage means (C1,C2) for controlling respective conduction paths between said respective energy storage means and said further energy storage means (C3) to transfer respective quantities of energy; and,

means (14) for controlling said respective switching means.

17. The system of claim 16, characterized in that said windings (W2a,W2b) are coupled at a junction, and said junction is coupled to ground.

18. The system of claim 16, characterized in that said windings (W2a,W2b) are different parts of a substantially centertapped winding, said centertap (16) being coupled to ground.

19. The system of claim 16 or 17, characterized in that said respective inductances and respective energy storage means comprise an inductor (L1,L2) coupled between each of said windings (W2a,W2b) and a capacitor (C1,C2).

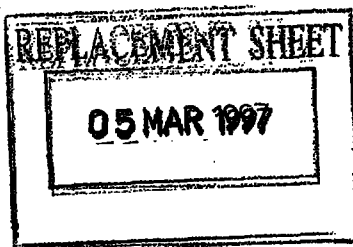
20. The system of claim 16 or 19, characterized in that each of said respective switching means comprises:

a switch (Q1,Q2) responsive to said controlling means (14);

a first diode (D1,D4) coupled to said switch (Q1,Q2) and coupled to said respective energy storage means (C1,C2); and,

a second diode (D2,D3) coupled to said respective energy storage means (L1,L2), coupled to said first diode (D1,D4) and coupled to said further energy storage means (C3).





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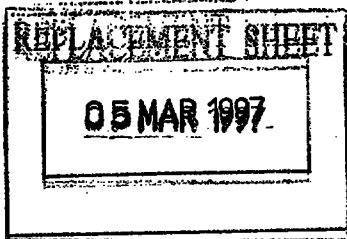
21. A deflection system, comprising:
first (W2a) and second (W2b) windings transformer coupled to a source (12) of a first deflection current;
first (Q1) and second (Q2) switching means respectively coupled to said first and second windings and coupled together at a first junction (D2,D3);
means (22) for developing a control voltage coupled to said first junction;
a deflection yoke (LV) coupled to said control voltage developing means(22); and,
means (14) for controlling said first and second switching means (Q1,Q2) to modulate said control voltage for generating a second deflection current in said deflection yoke (LV).

22. The system of claim 21, characterized in that said first (W2a) and second (W2b) windings are coupled together at a second junction (ground), and said second junction is coupled to ground.

23. The system of claim 21, characterized by:
first (L1) and second (L2) inductances respectively coupled to said transformer coupled windings (W2a,W2b); and,
first (C1) and second (C2) energy storage means respectively coupled to said first and second inductances and to said first (Q1) and second (Q2) switching means, and charged oppositely by respective currents flowing through said windings.

24. A deflection system, comprising:
first (W2a) and second (W2b) windings transformer coupled to a source (12) of a first deflection current, said first and second windings being coupled together at a junction (ground);
first (Q1) and second (Q2) switching means respectively coupled to said first and second windings;
means (22) for developing a control voltage respectively coupled to said first and second switching means; characterized in that said junction being coupled to ground;





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a deflection yoke (LV) coupled to said control voltage developing means (22); and,

means (C4) for controlling said first and second switching means to modulate said control voltage for generating a second deflection current in said deflection yoke.

25. The system of claim 24, characterized in that said windings (W2a,W2b) are different parts of a substantially centertapped winding.

26. The system of claim 24, characterized by:

first (L1) and second (L2) inductances respectively coupled to said transformer coupled windings (W2a,W2b); and,

first (C1) and second (C2) energy storage means respectively coupled to said first and second inductances and to said first (Q1) and second (Q2) switching means, and charged oppositely by respective currents flowing through said windings.

27. The system of claim 21, 23, 26 or 28, characterized in that each of said first (Q1) and second (Q2) switching means comprises:

a switch (Q1,Q2) responsive to said controlling means (C4);

a first diode (D1,D4) coupled to said switch (Q1,Q2) and coupled to said respective energy storage means (C1,C2); and,

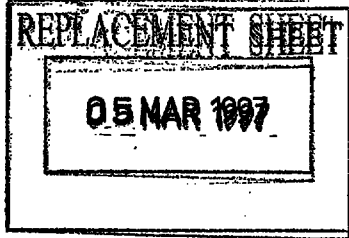
a second diode (D2,D3) coupled to said respective energy storage means (C1,C2), coupled to said first diode (D1,D4) and coupled to said control voltage developing means (22).

28. The system of claim 27, characterized in that said first (W2a) and second (W2b) windings are coupled together at a second junction, and said second junction is coupled to ground.

29. A vertical deflection system, comprising:

first means (T1) for generating first and second currents modulated at a horizontal rate;





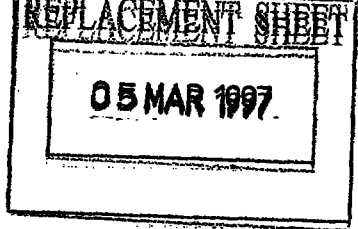
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second means (D2,D3) for generating a third current indicative of a difference between said first and second modulated horizontal rate currents; and,

means (LV) for integrating said third current to generate a vertical deflection current in a vertical deflection yoke, characterized by

a pincushion transformer (T2) having a first winding (W3) capacitively coupled to said integrating means and a second winding (W4) forming part of a horizontal rate resonant circuit coupled in series with said vertical deflection yoke (LV).





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RASTER CORRECTED VERTICAL DEFLECTION CIRCUIT
ABSTRACT

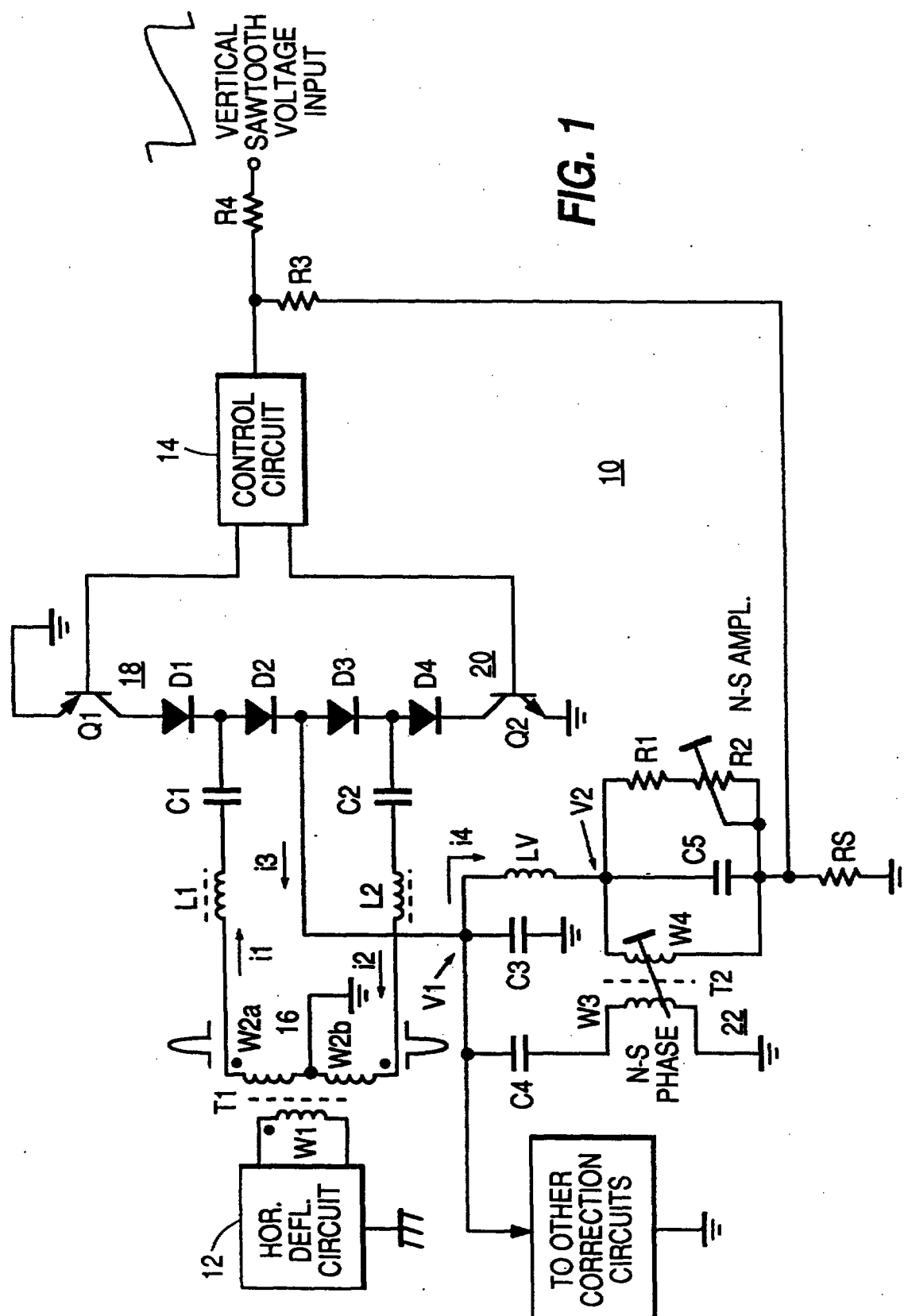
Two windings (W2a,W2b) of a flyback transformer (T1) in a horizontal deflection circuit are inductively coupled with opposite polarity to a source of horizontal rate retrace pulses (12). The windings have a common junction coupled to ground. A circuit (L1,C1,L2,C2) energized by the retrace pulses generates modulated currents of opposite polarity. Conduction of each current is controlled by a switch circuit (18,20) including a semiconductor switch (Q1,Q2) and two diodes (D1-D4). The switch circuits are coupled to one another at a junction, and the junction is coupled to an energy storage capacitance (C3). One of the diodes conducts positively valued portions of the respective current through the energy storage capacitance and the other of the diodes conducts negatively valued portions of the respective current through the semiconductor switch. Each semiconductor switch is a current discharge path. The energy storage capacitance is responsive to the currents for developing a vertical deflection voltage in phase with the currents at the horizontal rate for driving a vertical deflection current in a vertical deflection yoke (LV). The vertical deflection current is related to the difference in amplitude between positively valued portions of the currents. A North-South pincushion correction current in phase with the horizontal deflection is generated by integration of the vertical deflection voltage (V1) in the vertical deflection yoke. A North-South pincushion transformer (T2) has a first winding capacitively coupled to the energy storage capacitance (C3) and a second winding (W4) forming part of a horizontal rate resonant circuit coupled in series with the vertical deflection yoke (LV).

FIG.1



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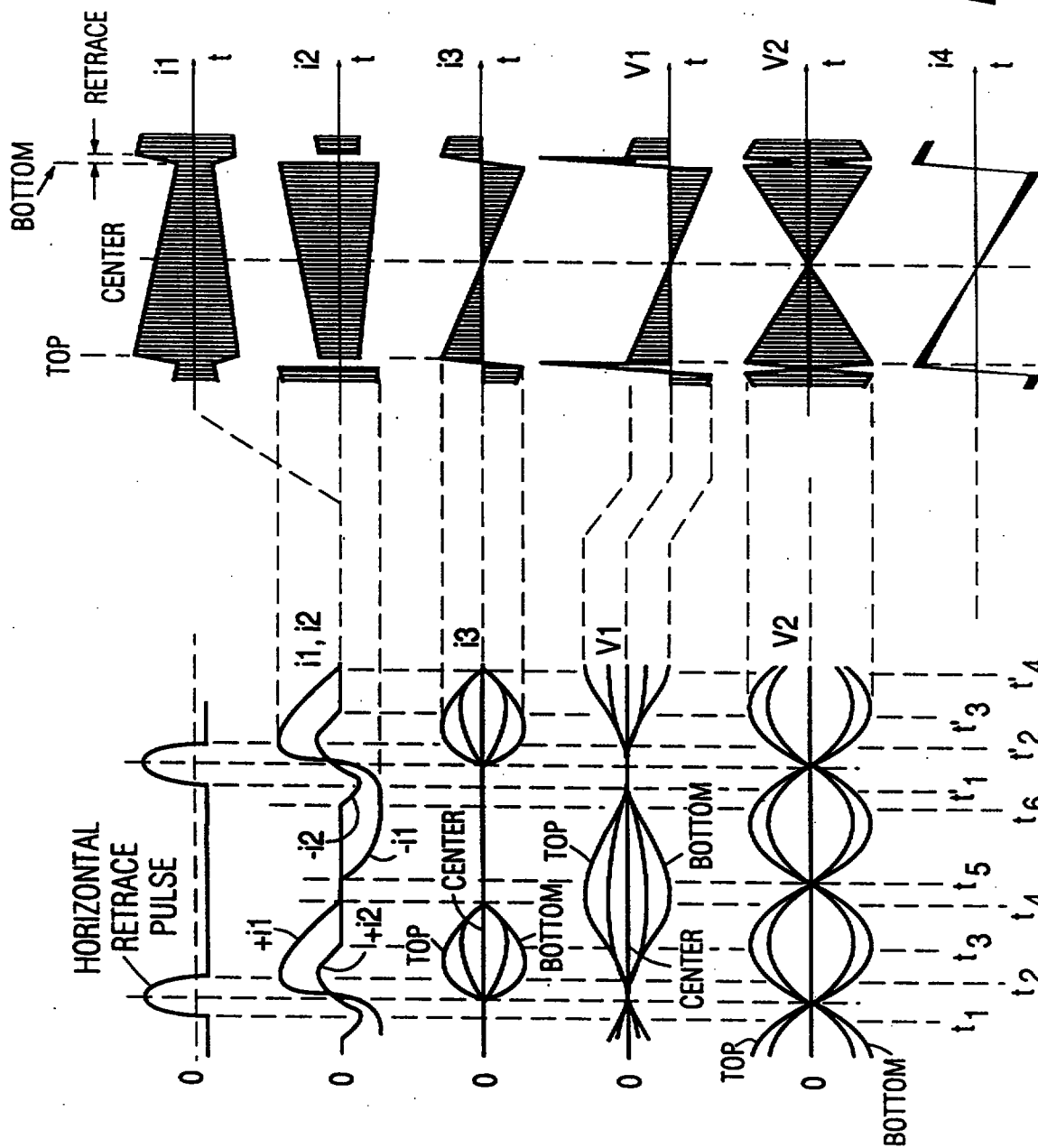


FIG. 2(a)

FIG. 2(b)

FIG. 2(c)

FIG. 2(d)

FIG. 2(e)

FIG. 2(f)

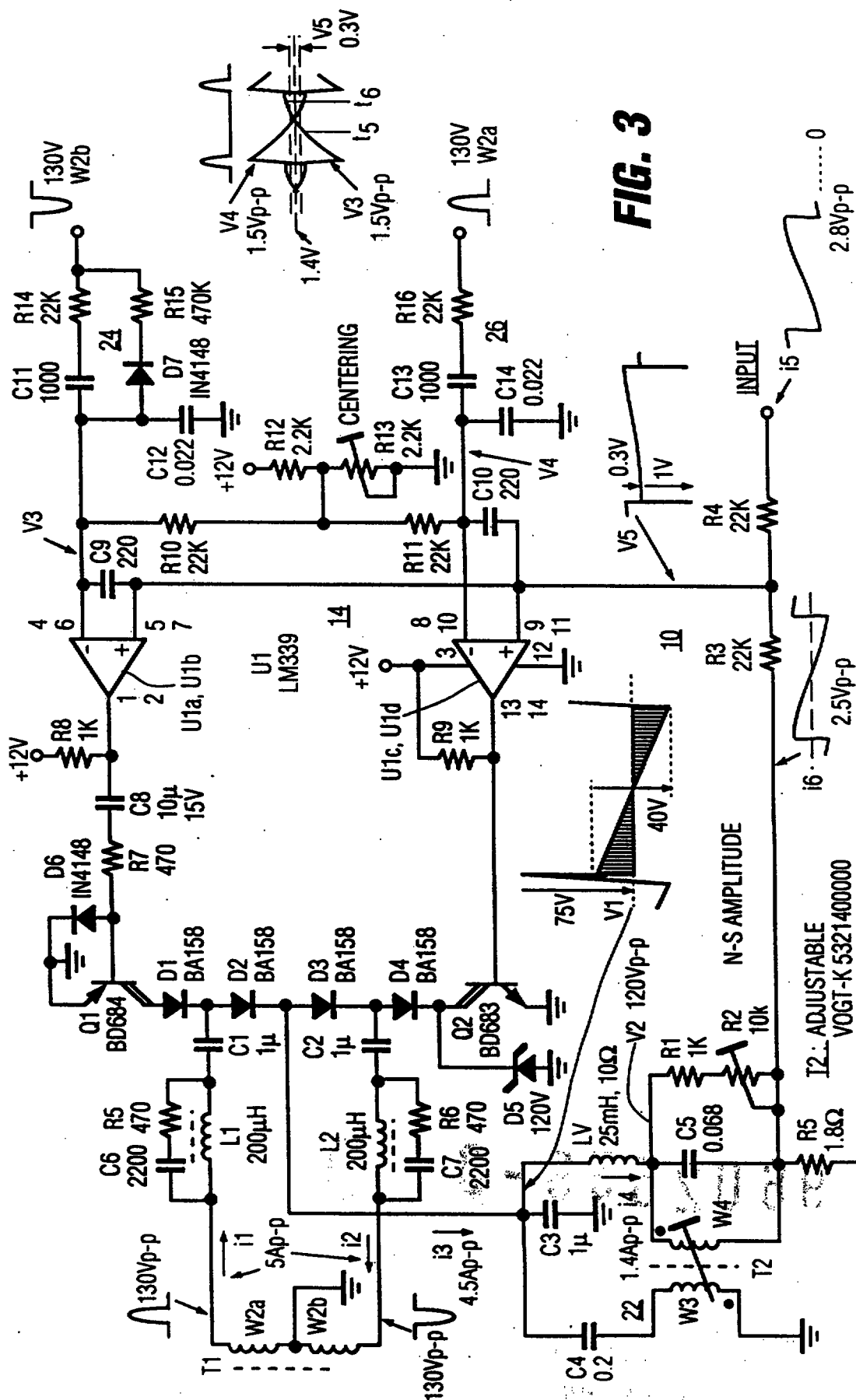


FIG. 3

CAPACITOR VALUES > 1 IN pf UNLESS OTHERWISE MARKED
 CAPACITOR VALUES ≤ 1 IN μf
 RESISTOR VALUES IN Ω UNLESS OTHERWISE MARKED

T2: ADJUSTABLE
 VOGT-K 5321400000
 W1: 50 TURNS, 0.25mm
 W2: 240 TURNS, 0.5mm
 MAX. 2mH 1Ω



TEXT OF THE ABSTRACT

RASTER CORRECTED VERTICAL DEFLECTION CIRCUIT

Two windings (W2a, W2b) of a flyback transformer (T1) in a horizontal deflection circuit are inductively coupled with opposite polarity to a source of horizontal rate retrace pulses (12). The windings (W2a, W2b) have a common junction coupled to ground. A circuit (L1, C1, L2, C2) energized by the retrace pulses generates modulated currents of opposite polarity. Conduction of each current is controlled by a switch circuit (18, 20) including a semiconductor switch (Q1, Q2) and two diodes (D1-D4). The switch circuits (18, 20) are coupled to one another at a junction, and the junction is coupled to an energy storage capacitance (C3). One of the diodes conducts positively valued portions of the respective current through the energy storage capacitance (3) and the other of the diodes conducts negatively valued portions of the respective current through the semiconductor switch (Q1, Q2). Each semiconductor switch (Q1, Q2) is a current discharge path. The energy storage capacitance (C3) is responsive to the currents for developing a vertical deflection voltage in phase with the currents at the horizontal rate for driving a vertical deflection current in a vertical deflection yoke (LV). The vertical deflection current is related to the difference in amplitude between positively valued portions of the currents. A North-South pincushion correction current in phase with the horizontal deflection is generated by integration of the vertical deflection is generated by integration of the vertical deflection voltage (V1) in the vertical deflection yoke (2V). A North-South pincushion transformer (T2) has a first winding capacitively coupled to the energy storage capacitance (C3) and a second winding (W4) forming part of a horizontal rate resonant circuit coupled in series with the vertical deflection yoke (LV).

Figure 1.

REPLACEMENT SHEET

28 MAY 2001