CLAIMS

1. A storage management apparatus, disposed between a network on chip and a storage apparatus, comprising:

an instruction parser, configured to parse an instruction received from the network on chip, and generate a control signal according to the instruction; and

a data packet generator, configured to generate at least one data packet based on data released from the storage apparatus according to the control signal, and send all the data packets to the network on chip;

wherein a plurality of processing cores are indicated by the instruction; and

the data packet generator is further configured to generate the data packets corresponding to each processing core based on the released data and the processing cores indicated by the instruction according to the control signal, and send the generated plurality of data packets to the network on chip in parallel.

2. The apparatus according to claim 1, wherein the instruction includes fetch information and storage information.

3. The apparatus according to claim 2, wherein the apparatus further comprises an access indicator;

the access indicator is configured to receive the fetch information, and instruct the storage apparatus to release the data indicated by the fetch information according to the fetch information; and

the access indicator is further configured to receive the storage information, and generate a storage address of the data packet corresponding to the processing core indicated by the instruction according to the storage information.

4. The apparatus of claim 3, wherein

the data packet generator is further configured to generate an address of the processing core indicated by the instruction according to the control signal, and generate the data packet based on the released data, the storage address and the address of the processing core indicated by the instruction.

5. The apparatus of claim 4, wherein the data packet generator comprises switches, and the number of the switches is greater than or equal to the number of processing cores connected to the network on chip;

wherein each processing core corresponds to one of the switches, and the control signal is used to control states of the switches.

6. The apparatus of claim 5, wherein

the data packet generator is further configured to turn on the switch corresponding to the processing core indicated by the instruction according to the control signal, and send the plurality of the data packets to the network on chip in parallel, so as to send the plurality of data packets to the respective corresponding processing cores through the network on chip.

7. The apparatus according to claim 5 or 6, wherein the switch comprises a control terminal, an input terminal and an output terminal;

the input terminal of each of the switches is configured to receive the storage address sent by the access indicator and the data released from the storage apparatus; and

the control terminal of each of the switches is configured to implement an on state or an off state according to the control signal received.

8. The apparatus according to any of claims 1-7, wherein

the instruction includes control bits; the control bit corresponding to the processing core indicated by each instruction is a preset value; and

the control signal is generated when the instruction parser determines that the control bit is a preset value.

9. A chip, comprising a network on chip, a plurality of processing cores connected to the network on chip, a storage apparatus, and the storage management apparatus according to any one of claims 1-8.