WHAT IS CLAIMED IS:

1. A semiconductor apparatus, comprising:
a substrate;
a transistor having a gate region, a source region, and a drain region located above the substrate in a vertical dimension perpendicular to the substrate;
a first metal layer located above the transistor in the vertical dimension;
a second metal layer located below the transistor in the vertical dimension;
a first via providing a vertical connection between the source region and the first metal layer;
a second via providing a vertical connection between the source region and the second metal layer;
a first rail connected to both the first and second metal layers;
a second rail connected to both the first and second metal layers; and
wherein the source region is coupled to at least one of the first rail and the second rail through both the first and second metal layers.

2. The semiconductor apparatus of claim 1, wherein the first metal layer is positioned on a topside of the substrate.

3. The semiconductor apparatus of claim 1, wherein the second metal layer is positioned on a backside of the substrate.

4. The semiconductor apparatus of claim 1, wherein the first rail and the second rail are power rails connected to one or more power supplies.

5. The semiconductor apparatus of claim 1, wherein the first rail and the second rail are signal rails for the source region.

6. The semiconductor apparatus of claim 1, wherein the source region is coupled to the first rail through the first via and the first metal layer and through the second via and

the second metal layer.

7. The semiconductor apparatus of claim 1, further comprising:

a third via providing a vertical connection between the drain region and the first metal layer; and

a fourth via providing a vertical connection between the drain region and the second metal layer.

8. The semiconductor apparatus of claim 7, wherein the drain region is coupled to the second rail through the third via and the first metal layer and through the fourth via and the second metal layer.

9. The semiconductor apparatus of claim 1, further comprising at least one via that couples the gate region to at least one of the first metal layer and the second metal layer.

10. An integrated device system, comprising:

a semiconductor substrate;

a transistor having a gate region, a source region, and a drain region located above the substrate in a vertical dimension perpendicular to the substrate;

a first metal layer located above the transistor in the vertical dimension;

a second metal layer located below the transistor in the vertical dimension;

a first via providing a vertical connection between the source region and the first metal layer;

a second via providing a vertical connection between the source region and the second metal layer;

a third via providing a vertical connection between the drain region and the first metal layer;

a fourth via providing a vertical connection between the drain region and the second metal layer;

a first rail connected to both the first and second metal layers;

a second rail connected to both the first and second metal layers;

wherein the source region is coupled to the first rail through the first via and the first metal layer and through the second via the second metal layer; and

wherein the drain region is coupled to the second rail through the third via and the first metal layer and through the fourth via and the second metal layer.

11. The integrated device system of claim 10, wherein the source region receives a first portion of a current from a power supply providing a supply voltage through the first metal layer and a second portion of the current from the power supply providing the supply voltage through the second metal layer.

12. The integrated device system of claim 11, wherein the first portion of the current and the second portion of the current are controlled based on resistances of the first metal layer and the second metal layer.

13. The integrated device system of claim 10, wherein the first metal layer includes power routing coupled to the first rail and ground routing coupled to the second rail, and wherein the source region is coupled to the power routing in the first metal layer and the drain region is coupled to the ground routing in the first metal layer.

14. The integrated device system of claim 10, wherein the second metal layer includes power routing coupled to the first rail and ground routing coupled to the second rail, and wherein the source region is coupled to the power routing in the second metal layer and the drain region is coupled to the ground routing in the second metal layer.

15. An integrated circuit device, comprising:

a semiconductor substrate;

a transistor having a gate region, a source region, and a drain region;

a first metal layer located vertically above the transistor towards a topside of the substrate, the first metal layer having power routing and ground routing;

a second metal layer located vertically below the transistor towards a backside of the substrate, the second metal layer having power routing and ground routing;

a first means for contact between the power routing in the first metal layer and the source region;

a second means for contact between the ground routing in the first metal layer and the drain region;

a third means for contact between the power routing in the second metal layer and the source region; and

a fourth means for contact between the ground routing in the second metal layer and the drain region.

16. The device of claim 15, wherein the power routing and the ground routing in the first metal layer are coupled to a power supply.

17. The device of claim 16, wherein the power routing and the ground routing in the second metal layer are coupled to the power supply.

18. The device of claim 17, wherein the source region is configured to receive a first portion of a current from the power supply through the power routing in the first metal layer, and wherein the source region is configured to receive a second portion of the current from the power supply through the power routing in the second metal layer.

19. The device of claim 15, wherein the first means for contact and the second means for contact are positioned in a first insulation layer vertically above the transistor, and wherein the third means for contact and the fourth means for contact are positioned in a second insulating layer vertically below the transistor.

20. The device of claim 15, wherein the gate region is coupled to at least one of the first metal layer and the second metal layer with a via through an insulating layer above the transistor.