cells (32 typically) but consisting of very few (typically three) transistors.

It will be noted that this article proposes an architecture in which the different memory cells are made on a silicon-on-insulator substrate (SOI). The different micro-sense amplifiers are, as for them, formed either on a bulk substrate or a SOI substrate.

Each micro-sense amplifier has two input terminals connected to two main bitlines RBL (Read Bitline) and WBL (Write Bitline) which will control the read/write operations of the cells addressed in parallel via the local bitline LBL connected to the output terminal of the micro-sense amplifier.

Resorting to two main bitlines proves to be a problem in that the architecture proposed by this article cannot be transposed for producing standalone memories and thus remains limited to the production of embedded memories.

Further, each micro-sense amplifier can only address a reduced number of memory cells (16 to 32 typically) so that a relatively large number of micro-sense amplifiers (from 64k to 128k for a 2 Mbit memory) has to be resorted to. In spite of the relatively reduced size of the micro-amplifier (only 3 transistors), the drawback mentioned earlier of significant surface consumption for the sense amplification function, to the detriment of the memory function, therefore partly remains.

SHORT DESCRIPTION OF THE INVENTION

~~The object~~Embodiments of the invention ~~is~~seek to propose a technique which may allow~~s~~ the drawbacks of the architectural hierarchy proposed in the aforementioned article to be overridden.

~~For this purpose, the invention proposes, according~~ According to ~~a first~~ an aspect, there is provided a sense amplifier ~~for~~of a series of cells of a rewritable memory, including:

- a writing stage comprising a CMOS inverter, the input of which is directly or indirectly connected to an input terminal

of the sense amplifier, and the output of which is connected to an output terminal of the sense amplifier intended to be connected to a local bitline addressing the cells of said series;

- a reading stage comprising a sense transistor, the gate of which is connected to the output of the inverter and the drain of which is connected to the input of the inverter;

wherein each of the transistors has a back control gate formed in the base substrate below the channel and capable of being biased in order to modulate the threshold voltage of the transistor.

According to another aspect, there is provided a sense amplifier of a series of cells of a memory, including: a writing stage comprising a CMOS inverter, the input of which is directly or indirectly connected to an input terminal of the sense amplifier, and the output of which is connected to an output terminal of the sense amplifier intended to be connected to a local bitline addressing the cells of said series, and a reading stage comprising a sense transistor, the gate of which is connected to the output of the inverter and the drain of which is connected to the input of the inverter, wherein the reading stage comprises an additional transistor complementary to the sense transistor, the additional transistor and the sense transistor forming a CMOS inverter, the input of which is connected to the output of the reading stage and the output of which is connected to the input of the inverter of the writing stage.

According to a first embodiment, the input of the writing stage is directly connected to the input terminal of the inverter, said input terminal being intended to be connected to a main bitline which will address a plurality of sense amplifiers in parallel.

According to a second embodiment, the reading stage comprises an additional transistor, complementary to the sense transistor, the additional transistor and the sense transistor forming a CMOS inverter, the input of which is connected to the output of the writing stage and the output of which is connected to the input of the inverter of the writing stage.

In this second embodiment, the input of the writing stage may be indirectly connected to the input terminal of the inverter via a decoding stage comprising a transistor, the drain of which is connected to the input terminal of the sense amplifier and the source of which is connected to the input of the writing stage.

One or more transistors of the sense amplifier are multigate transistors. The biasing of one of the gates of the multigate transistors can be modified during operations for writing, reading and retaining data in the cells of said series.

The sense amplifier according to the ~~first aspect of the invention~~ example embodiments is preferentially made on a semiconductor-oninsulator substrate comprising a thin layer of semiconducting material separated from a base substrate by an insulating layer, and each of the transistors has a back control gate

formed in the base substrate below the channel and capable of being biased for modulating the threshold voltage of the transistor.

~~According to a second aspect, the invention relates to~~ There is also disclosed a method for controlling a sense amplifier ~~according to the first aspect of the invention made on a SeOI substrate~~ as described herein, in which the bias of the back control gates is modified during operations for writing, reading and retaining data in the cells of said series.

During a reading operation, the threshold voltage of the transistors of the writing stage may be increased and the threshold voltage of the transistor(s) of the reading stage may be decreased by controlling the bias of their back control gates.

During a writing operation, the threshold voltage of the transistors of the writing stage may be decreased and the threshold voltage of the transistor(s) of the reading stage may be increased by controlling the bias of their back control gates.

During a retention operation, the local bitline may be discharged via one of the transistors of the writing stage, for which the bias of the back control gate is controlled so as to lower its threshold voltage.

~~According to still another aspect, the invention relates to~~ There is also disclosed a matrix array of cells connected to local bitlines and to word lines, characterized in that it includes sense amplifiers ~~according to the first aspect of the invention~~ as describe herein.

In the matrix array of cells, the sense amplifiers can be arranged in one or more sense amplifier banks and the matrix array can further comprise a column decoder placed next to each bank and configured to drive said bank directly. Further logic circuits can be placed next to the sense amplifier banks or the column decoder.

~~According to another aspect, the invention relates to~~ There is also disclosed a memory including a matrix array of cells.

The memory cells and the sense amplifiers of the memory are preferentially made on a semiconductor-on-insulator substrate.

According to still another aspect, the invention ~~relates to~~ provides a main sense amplifier (MSA) intended to be connected via a main bitline to a plurality of sense amplifiers ~~according to the first embodiment of the first aspect of the invention, characterized in that it comprises a stage~~ of a series of cells of a memory, including a writing stage comprising a CMOS inverter, the input of which is directly or indirectly connected to an input terminal of the sense amplifier, and the output of which is connected to an output terminal of the sense amplifier intended to be connected to a local bitline addressing the cells of said series, and a reading stage comprising a sense transistor, the gate of which is connected to the output of the inverter and the drain of which is connected to the input of the inverter, the MSA comprising means for amplifying the signal delivered by a cell during a reading operation, and a switchable high impedance inverter stage for sending back the amplified signal onto the main bitline following the reading operation.

According to a further aspect, the invention ~~relates to~~ provides a sense amplifier including:

- a writing stage comprising a CMOS inverter, the input of which is directly or indirectly connected to an input terminal of the sense amplifier, and the output of which is connected to an output terminal of the sense amplifier intended to be connected to a local line,
- a reading stage comprising a sense transistor, the gate of which is connected to the output of the inverter and the drain of which is connected to the input of the inverter;

~~and~~ wherein one or more transistors of the writing stage and of the reading stage are independent double gate transistors~~.~~; wherein each of the transistors has a back control gate formed in the base substrate below the channel and capable of being biased in order to modulate the threshold voltage of the transistor.

~~Yet according to another aspect, the invention relates to~~ There is also disclosed a matrix array of cells comprising sense amplifiers and column decoders, wherein the sense amplifiers are arranged in a nonstaggered fashion in one or more sense amplifier banks and wherein a column decoder is placed next to each bank and configured to drive said bank directly.

SHORT DESCRIPTION OF THE DRAWINGS

Other aspects, objects and advantages of the present invention will become better apparent upon reading the

CLAIMS

1. A sense amplifier of a series of cells of a memory, including:

a writing stage comprising a CMOS inverter, the input of which is directly or indirectly connected to an input terminal of the sense amplifier, and the output of which is connected to an output terminal of the sense amplifier intended to be connected to a local bitline addressing the cells of said series, and

a reading stage comprising a sense transistor, the gate of which is connected to the output of the inverter and the drain of which is connected to the input of the inverter;

wherein each of the transistors has a back control gate formed in the base substrate below the channel and capable of being biased in order to modulate the threshold voltage of the transistor.

2. The sense amplifier according to claim 1, wherein the input of the writing stage is directly connected to the input terminal of the inverter, said input terminal being intended to be connected to a main bitline which will address a plurality of sense amplifiers in parallel.

3. The sense amplifier according to claim 1, which is made on a semiconductor-on-insulator substrate comprising a thin layer of semiconducting material separated from a base substrate by an insulating layer.

4. A matrix array of cells comprising sense amplifiers according to claim 1 and column decoders, wherein the sense amplifiers are arranged in a non-staggered fashion in one or more sense amplifier banks and wherein a column decoder is placed next to each bank and configured to drive said bank directly.

5. The sense amplifier according to claim 1, wherein one or more of the transistors are multigate transistors.

6. A sense amplifier of a series of cells of a memory, including:

a writing stage comprising a CMOS inverter, the input of which is directly or indirectly connected to an input terminal of the sense amplifier, and the output of which is connected to an output terminal of the sense amplifier intended to be connected to a local bitline addressing the cells of said series, and

a reading stage comprising a sense transistor, the gate of which is connected to the output of the inverter and the drain of which is connected to the input of the inverter,

wherein the reading stage comprises an additional transistor complementary to the sense transistor, the additional transistor and the sense transistor forming a CMOS inverter, the input of which is connected to the output of the reading stage and the output of which is connected to the input of the inverter of the writing stage.

7. The sense amplifier according to claim 6, wherein the input of the writing stage is indirectly connected to the input terminal of the inverter via a decoding stage comprising a transistor, the drain of which is connected to the input terminal of the sense amplifier and the source of which is connected to the input of the writing stage.

8. The sense amplifier according to claim 6, wherein one or more of the transistors are multigate transistors.

9. A matrix array of cells comprising sense amplifiers according to claim 6 and column decoders, wherein the sense amplifiers are arranged in a non-staggered fashion in one or more sense amplifier banks and wherein a column decoder is placed next to each bank and configured to drive said bank directly.

10. A main sense (MSA) amplifier intended to be connected via a main bitline to a plurality of sense amplifiers of a series of cells of a memory, including a writing stage comprising a CMOS inverter, the input of which is directly or indirectly connected to an input terminal of the sense amplifier, and the output of which is connected to an output terminal of the sense amplifier intended to be connected to a local bitline addressing the cells of said series, and a reading stage comprising a sense transistor, the gate of which is connected to the output of the inverter and the drain of which is connected to the input of the inverter, the MSA comprising means for amplifying the signal delivered by a cell during a reading operation, and a switchable high impedance inverter stage for sending back the amplified signal onto the main bitline following the reading operation.

11. A sense amplifier including:

a writing stage comprising a CMOS inverter, the input of which is directly or indirectly connected to an input terminal of the sense amplifier, and the output of which is connected to an output terminal of the sense amplifier intended to be connected to a local line, and

a reading stage comprising a sense transistor, the gate of which is connected to the output of the inverter and the drain of which is connected to the input of the inverter;

wherein one or more transistors of the writing stage and of the reading stage are independent double gate transistors;

wherein each of the transistors has a back control gate formed in the base substrate below the channel and capable of being biased in order to modulate the threshold voltage of the transistor.

12. A matrix array of cells connected to local bitlines and to wordlines, comprising a sense amplifier according to claim 1 or 11.

13. A matrix array of cells according to claim 12, wherein the sense amplifiers are made on a semiconductor-on-insulator substrate.

14. A matrix array of cells according to claim 13, wherein the sense amplifiers are arranged in one or more sense amplifier banks and further comprising a column decoder placed next to each bank and configured to drive said bank directly.

15. A matrix array of cells according to claim 14, further comprising logic circuits placed next to the sense amplifier banks or the column decoder.

16. A memory including a matrix array of cells according to claim 12.

17. A method for controlling a sense amplifier according to claim 8, which comprises modifying the biasing of one of the gates of the transistors during operations for writing, reading or retaining of data in the cells of the series.

18. A method for controlling a sense amplifier according to claim 3, which comprises modifying the biasing of the back control gates during operations for writing, reading and retaining data in the cells of the series.

19. The method according to claim 18, wherein the biasing of the back control gates is controlled during a reading operation to increase the threshold voltage of the transistors of the writing stage and to reduce the threshold voltage of the transistor(s) of the reading stage.

20. The method according to claim 18, wherein the biasing of the back control gates is controlled during a writing operation to reduce the threshold voltage of the transistors of the writing stage and to increase the threshold voltage of the transistor(s) of the reading stage.

21. The method according to claim 18, wherein during a retention operation, the local bitline is discharged via one of the transistors of the writing stage, for which the biasing of the back control gate is controlled so as to lower its threshold voltage.

22. A method for controlling a sense amplifier according to claim 5, which comprises modifying the biasing of one of the gates of the transistors during operations for writing, reading or retaining of data in the cells of the series.

CLAIMS

1. A sense amplifier (nSA) of a series of cells (Ci, Cj) of a memory, including:

- a writing stage comprising a CMOS inverter (T1-T2), the input of which is directly or indirectly connected to an input terminal of the sense amplifier, and the output of which is connected to an output terminal of the sense amplifier intended to be connected to a local bitline (LBL) addressing the cells of said series,

- a reading stage comprising a sense transistor (T3), the gate of which is connected to the output of the inverter and the drain of which is connected to the input of the inverter,

wherein each of the transistors has a back control gate formed in a base substrate below the channel and capable of being biased in order to modulate the threshold voltage of the transistor.

2. The sense amplifier according to claim 1, wherein the input of the writing stage is directly connected to the input terminal of the inverter, said input terminal being intended to be connected to a main bitline (MBL) which will address a plurality of sense amplifiers in parallel.

3. The sense amplifier according to the preceding claim, characterized in that it is made on a semiconductor-on-insulator substrate comprising a thin layer of semiconducting material separated from the base substrate by an insulating layer.

4. A matrix array of cells according to claim 15, wherein the sense amplifiers are arranged in one or more sense amplifier banks and further comprising a column decoder placed next to each bank and configured to drive said bank directly.

5. The sense amplifier according to any of the preceding claims, wherein one or more of the transistors are multigate transistors.

6. The sense amplifier according to claim 1, wherein the reading stage comprises an additional transistor (T4) complementary to the sense transistor, the additional transistor and the sense transistor forming a CMOS inverter, the input of which is connected to the output of the reading stage and the output of which is connected to the input of the inverter of the writing stage.

7. The sense amplifier according to claim 6, wherein the input of the writing stage is indirectly connected to the input terminal of the inverter via a decoding stage comprising a transistor (T5), the drain of which is connected to the input terminal of the sense amplifier and the source of which is connected to the input of the writing stage.

8. A main sense amplifier (MSA) intended to be connected via a main bitline (MBL) to a plurality of sense amplifiers according to any of claims 1 to 7, characterized in that it comprises a step for amplifying

the signal (T6-T10) delivered by a cell during a reading operation, and a switchable high impedance inverter stage (HZI) for sending back the amplified signal onto the main bitline following the reading operation.

9. A sense amplifier (nSA) including:

- a writing stage comprising a CMOS inverter (T1-T2), the input of which is directly or indirectly connected to an input terminal of the sense amplifier, and the output of which is connected to an output terminal of the sense amplifier intended to be connected to a local line,

- a reading stage comprising a sense transistor (T3), the gate of which is connected to the output of the inverter and the drain of which is connected to the input of the inverter;

and wherein one or more transistors of the writing stage and of the reading stage are independent double gate transistors,

each of the transistors has a back control gate formed in the base substrate below the channel and capable of being biased in order to modulate the threshold voltage of the transistor.

10. A matrix array of cells connected to local bitlines and to wordlines, characterized in that it includes sense amplifiers according to any of claims 1 to 7, or to claim 9.

11. A matrix array of cells according to claim 10, wherein the sense amplifiers are made on a semiconductor-on-insulator substrate.

12. A matrix array of cells according to claim 11, further comprising logic circuits placed next to the sense amplifier banks or the column decoder.

13. A matrix array of cells according to claim 12, wherein the sense amplifiers are arranged in a non-staggered fashion in one or more sense amplifier banks and wherein a column decoder is placed next to each bank and configured to drive said bank directly.

14. A memory including a matrix array of cells according to any one of claims 14 to 17.

15. A method for controlling a sense amplifier according to any of claims 1 to 7, wherein the biasing of one of the gates of the transistors is modified during operations for writing, reading and retaining data in the cells of said series.

16. A method for controlling a sense amplifier according to any of claims 1 to 7, wherein the biasing of the back control gates is modified during operations for writing, reading and retaining data in the cells of said series.

17. The method according to claim 15 or 16, wherein during a reading operation, the threshold voltage of the transistors of the writing stage is increased and the threshold voltage of the transistor(s) of the reading

stage is reduced by controlling the biasing of the back control gates thereof.

18. The method according to claim 15 or 16, wherein during a writing operation, the threshold voltage of the transistors of the writing stage is reduced and the threshold voltage of the transistor(s) of the reading stage is increased by controlling the biasing of the back control gates thereof.

19. The method according to claim 15 or 16, wherein during a retention operation, the local bitline is discharged via one of the transistors of the writing stage, for which the biasing of the back control gate is controlled so as to lower its threshold voltage.