PROCESS FOR MANUFACTURE OF A P-CHANNEL MOS GATED DEVICE WITH BASE IMPLANT THROUGH THE CONTACT WINDOW

ABSTRACT OF THE DISCLOSURE

An MOS-gated power semiconductor device is formed by a process that uses a reduced number of masking steps and minimizes the number of critical alignments. A first photolithographic masking step defines the body or channel region and the source region of each of the cells. A second photolithographic step is aligned to a small central area above the source region of each of the cells or strips, the only critical alignment in the process, and is used to define openings in a protective oxide layer which, in turn, masks the etching of depressions in the substrate surface and the formation of a contact region. An isotropic etch undercuts the protective oxide to expose shoulders at the silicon surface of the chip which surround the etched holes. A conductive layer fills the holes and thus contacts the underlying body regions and overlaps the shoulders surrounding the source regions at the silicon surface. The conductive layer is sintered at a temperature that is sufficiently high to achieve low contact resistance between the metal and body regions but is low enough to be tolerated by the conductive layer.

Fig.4