

SPECIFICATION

RMS circuit for voltage regulation

5 DESCRIPTION

This invention relates to a circuit for calculating the RMS (Root Mean Square) value of a periodic voltage and, more particularly, to a voltage regulator for a generator which utilizes the RMS value of the voltage from the generator for regulation.

Voltage regulators for aircraft generators usually employ peak or average voltage sensing for regulation. Various specifications and military requirements, however, often list performance standards of power quantity and quality in terms of RMS values. Accordingly, regulators have been developed which sense the average or peak values of the voltage and provide RMS voltage regulation from the measured average or peak values of the voltage.

These regulators may be satisfactory for generators that provide perfect sinusoidal waveforms since a fixed relationship exists between peak or average voltages and the RMS value of the voltage. However, the output voltage from the generators is not a perfect sinusoidal waveform, and the harmonic content in the output varies between generators and with loads. The harmonic content in the output destroys the fixed relationship between the peak or average voltage and the RMS voltage. Thus, regulators that sense peak or average voltage and provide RMS voltage regulation are often inaccurate.

Several attempts have been made to more accurately provide RMS voltage regulation from regulators that sense the peak or average voltage. For example, specifically designed filters and load current feedback circuits have been designed to tailor a particular generator to a voltage regulator. Since for each application the generator and regulator has unique characteristics, a filter or feedback circuit which is designed for one may not work for another as a result of variations in the harmonic content of the output voltage from the generator.

Conventional hybrid RMS to DC converters are not capable of quickly regulating the voltage in generators because they usually include a low pass filter which introduces a lag into the information conversion process that is longer than one cycle of the frequency of the generator.

The invention provides a circuit for providing a signal proportional to the RMS value of a periodic input voltage having a variable frequency comprising:
means for sensing the periodic input voltage $V_{IN}(t)$; and
means for providing a signal proportional to

$$\sqrt{\frac{1}{T} \int_0^T [V_{IN}(t)]^2 dt}$$

wherein t represents time and T represents the period of the periodic input voltage at least once each period of the input voltage $V_{IN}(t)$.

A circuit according to the invention can provide the RMS value of a periodic waveform having either a variable or fixed frequency, without introducing a time lag into the information conversion process. The circuit can be used in a voltage regulator for providing a field current proportional to the RMS value of the voltage from the generator.

In a typical circuit according to the invention, the voltage from the generator is applied to a rectifier which provides for either half-wave or full-wave rectification. The output from the rectifier is applied to a multiplier for squaring the voltage from the rectifier. The squared voltage is then integrated for a period of time equal to the half-period of the waveform. At or near the end of each half period, the integrator is sampled and reset, and a voltage equal to the voltage sampled is held until the integrated voltage is again sampled. The voltage equal to the sampled voltage is divided by a voltage proportional to the half-period of the waveform. The output from the divider is applied to a circuit which takes the square root thereof to provide a continuous signal representative of the RMS value of the voltage from the generator.

The voltage regulator in accordance with the present invention is particularly well suited for a three-phase generator and provides a field current representative of the RMS value of each phase by calculating the RMS value of the voltage for each phase as discussed above and coordinating that field current with the output voltage from the generator.

It is a feature of the present invention to provide a circuit for calculating the RMS voltage of a periodic waveform having either a variable or fixed frequency.

Another feature of the present invention is to provide a circuit for calculating the RMS value of a periodic waveform for use in a voltage regulator for a generator.

Yet another feature of the present invention is to provide a circuit for calculating the RMS value of a periodic waveform which can be used in a voltage regulator for a three-phase generator.

DRAWING

Figure 1A is a block diagram illustrating the circuit for calculating the RMS voltage from a periodic waveform having a variable frequency;

Figure 1B depicts various waveforms at various points in the block diagram of Figure 1A;

- 5 Figure 2A is a block diagram illustrating the circuit for calculating the RMS voltage for a periodic waveform having a fixed frequency;

Figure 2B depicts various waveforms at various points in the block diagrams of Figure 2A;

Figure 3 is a block diagram of a generator employing an RMS voltage regulator in accordance with the present invention;

- 10 Figure 4 is a block diagram of the RMS voltage regulator for the generator shown in Figure 3;

Figure 5 is a diagram of a portion of the timing logic employed in the circuit of Figure 4;

Figure 6 depicts waveforms helpful in the understanding of the timing logic shown in Figure 5; and

Figure 7 is a circuit diagram of a portion of the timing logic employed in the circuits shown in Figures 1, 2 or 4 and the associated waveforms.

- 15 Referring to Figure 1A, the circuit for calculating the root mean square voltage receives a periodic waveform V_{IN} , and provides a voltage V_{RMS} , which is the RMS value of V_{IN} . V_{RMS} is often referred to as the effective voltage, and may be expressed as:

$$20 \quad V_{RMS} = \sqrt{\frac{1}{T} \int_0^T [V_{IN}(t)]^2 dt} \quad (1) \quad 20$$

- 25 wherein $V_{IN}(t)$ represents the Fourier series for any periodic input waveform of period T. Or, considering only symmetrical half-waves, Equation (1) can be rewritten as:

$$30 \quad V_{RMS} = \sqrt{\frac{2}{T} \int_0^{T/2} [V_{IN}(t)]^2 dt} \quad (2) \quad 30$$

- 35 Referring to Figure 1B, waveforms at various points in the block diagram of Figure 1A are shown. The waveforms shown are for a circuit that employs a half-wave rectifier, as will be discussed in detail below. A half-wave rectifier may be selected for use in the circuit when the input voltage is known to display half-wave symmetry, as is clear from Equation (2). Of course, a full-wave rectifier could be employed in lieu of a
40 half-wave rectifier, but the waveforms in Figure 1B would not be the same. The circuit would necessarily be changed slightly to conform to Equation (1).

- Rectifier and divider circuit 10 provide for half-wave rectification of the input voltage $V_{IN}(t)$ which, for illustrative purposes is shown to have a peak of 115 volts. The output from the rectifier and divider circuit 10 is a half-wave rectified signal V_1 attenuated to a selected lower level, as for example a 2V peak value. The
45 output V_1 is applied to multiplier circuit 12 for squaring the input waveform to provide the $[V_{IN}(t)]^2$ term in Equation (2), which is shown as V_2 .

- The output of multiplier 12 is applied to controlled integrator 14 for integrating $[V_{IN}(t)]^2$ for each full half-period of the waveform, that is between 0 and $\frac{T}{2}$. The output from controlled integrator 14, denoted as V_3 , is applied to sample and hold circuit 16. After the voltage V_3 from controlled integrator 14 is sampled and
50 held by sample and hold circuit 16, controlled integrator 14 is zeroed and is ready to operate on a next half-cycle of the input waveform.

The output of the sample and hold circuit 16, is a constant dc voltage which is updated to a new value each time the control integrator 14 is sampled. The output from the sample and hold circuit 16 is constant until the next update point.

- 55 Timing circuit 18, which is responsive to the input voltage $V_{IN}(t)$, controls the points in time at which the controlled integrator 14 integrates the voltage $[V_{IN}(t)]^2$ to assure that integration takes place for the full half-period of $V_{IN}(t)$, that is, between 0 and time $T/2$. Timing circuit 18 also coordinates the timing of the sample and hold circuit 16 so that the output from the controlled integrator 14 is sampled at the end of the period during which integration occurs. Thereafter, the controlled integrator 14 is cleared by a signal from
60 the timing circuit 18. The details of timing circuit 18 will be discussed in greater detail below in connection with Figures 5 and 6.

- The constantly updated DC voltage from sample and hold circuit 16, which is shown in Figures 1A and 1B as V_4 , is applied to divider circuit 20. The time period $T/2$ is derived from the voltage V_5 from the timing circuit 18. This voltage is sampled by sample and hold circuit 22 to provide a voltage V_6 . The magnitude of the
65 voltage V_6 is proportional to the length of time $T/2$, but is constant for the half-period. The voltage from

sample and hold circuit 16 is divided by the voltage from sample and hold circuit 22 to provide the division of $[V_{IN}(t)]^2$ by $T/2$ as required by Equation (2).

The output from divide circuit 20, as represented by V_7 , is applied to square root circuit 24. The square root circuit 24 generates a voltage equal to the square root of the voltage applied to its input. This circuit provides the square root operation in Equation (2). The output from square root circuit 20 is $V_{RMS}(t)$, which is proportional to the RMS value of $V_{IN}(t)$, as shown.

Often there are systems in which the frequency of the voltage $V_{IN}(t)$ is controlled to remain constant. If the frequency of the voltage $V_{IN}(t)$ is constant and displays half-wave symmetry, the circuit shown in Figure 1A can be simplified. Specifically, assuming half-wave symmetry and further assuming that the frequency of the input waveform $V_{IN}(t)$ is constant, Equation (3) can be expressed as follows:

$$V_{RMS} = \sqrt{\frac{1}{K} \int_0^{T/2} [V_{IN}(t)]^2 dt} \quad (3)$$

wherein $T/2$ represents a fixed period of time equal to a half period of the waveform $V_{IN}(t)$, and K represents a constant proportional to the fixed period of time $T/2$.

Referring to Figure 2A, the circuit for calculating the root mean square voltage of a periodic waveform displaying half-wave symmetry and displaying a fixed frequency is shown. Although a half-wave rectifier will be described in detail below, a full-wave rectifier could be employed in lieu of the half-wave rectifier. In that event, the waveforms of Figure 2B would not be the same.

Rectifier and divider circuit 26 provide for half-wave rectification of the input voltage which, for purposes of illustration, is shown to have a peak of 115 volts. The output from the rectifier and divider circuit 26 is a half-wave rectified signal V_1 attenuated to a selected lower level as, for example, 2 volts peak value. The output V_1 is applied to multiplier circuit 28 for squaring the input waveform to provide the $[V_{IN}(t)]^2$ term of Equation (3), which is shown as V_2 .

The output from multiplier 28 is applied to controlled integrator 30 for integrating the $[V_{IN}(t)]^2$ for each full half-period of the waveform, that is, between 0 and $T/2$. The output from controlled integrator 30, denoted as V_3 , is applied to sample and hold circuit 32. After the voltage V_3 from controlled integrator 30 is sampled and held by sample and hold circuit 32 to provide V_4 , controlled integrator 30 is zeroed and is ready to operate on the next half-cycle of the input waveform having the constant period.

The output of the sample and hold circuit 32, V_4 , remains constant for the half-period, and is updated to a new value each time the controlled integrator 30 is sampled. The output from the sample and hold circuit 32 is constant until the next update point.

Timing circuit 34, which is responsive to the input voltage $V_{IN}(t)$, controls the point in time at which the controlled integrator 30 integrated the voltage $[V_{IN}(t)]^2$ to assure that integration takes place for the full half-period of the voltage $V_{IN}(t)$, that is, between 0 and $T/2$. Timing circuit 34 also coordinates the timing of sample and hold circuit 32 so that the output from the controlled integrator 30 is sampled at the end of the period during which integration occurs. Thereafter, controlled integrator 30 is cleared by a signal from timing circuit 34. The details of the timing circuit will be discussed in greater detail below in connection with Figures 5 and 6.

The constantly updated DC voltage, V_4 , from sample and hold circuit 32, is applied to the square root circuit 36. The square root circuit 36 provides a voltage equal to the square root of the voltage applied to its input in a manner identical to that described with respect to Figure 1A. The output from the circuit is $V_{RMS}(t)$, which is proportional to the RMS value of $V_{IN}(t)$ as shown for an input waveform having a constant frequency.

Referring to Figure 3, a generator having a regulator employing the principles of the circuit of Figure 1 or Figure 2 is shown. Generator 38, schematically shown to include main windings 40, provides power at a rated AC voltage (115 volts) to load 42. RMS voltage regulator 44 receives the voltages $V_{IN}(t)$ for each phase of the voltage from windings 40. The phase voltages will hereinafter be referred to as ϕA , ϕB and ϕC voltages. As will be explained in detail below, RMS voltage regulator 44 provides a field current to maintain the RMS value of the input voltage $V_{IN}(t)$ for accurate RMS regulation of the output voltage. Also applied to RMS voltage regulator 44 are signals from current transformers 48 which represent the current provided to load 42. These signals can be employed to control the magnitude of the exciter field current during a fault condition.

Referring to Figure 4, the RMS voltage regulator will now be described. The input voltages $V_{IN}(t)$ for each ϕA , ϕB and ϕC are applied to rectifier and divider circuit 50-A, 50-B and 50-C, respectively. Each of the rectifier and divider circuits 50 operates in an identical manner, and similar to the corresponding circuit discussed above in connection with Figure 1. The outputs from the rectifier and divider circuits are applied to the multiplier circuits 52 for each ϕA , ϕB and ϕC , and operate in a manner identical to the corresponding circuit discussed in connection with Figure 1. The output from the multiplier circuit is applied to controlled

integrator circuit 54 for each ϕA , ϕB and ϕC , and also operates in a manner identical to the corresponding circuit described in connection with Figure 1.

The outputs from controlled integrators 54 are applied to the sample and hold circuit 56 which samples voltage therefrom once each half-period for ϕA , ϕB and ϕC , or three times per cycle of $V_{IN}(t)$.

5 The timing circuit 58, which is functionally similar to timing circuit 18 in Figure 1, includes wave-shaping circuit 60-A, 60-B, 60-C and timing logic 62. The timing logic 62 is responsive to $V_{IN}(t)$, and controls the periods of time in which controlled integrators 54-A, 54-B and 54-C are operated and cleared and the time in which the sample from integrators 14 are sampled by sample and hold circuit 16. Timing logic 62 also provides a signal proportional to $T/2$ to sample and hold circuit 64.

10 The output from the sample and hold circuit 56 is applied to the divider circuit 66. The voltage from sample and hold circuit 56 is divided by the voltage representing $T/2$ as required by Equation (2). The output of divide circuit 66 is applied to square root circuit 68. The square root circuit 68 provides an output voltage $V_{RMS}(t)$ proportional to the RMS value of the input voltage for ϕA , ϕB and ϕC of the voltage $V_{IN}(t)$.

The output from square root circuit 68 is applied to a comparator 70. Also applied to comparator 70 is a voltage from zener reference 72 which represents a selected or reference RMS value for the voltage. The output from comparator 70 is an error signal representative of the difference in magnitude and sign between the measured RMS voltage from square root circuit 68 and the reference voltage from zener reference 72. The output from comparator 70 is applied to high-phase gain and compensation circuit 74 and to integrator gain and compensation circuit 76.

20 The high-phase gain and compensation circuit 74 is of the form

$$\frac{K_1(T_1S+1)}{T_2S+1}$$

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and has a selected time constant such that the highest phase will dominate. The output from high-phase gain and compensation circuit 74 provides the basic correction signal to summer 78.

The integrator gain and compensation circuit 76 is of the form

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$$\frac{K_2(T_3S+1)}{S(T_4S+1)}$$

35 and provides for integral trim yielding zero error voltage control. The voltage correction range of this circuit is limited (as to 5 volts) so the highest phase proportional signal dominates during transients. The output of integrator gain and compensation circuit 76 is applied to summer 78.

The output from summer 76 is a voltage proportional to the RMS value of the voltage $V_{IN}(t)$, and is coupled to the exciter field 46 (Figure 2) of generator 44.

40 Other networks and circuits can be applied to summer 76 to further modify the signal from integrator gain and compensation circuit 78. For example, current limit gain and compensation circuit 80, coupled to the current transformer 48 (Figure 2) may provide a signal to reduce the magnitude of the field current in the event that the per unit current becomes excessive, as during fault conditions. Also, compensation network 82, which receives a signal proportional to the exciter current, may be employed to improve transient performance and eliminate gain variations due to temperature changes in the exciter field resistance.

45 The field current may be pulse-width modulated and synchronized with generator 44 in any acceptable manner including synchronization of the 1200 Hz ripple frequency. Alternatively, the field current amplifier can be synchronized to the generator 44 by use of a PMG (permanent magnet generator) (not shown).

It is apparent that the system described above is particularly well suited for accurate regulating during a transient condition when the frequency of $V_{IN}(t)$ changes. Such transient conditions may result from many factors, including the application of a shock load (i.e., when the rated load is applied to the generator in one step). Of course, if the frequency of $V_{IN}(t)$ is assumed to be constant, the system described above can be simplified, as discussed in connection with Figure 2.

50 The timing logic 62 includes the circuit shown in Figure 5 and the circuit shown in Figure 7. Referring to Figure 5, ϕA , ϕB and ϕC of the voltage $V_{IN}(t)$ are selectively provided to gates 84-89. Gates 84, 86 and 88 are provided with inverters on their input, as shown. The outputs from gates 84-89 represent the sample and clear functions for each phase of the voltage from generator 44. Specifically, the sampling of the ϕA voltage occurs at the end of the reception of the half-period from ϕA (π), and is represented by $\overline{A-C}$, as seen in Figure 6. The integrator 54-A is cleared at $4\pi/3$ after ϕA has been sampled, and is represented by $B-C$. Each half-period, the voltage of controlled integrator 54-B is sampled by a sample ϕB signal developed from $\overline{A-B}$ at $5\pi/3$. After integrator 54 has been sampled, it is cleared by a signal clear ϕB signal developed from $\overline{A-C}$ at 2π . Finally, integrator 54-C is sampled at the end of the half-period of ϕC voltage at $\pi/3$ by sample ϕC developed from $\overline{B-C}$. Controlled integrator 54-C is cleared by clear ϕC signal which may be developed from $\overline{A-B}$ at $2\pi/3$. OR gate 90 may be employed to provide a clear signal for ϕA , ϕB or ϕC .

Referring to Figure 7, an analog circuit for providing a voltage proportional to $T/2$ is shown, and is typical of each circuit required for each of ϕA , ϕB and ϕC . The switches 92 and 94 may be controlled by the logic

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shown in Figure 5 so long as they open and close in accordance with the waveform shown in Figure 7. When switch 92 is closed, a reference voltage, established by zener diode 94 by current flow through resistor 96, is applied to the negative terminal of op-amp 98 by way of resistor 100. At the end of the $V_{IN}(t)$ for A, switch 92 is opened and the output voltage stored by capacitor 102 may be sampled. The output voltage is proportional to $T/2$. After the voltage has been sampled, capacitor 102 is cleared by closing switch 94.

Although an analog system has been described, many circuits could be used to provide a voltage proportional to the time $T/2$. It is apparent that the timing logic can perform additional functions. First, in the event of a fault which causes the voltage of one or more phases to collapse to zero, the PMG takes over the timing function. Also, the PMG voltage of the phase voltage can be applied to a triangular oscillator to synchronize the frequency of the modulating means so that the output pulse width-modulated waveform frequency is an even multiple of and in synchronization with the line voltage frequency. This is desirable to avoid any possibility of frequency modulation caused by two unsynchronized frequencies.

CLAIMS

1. A circuit for providing a signal proportional to the RMS value of a periodic input voltage having a variable frequency comprising:
means for sensing the periodic input voltage $V_{IN}(t)$; and
means for providing a signal proportional to

$$\sqrt{\frac{1}{T} \int_0^T [V_{IN}(t)]^2 dt}$$

wherein t represents time and T represents the period of the periodic input voltage at least once each period of the input voltage $V_{IN}(t)$.

2. A circuit for providing a signal proportional to the RMS value of a periodic input voltage having a variable frequency comprising:
means for sensing the periodic input voltage $V_{IN}(t)$; and
means for providing a signal proportional to

$$\sqrt{\frac{2}{T} \int_0^{T/2} [V_{IN}(t)]^2 dt}$$

wherein t represents time and $T/2$ represents a half period of the periodic waveform at least once each half-period of the input voltage $V_{IN}(t)$.

3. A circuit for providing a signal proportional to the RMS value of a periodic input voltage having a constant frequency comprising:
means for sensing the periodic input voltage $V_{IN}(t)$; and
means for providing a signal proportional to

$$\sqrt{\frac{1}{K} \int_0^{T/2} V_{IN}(t)^2 dt}$$

wherein t represents time, $T/2$ represents a fixed period of time equal to a half-period of the waveform $V_{IN}(t)$, and K represents a constant proportional to the period of time $T/2$ at least once each cycle of the input voltage $V_{IN}(t)$.

4. A circuit for providing a voltage proportional to the RMS value of a periodic waveform having a fixed frequency comprising:
means for rectifying said periodic waveform to provide a first voltage;
means for squaring the first voltage to provide a second voltage;
means for integrating said second voltage for a period of time equal to one-half a period of said periodic waveform to provide an integrated voltage;

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means for reading and storing the integrated voltage at least once each period of said periodic waveform to provide a sample voltage, while simultaneously resetting the value of the integrated voltage to zero; and means for taking the square root of the sample voltage, thereby providing a voltage proportional to said RMS value of the periodic waveform.

5 5. A circuit for providing a voltage proportional to the RMS value of a periodic waveform having a variable frequency comprising:

means for rectifying said periodic waveform to provide a first voltage;

means for squaring the first voltage to provide a second voltage;

means for integrating said second voltage for a period of time equal to one-half a period of said periodic

10 waveform to provide an integrated voltage;

means for dividing said integrated voltage by a signal proportional to the period of said periodic waveform;

means for reading and storing the integrated voltage at least once each period of said periodic waveform to provide a sample voltage, while simultaneously resetting the value of the integrated voltage to zero; and

15 means for taking the square root of the sample voltage, thereby providing a voltage proportional to said RMS value of the periodic waveform.

6. The circuit of claim 5 further including:

means for holding said sample voltage until said means for reading and storing said integrated voltage next provides a sample voltage representative of a subsequent period of said periodic waveform.

20 7. The circuit of claim 5 wherein said rectifier is a half-wave rectifier.

8. The circuit of claim 7 wherein said means for reading and storing said integrated voltage provides said sample voltage once each half-period of said periodic waveform.

9. The circuit of claim 5 wherein said rectifier is a full-wave rectifier.

10. The circuit of claim 9 wherein said means for reading and storing said integrated voltage provides said sample voltage once each period of said periodic waveform.

11. A circuit for providing a voltage proportional to the RMS value of a periodic waveform comprising: a half-wave rectifier for providing a first voltage representative of every other half-period of the periodic waveform;

a voltage divider coupled to said half-wave rectifier for providing a second voltage proportional to and less than the first voltage;

a voltage multiplier coupled to said voltage divider for squaring the second voltage;

integrator means coupled to said voltage multiplier and responsive to said periodic waveform for integrating the second voltage during each half-period of the periodic waveform to provide a third voltage;

35 sampling means coupled to said integrator means and responsive to said periodic waveform for reading the third voltage at substantially the end of each half-period of the periodic waveform to provide a fourth voltage, while simultaneously resetting the third voltage to zero;

means responsive to said periodic waveform for holding said fourth voltage and providing a voltage equal to said fourth voltage until said sampling means provides a fourth voltage representative of a next succeeding half-period of the periodic waveform; and

40 means coupled to said holding means for providing the square root of said voltage equal to said fourth voltage, thereby providing the voltage proportional to the RMS value of the periodic waveform.

12. The circuit of claim 11 further including:

means for providing a fifth voltage proportional to the length of each half-period of the periodic waveform; and

45 means for dividing said voltage equal to said fourth voltage by said fifth voltage to provide a sixth voltage when said sixth voltage is applied to said means for providing the square root so that said means for providing the square root provides said voltage proportional to the periodic waveform.

13. In an AC generator for providing power to a load in response to a field current, an improved voltage regulator for providing said field current, comprising:

50 means for sensing a voltage component $V_{IN}(t)$ of the power;

means for generating a signal V_{RMS} , which signal is proportional to

$$\sqrt{\frac{2}{T} \int_0^{T/2} [V_{IN}(t)]^2 dt}$$

wherein t represents time and $T/2$ represents a half-period of the periodic waveform at least once each cycle of the voltage $V_{IN}(t)$;

means for generating a field current proportional to the signal V_{RMS} ; and

means for applying field current to the AC generator.

14. The AC generator of claim 13 wherein said means for applying the field current to the AC generator includes:

65 a high phase gain and compensation circuit.



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15. The AC generator of claim 14 further including:
an integrator gain and compensation circuit coupled in parallel with said high phase gain and compensation circuit.
16. In an AC generator for providing power to a load in response to a field current, an improved voltage
5 regulator for providing said field current, comprising: 5
means for sensing the voltage component $V_{IN}(t)$ of the power;
means for rectifying $V_{IN}(t)$ to provide a first voltage;
means for squaring the first voltage to provide a second voltage;
means for integrating said second voltage for a period of time equal to one-half period of such voltage
10 $V_{IN}(t)$; 10
means for reading and storing the integrated voltage at least once each period of said periodic waveform
to provide a sample voltage, while simultaneously resetting the value of the integrated voltage to zero; and
means for taking the square root of the sampled voltage, thereby providing a voltage proportional to the
RMS value of $V_{IN}(t)$.
- 15 17. The AC generator of claim 16 further including: 15
means responsive to $V_{IN}(t)$ for causing said means for sampling the integrated voltage to sample said
integrated voltage after said period of time of said voltage $V_{IN}(t)$ is completed.
18. The AC generator of claim 13 wherein said generator provides $V_{IN}(t)$ at phases ϕA , ϕB , ϕC , and said
voltage is proportional to said RMS value of $V_{IN}(t)$ for phases ϕA , ϕB and ϕC .
- 20 19. The AC generator of claim 18 wherein said means for sampling the integrated voltage samples $V_{IN}(t)$ 20
for ϕA , ϕB and ϕC once each cycle of $V_{IN}(t)$.
20. A circuit for providing a signal proportional to the RMS value of a periodic input voltage having a
variable frequency, substantially as described herein with reference to Figures 1A, 1B and 7 of the drawings.
21. A circuit for providing a signal proportional to the RMS value of a periodic input voltage having a
25 fixed frequency, substantially as described herein with reference to Figures 2A, 2B and 7 of the drawings. 25
22. A generator having a RMS voltage regulator, substantially as described herein with reference to
Figures 3 to 7 of the drawings.