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PATENT SPECIFICATION

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DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Electrical Resistors

5 We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organized according to the Laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

10 This invention relates to electrical resistors and especially to those formed as components in integrated circuits.

15 According to the present invention, an electrical resistor comprises a diffused region of semiconductor material of one conductivity type in a body of semiconductor material of opposite conductivity type, which region extends to a surface of the semiconductor body and is covered by an epitaxial layer of semiconductor material of the said opposite conductivity type, and spaced semiconductor regions of the said one conductivity type extending through the epitaxial layer to form electrical contact regions to the said resistor region. Such a resistor is protected from surface damage by the epitaxial layer, does not suffer from inversion effects and provides relatively high sheet resistance. Such a resistor can be manufactured, in accordance with the present invention, by diffusing impurity of one conductivity type into a body of semiconductor material of opposite conductivity type to form a diffused region of the said one conductivity type extending to a surface of the body; forming an epitaxial layer of semiconductor material of the said opposite conductivity type on the said surface of the body over the said diffused region; and diffusing impurity of the said opposite conductivity type at selected spaced locations through the epitaxial layer to form electrical contact regions to the said diffused region

which provides an electrically resistive path between the contact regions. 45

The invention also provides an electrical circuit device including two diffused regions of semiconductor material of one conductivity type in a body of semiconductor material of opposite conductivity type, both regions having like impurity concentrations and extending like depths into the body from a common surface of the body at which they are covered by an epitaxial layer of the said opposite conductivity type, spaced semiconductor regions of the said one conductivity type extending through the epitaxial layer to form electrical contact regions to one of the said two regions, the said one region providing a resistive path between the contact regions, and an annular region of semiconductor material of the said one conductivity type extending through the epitaxial layer around the periphery of and contacting the other one of the said two regions. This device can be manufactured by modification of the steps required during manufacture of the electrical resistor, by the above described method according to the invention. During the first mentioned diffusion of the said one conductivity type, a further diffused region of like diffusion depth and impurity concentration is also formed in the body and the epitaxial layer is formed also to cover the further diffused region. During the second diffusion of the impurity of said one type conductivity, there is also formed an annular region of said one conductivity type which has like impurity concentration as that of the said contact regions and extends through the epitaxial layer around the periphery of and contacting the further diffused region. One or more diffusions can be made into the epitaxial layer to form an electrical circuit component in the portion of the epitaxial layer enclosed by the said annular region. 85

By way of example, embodiments of the

invention will be described in greater detail with reference to the accompanying drawings, in which:—

Figures 1a and 1b, collectively, show a single substrate after the first p-type diffusion upon which six different circuit devices are to be fabricated concurrently;

Figures 2a and 2b, collectively, show the substrate of Figures 1a and 1b after the pre-epitaxial n-type diffusion step of the process;

Figures 3a and 3b, collectively, show the substrate of Figures 2a and 2b after the formation of an epitaxial layer;

Figures 4a and 4b, collectively, show the substrate of Figures 3a and 3b after the second p-type diffusion step forming isolation rings and collector contacts;

Figures 5a and 5b, collectively, show the substrate of Figures 4a and 4b after the third p-type diffusion step of the process; and

Figures 6a and 6b, collectively, show the substrate of Figures 5a and 5b after the second n-type diffusion step of the process and also illustrate a substantially completed integrated circuit including a sub-epitaxial resistor in accordance with this invention.

Referring now to the drawings, and particularly to Figures 1a and 1b, the starting material for fabricating integrated circuit devices in accordance with a specific embodiment of this invention is a slice 10 of single crystal n-type silicon having a polished surface oriented three to five degrees off the 1-1-1 plane. The silicon may be doped with phosphorous and typically has a resistivity of about 10-20 ohm-cm. Each of the individual diffusion steps herein described may be carried out using conventional techniques which are well known and will not be described in detail herein. The first diffusion step is made through a silicon dioxide or other conventional masking layer 12 formed over one surface of substrate 10 and having diffusion windows 14 formed over predetermined areas of the substrate. A p-type impurity, preferably boron, is diffused through the window 14 in a conventional manner to form p-type conductivity regions 16a-16f. This diffusion, which is of a non-critical nature, is typically made to a depth of approximately 0.7 mil and results in a surface concentration of about 5×10^{15} atoms/cm³. The p-type region 16b will ultimately form the collector of a PNP transistor, region 16c will form a subepitaxial diffused resistor according to the invention, region 16e a back gate for an n-channel FET, and regions 16a, 16d and 16f will provide electrical isolation of an NPN transistor, a surface diffused resistor and a p-channel FET.

Next a diffusion window 20 is cut in the oxide 18 over the p-type region 16a, as illustrated in Figures 2a and 2b. N-type

impurities, such as antimony or arsenic, are then diffused through window 20 in a conventional manner to form the relatively heavily doped n-type region 22. In a preferred embodiment, antimony is the impurity employed. Diffusion is to a depth of about 0.3 mil with a surface concentration of approximately 10^{19} atoms/cm³. Region 22 will form a low resistivity subsurface path for current to the collector region of the NPN transistor.

Next the oxide layer is stripped and a lightly doped n-type epitaxial layer 24 is grown over the silicon slice as illustrated in Figures 3a and 3b. Any suitable epitaxial process can be used for this purpose such as the known process wherein silane tetrachloride (SiCl₄) carried by hydrogen gas is thermally decomposed by passing the gaseous mixture over the substrate when heated to about 1250°C. for about five minutes. The epitaxial layer is preferably formed in an antimony atmosphere which furnishes n-type impurities to produce the relatively lightly doped n-type layer 24. The epitaxial layer may typically be about 0.5 mil thick and have a resistance of about 2.0 ohms-cm.

Next a p-type impurity, preferably boron, is diffused into epitaxial layer 24 to form regions 26a-26f. With an epitaxial layer thickness of about 0.5 mil, this diffusion is typically made about 0.5-0.6 mil deep to extend through the epitaxial layer and has a relatively heavy surface concentration of about 10^{20} atoms/cm³. The diffused region 26b provides a low resistivity current path to the underlying collector region 16b of the PNP transistor. Region 26c is separated in two parts located at opposite ends of the subepitaxial resistor 16c to provide surface contact regions to the ends of the buried resistor. Region 26e establishes deep ohmic contact with diffused region 16e which is the back gate of an n-channel field effect transistor. Regions 26a, 26d and 26f extend around the peripheries of regions 16a, 16d and 16f and form electrical isolation rings in the conventional manner.

As illustrated in Figures 5a and 5b, a p-type diffusion, preferably boron, is then made in regions 28a, 28b, 28d-28f to convert the epitaxial layer from n-type conductivity to p-type conductivity. A typical diffusion depth is about 0.25 mil with a surface concentration of about 10^{18} atoms/cm³. Region 28a forms the base of the NPN transistor. Region 28b forms the emitter of the PNP transistor. Region 28d forms a diffused surface resistor. Region 28e forms a gate diffusion for an n-channel field effect transistor, and region 28f forms the channel for the p-channel field effect transistor.

Finally, an n-type impurity, preferably phosphorous, is diffused to form n-type

conductivity regions 30-36 as shown in Figures 6a and 6b. The depth of this diffusion is typically about 0.18 mil and the surface concentration is approximately 10^{21} atoms/cm³. Diffused region 30 forms the emitter of the NPN transistor. Region 31 provides a means for establishing ohmic contact with the high impurity concentration n-type region 22 which provides a low resistivity current path to the active collector region of the NPN transistor. The diffused regions 32 may be placed around any one or more of the components to form a guard ring and prevent surface inversion. Regions 33 and 34 provide a source and a drain contact, respectively, for the n-channel field effect transistor, and region 35 forms a diffused front gate region for the p-channel field effect transistor.

The subepitaxial diffused resistor constructed in the integrated circuit by this process enables the circuit to operate under high voltage conditions without the breakdown problems of surface resistors built by prior art processes. Placing the lightly doped low conductivity p-type regions below the epitaxial layer eliminates inversion difficulties, and minimizes breakdowns attributable to surface defects of the initial material and defects induced by the diffusion processes. Surface inversion is no problem because the resistor is well below the surface. Degradation from defects in the starting material is minimized because the density of such defects tends to decrease beneath the surface. Since surface inversion is no problem, the sheet resistance of the subepitaxial resistor may be as much as five times the sheet resistance of a standard surface diffusion. For example, nominal values for standard surface diffused resistors are 150 ohms per square, as opposed to 750 ohms per square available in subepitaxial resistors fabricated in accordance with this invention. Thus, not only is more resistance obtainable for less length, the use of such subsurface resistors allows more complex connections to be achieved, since the resistors form another level of interconnections which tunnel under other circuit elements and surface interconnections.

From Figures 6a and 6b, it will be noted that the process heretofore described can be used to concurrently fabricate NPN and PNP transistors, subepitaxial resistors, diffused surface resistors, n-channel field effect transistors, and p-channel field effect transistors. The subepitaxial n-type region under the NPN device provides a collector saturation resistance on the order of 50 to 100 times better than present topside contact devices on complementary monolithic structures. Further, the collector-base breakdown voltages are substantially equal on both the PNP and NPN devices. In addition to these advantages, this process permits the

construction of a PNP device having an extremely high emitter-base breakdown voltage, typically about 100 volts.

This process is also described in co-pending Application No. 35772/67 (Serial No. 1,193,693) from which the present Application has been divided.

Although a preferred embodiment of the invention has been described in detail, it is to be understood that various changes, substitutions and alterations can be made therein without departing from the invention as defined by the appended claims.

WHAT WE CLAIM IS:—

1. An electrical resistor device comprising a diffused region of semiconductor material of one conductivity type in a body of semiconductor material of opposite conductivity type, which region extends to a surface of the semiconductor body and is covered by an epitaxial layer of semiconductor material of the said opposite conductivity type, and spaced semiconductor regions of the said one conductivity type extending through the epitaxial layer to form electrical contact regions to the said resistor region.

2. An electrical circuit device including two diffused regions of semiconductor material of one conductivity type in a body of semiconductor material of opposite conductivity type, both regions having like impurity concentrations and extending like depths into the body from a common surface of the body at which they are covered by an epitaxial layer of the said opposite conductivity type, spaced semiconductor regions of the said one conductivity type extending through the epitaxial layer to form electrical contact regions to one of the said two regions, the said one region providing a resistive path between the contact regions, and an annular region of semiconductor material of the said one conductivity type extending through the epitaxial layer around the periphery of and contacting the other one of the said two regions.

3. A device according to Claim 2, in which the said annular region together with the said other region electrically isolates the region of the epitaxial layer enclosed by the said annular region, the said isolated region containing or forming part of an electrical circuit component.

4. A device according to Claim 2 or 3, in which the said contact regions and the said annular region have a higher impurity concentration than the two regions of the said one conductivity type.

5. A device according to any one of the preceding claims, in which the said one conductivity type is p-type.

6. A resistor device according to Claim 1,

conductivity regions 30-36 as shown in Figures 6a and 6b. The depth of this diffusion is typically about 0.18 mil and the surface concentration is approximately 10^{21} atoms/cm³. Diffused region 30 forms the emitter of the NPN transistor. Region 31 provides a means for establishing ohmic contact with the high impurity concentration n-type region 22 which provides a low resistivity current path to the active collector region of the NPN transistor. The diffused regions 32 may be placed around any one or more of the components to form a guard ring and prevent surface inversion. Regions 33 and 34 provide a source and a drain contact, respectively, for the n-channel field effect transistor, and region 35 forms a diffused front gate region for the p-channel field effect transistor.

The subepitaxial diffused resistor constructed in the integrated circuit by this process enables the circuit to operate under high voltage conditions without the breakdown problems of surface resistors built by prior art processes. Placing the lightly doped low conductivity p-type regions below the epitaxial layer eliminates inversion difficulties, and minimizes breakdowns attributable to surface defects of the initial material and defects induced by the diffusion processes. Surface inversion is no problem because the resistor is well below the surface. Degradation from defects in the starting material is minimized because the density of such defects tends to decrease beneath the surface. Since surface inversion is no problem, the sheet resistance of the subepitaxial resistor may be as such as five times the sheet resistance of a standard surface diffusion. For example, nominal values for standard surface diffused resistors are 150 ohms per square, as opposed to 750 ohms per square available in subepitaxial resistors fabricated in accordance with this invention. Thus, not only is more resistance obtainable for less length, the use of such subsurface resistors allows more complex connections to be achieved, since the resistors form another level of interconnections which tunnel under other circuit elements and surface interconnections.

From Figures 6a and 6b, it will be noted that the process heretofore described can be used to concurrently fabricate NPN and PNP transistors, subepitaxial resistors, diffused surface resistors, n-channel field effect transistors, and p-channel field effect transistors. The subepitaxial n-type region under the NPN device provides a collector saturation resistance on the order of 50 to 100 times better than present topside contact devices on complementary monolithic structures. Further, the collector-base breakdown voltages are substantially equal on both the PNP and NPN devices. In addition to these advantages, this process permits the

construction of a PNP device having an extremely high emitter-base breakdown voltage, typically about 100 volts.

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Although a preferred embodiment of the invention has been described in detail, it is to be understood that various changes, substitutions and alterations can be made therein without departing from the invention as defined by the appended claims.

WHAT WE CLAIM IS:—

1. An electrical resistor device comprising a diffused region of semiconductor material of one conductivity type in a body of semiconductor material of opposite conductivity type, which region extends to a surface of the semiconductor body and is covered by an epitaxial layer of semiconductor material of the said opposite conductivity type, and spaced semiconductor regions of the said one conductivity type extending through the epitaxial layer to form electrical contact regions to the said resistor region.
2. An electrical circuit device including two diffused regions of semiconductor material of one conductivity type in a body of semiconductor material of opposite conductivity type, both regions having like impurity concentrations and extending like depths into the body from a common surface of the body at which they are covered by an epitaxial layer of the said opposite conductivity type, spaced semiconductor regions of the said one conductivity type extending through the epitaxial layer to form electrical contact regions to one of the said two regions, the said one region providing a resistive path between the contact regions, and an annular region of semiconductor material of the said one conductivity type extending through the epitaxial layer around the periphery of and contacting the other one of the said two regions.
3. A device according to Claim 2, in which the said annular region together with the said other region electrically isolates the region of the epitaxial layer enclosed by the said annular region, the said isolated region containing or forming part of an electrical circuit component.
4. A device according to Claim 2 or 3, in which the said contact regions and the said annular region have a higher impurity concentration than the two regions of the said one conductivity type.
5. A device according to any one of the preceding claims, in which the said one conductivity type is p-type.
6. A resistor device according to Claim 1,



substantially as described herein with reference to the accompanying drawings.

7. A method of manufacturing an electrical resistor device, including the steps of:

5 a) diffusing impurity of one conductivity type into a body of semiconductor material of opposite conductivity type to form a diffused region of the said one conductivity type extending to a surface of the body,

10 b) forming an epitaxial layer of semiconductor material of the said opposite conductivity type on the said surface of the body to cover the said diffused region, and

15 c) diffusing impurity of the said one conductivity type at selected spaced locations through the epitaxial layer to form electrical contact regions to the said diffused region which provides an electrically resistive path between the said contact regions.

20 8. A method according to Claim 7, in which:

the said step a) also forms in the body a further diffused region of like diffusion depth and impurity concentration,

25 the epitaxial layer formed by said step b) also covers the said further diffused region, and

the said step c) also forms an annular region of the said one conductivity type having like impurity concentration as that of the said contact regions and extending through the epitaxial layer around the periphery of and contacting the further diffused region.

9. A method according to claim 8, including the steps of effecting one or more diffusions into the epitaxial layer to form an electrical circuit component in the portion of the epitaxial layer enclosed by the said annular region.

10. A method according to Claim 7 or Claim 8, in which the impurity concentration in the regions produced by the said step c) is higher than that in the region(s) produced by the said step a).

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