WIRE SWEEP RESISTANT SEMICONDUCTOR PACKAGE AND MANUFACTURING METHOD THEREOF

TECHNICAL FIELD

The present invention relates generally to integrated circuits, and more particularly to package structures for integrated circuits.

BACKGROUND ART

In the electronics industry, a continuing objective is to further and further reduce the size of electronic devices while simultaneously increasing performance and speed. Cellular telephones, personal data devices, notebook computers, camcorders, and digital cameras are but a few of the consumer products that require and benefit from this ongoing miniaturization of sophisticated electronics.

Integrated circuit ("IC") assemblies for such complex electronic systems typically have a large number of interconnected IC chips. The IC chips, commonly called dies, are usually made from a semiconductor material such as silicon or gallium arsenide. Photolithographic techniques are used to form the various semiconductor devices in multiple layers on the dies.

Dies are encapsulated in a molded plastic package that has connectors or leads on the exterior of the package that function as input/output terminals for the die inside the package. The package includes an interposer and a die mounted on the top surface of the interposer.

The interposer may be comprised of a flexible resin tape, a rigid fiber-glass/copper sheet laminate, a co-fired ceramic coupon, a flexible metal lead frame, a ball grid array substrate or other well-known types of interposers in the semiconductor industry, depending on the particular type of semiconductor package being used.

The die is conventionally mounted to the top surface of the interposer with, for example, a layer of an adhesive or an adhesive film, and then electrically connected to the interposer by a number of fine, conductive wires, typically gold (Au) or aluminum (Al), that electrically connect the die to the interposer. The wires are attached to the die at the bonding pads of the die, which are located around the periphery of the die.

After one or more dies are wire bonded to the interposer, the dies, the interposer, and conductive wires are encapsulated in a mold material, such as plastic or epoxy, or in a multi-part housing made of plastic, ceramic, or metal. The encapsulation protects the interposer, the fine conductive wires, and the die from physical, electrical, moisture, and/or chemical damage.

Because of their fineness, wire sweep of the fine conductive wires is a constant problem during the encapsulation of a semiconductor die. The high viscosity of the encapsulation material in its liquid state during the encapsulation process drags the wires along the flow path of the material, causing the wires to bend away from their original upright positions. Wire sweep poses a reliability risk to the functionality of the semiconductor device. Wires that are swept may come in contact with each other causing shorts in the device. Wires that are swept may also touch the surface of the semiconductor die, which would cause shorts between different components on the die. Therefore, it is always desirable to keep the wire sweep level to a minimum to protect the functional integrity of the semiconductor device.

Certain factors contribute to the overall difficulty in limiting the wire sweep. As stated previously, flowing molding material exerts a drag force on the wires. If this force exceeds the strength of the wires or of the bonds, then the wires will bend. Longer wires tend to bend more easily than shorter wires; therefore, it is desirable to keep the wire lengths as short as possible. However, it is not always possible to keep the wire lengths short.

Another factor that contributes to the difficulty of controlling wire sweep is the proximity of the wires to each other. The closer the wires are together, the harder it is to reduce the possibility of wires coming into contact with each other. Miniaturization of circuit patterns on semiconductor dies results in wires being located closer together. Moreover, die designers are putting more components on a single die to expand its functions. Expanded functionality of each die results in more wires. More wires and smaller die circuit geometry require that the wires be much closer together, making wire sweep control far more difficult.

Thus, a need still remains to effectively control wire sweep. In view of the ever-increasing need to save costs and improve efficiencies, it is more and more critical that answers be found to this problem.

Solutions to this problem have been long sought but prior developments have not taught or suggested any and thus, answers to this phenomena have eluded those skilled in the art.

DISCLOSURE OF THE INVENTION

The present invention provides a method for manufacturing a wire sweep resistant semiconductor package. A die is attached to an interposer, and the die is electrically connected to the interposer with conductive wires. A sealant is applied to the conductive wires and optionally the die to prevent wire sweep, the sealant being applied free of contact with the interposer. The die, the interposer, the conductive wires, and the sealant are enclosed in an encapsulant.

Certain embodiments of the invention have other advantages in addition to or in place of those mentioned above. The advantages will become apparent to those skilled in the art from a reading of the following detailed description when taken with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a side cross-sectional view of a wire sweep resistant semiconductor package in an intermediate stage of manufacture;

FIG. 2 is a cross-sectional view of the structure of FIG. 1 after application of a sealant, taken on cross sectional line 2-2 in FIG. 3;

FIG. 3 is a top view of the structure of FIG. 2;

FIG. 4 is the structure of FIG. 2 after application and molding of an encapsulant;

FIG. 5 is a cross-sectional view, taken on cross sectional line 5-5 in FIG 6, of an alternate embodiment of a wire sweep resistant semiconductor package, in accordance with the present invention;

FIG. 6 is a top view of the structure of FIG. 5;

FIG. 7 is a top view of another embodiment of a wire sweep resistant semiconductor package, in accordance with the present invention;

FIG. 8 is a top view of still another embodiment of a wire sweep resistant semiconductor package in accordance with the present invention;

FIG. 9 is a side cross-sectional view of a still another alternate embodiment of a wire sweep resistant semiconductor package in accordance with the present invention; and

FIG. 10 is a flow chart of a method for manufacturing a wire sweep resistant semiconductor package in accordance with the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

In the following description, numerous specific details are given to provide a thorough understanding of the invention. However, it will be apparent that the invention may be practiced without these specific details. In order to avoid obscuring the present invention, some well-known package configuration structural components and process steps are not disclosed in detail.

The drawings showing embodiments of the invention are semi-diagrammatic and not to scale and, particularly, some of the dimensions are for the clarity of presentation and are shown exaggerated in the FIGs. Also, where multiple embodiments are disclosed and described having some features in common, for clarity and ease of illustration, description, and comprehension thereof, like features one to another will ordinarily be described with like reference numerals.

The term “horizontal” as used herein is defined as a plane parallel to the conventional plane or surface of a die, die paddle (or “pad”), or die package, regardless of its orientation. The term “vertical” refers to a direction perpendicular to the horizontal as just defined. Terms, such as “on”, “above”, “below”, “bottom”, “top”, “side” (as in “sidewall”), “higher”, “lower”, “over”, and “under”, are defined with respect to the horizontal plane.

The term “processing” as used herein includes deposition of material, patterning, exposure, development, etching, cleaning, and/or removal of the material as required in forming a described structure.

Referring now to FIG. 1, therein is shown a side cross-sectional view of a wire sweep resistant semiconductor package 100 in an intermediate stage of manufacture. A die 102 is attached by an epoxy 104 to an interposer 106. The interposer 106 may be comprised of a flexible resin tape, a rigid fiber-glass/copper sheet laminate, a co-fired ceramic coupon, a flexible metal lead frame, a ball grid array substrate or other well-known types of interposers in the semiconductor industry, depending on the particular type of semiconductor package 100 being used.

The die 102 is then electrically connected to the interposer 106 by a number of fine, conductive wires 108, typically gold or aluminum. The wires 108 are wire bonded to the die 102 around the periphery of the die 102, typically with automated wire bonding equipment employing well-known thermal-compression or ultrasonic wire bonding techniques.

Because of their fineness, wire sweep of the fine conductive wires 108 is a problem during the encapsulation of the die 102. During the encapsulation process, encapsulation

materials in a high viscosity liquid state drag the wires 108 along the flow path of the material. This causes wire sweep, the bending of wires 108 away from their original upright positions.

Wire sweep poses a reliability risk to the functionality of semiconductor devices. Wires that are swept may come in contact with each other causing short circuits in the device. Wires that are swept may also touch the surface of dies, which would cause short circuits between different components on the dies. Therefore, it is always desirable to keep the wire sweep level to a minimum to protect the functional integrity of dies.

Referring now to FIG. 2, therein is shown a cross-sectional view of the structure of FIG. 1 after application of a sealant, taken on cross sectional line 2-2 in FIG. 3. A sealant 202, such as a liquid, gel, paste, or high thermal film, is applied directly on the die 102 where the wires 108 are bonded. The sealant 202 prevents wire sweep of the wires 108 by securing the wires 108 at their bonded positions on the die 102. These are the highest points of the securing wires 108 and the most likely to be affected by the flow of the encapsulant material.

Referring now to FIG. 3, therein is shown a top view of the structure of FIG. 2. The sealant 202 is attached directly on top of the die 102 and encloses the ends of the wires 108 where they are bonded to the die 102. However, the sealant 202 is in contact with the die 102 and free of contact with the interposer 106.

There are several advantages to the sealant 202 being free of contact with the interposer 106. One advantage is the reduction of problems associated with the risk of delamination. For example, it is easier to look for sealant 202 material properties without considering interposer 106 adhesions. Another advantage is in the case of packages wherein the leadframe is used as an interposer 106. In this case, the leadframe is open from the die paddle area to the leadfinger area. Therefore, the only location possible to dispense the sealant 202 is on the wires 108. Yet another advantage is that a smaller volume of sealant 202 is needed, thus making the process more economical.

Referring now to FIG. 4, therein is shown the structure of FIG. 2 after encapsulation. The die 102, the epoxy 104, the interposer 106, the wires 108, and the sealant 202 have all been encapsulated through molding or glob top processes in an encapsulant 402. By securing the wires 108, the sealant 202 has prevented wire sweep.

Referring now to FIG. 5, therein is shown a cross-sectional view, taken on cross sectional line 5-5 in FIG 6, of an alternate embodiment of a wire sweep resistant semiconductor package 500, in accordance with the present invention. A die 502 is attached

by an epoxy 504 to an interposer 506. A number of fine, conductive wires 508 electrically connect the die 502 to the interposer 506.

A sealant 516, such as a liquid, gel, paste, or high thermal film, dispensed directly on the fine, conductive wires 508, is free of contact with the die 502 or the interposer 506. The sealant 516 secures the fine conductive wires 508 at any position along the length of the fine conductive wires 508 or completely covering (not shown) the fine conductive wires 508. The sealant 516 prevents wire sweep of the wires 508 by securing the wires 508 in a fixed position. The die 502, the epoxy 504, the interposer 506, the wires 508, and the sealant 516 are all then encapsulated in an encapsulant 518.

Referring now to FIG. 6, therein is shown a top view of the structure of FIG. 5, with the encapsulant 518 omitted for clarity of illustration. The sealant 516 secures the fine conductive wires 508. However, the sealant 516 is free of contact with the die 502 or the interposer 506.

Referring now to FIG. 7, therein is shown a top view of another embodiment of a wire sweep resistant semiconductor package 700, in accordance with the present invention. A die 702 is attached by an epoxy (not shown, but see the epoxy 104 in FIG. 1) to an interposer 704. A first discrete drop 708 of a sealant secures a first distinct group of fine conductive wires 706. A second discrete drop 712 of a sealant secures a second distinct group of fine conductive wires 710. A third discrete drop 716 of a sealant secures a third distinct group of fine conductive wires 714. A fourth discrete drop 720 of a sealant secures a fourth distinct group of fine conductive wires 718.

Several distinct groups may be formed using different, distinct conductive wires and/or including some of the same conductive wires. For example, of eight wires numbered one to eight, distinct groups could be, for example: 1-2-3-4, 3-4-5-6, 5-6-7-8, and 7-8-1-2. In addition, not all the wires have to be secured, and such distinct groups could be, for example: 1-2-3 and 5-6-7. Furthermore, the drops do not have to be the same size, so other distinct groups could be, for example: 1-2-3-4-5-6 and 7-8.

The drops 708, 712, 716, and 720 are free of contact with each other, the die 702, or the interposer 704. The die 702, the epoxy (not shown), the interposer 704, the wire groups 706, 710, 714, and 718, unsecured fine conductive wires 722, and the sealants 708, 712, 716, and 720 are all encapsulated in an encapsulant (not shown, but see the encapsulant 402 in FIG. 4).

Referring now to FIG. 8, therein is shown a top view of still another embodiment of a wire sweep resistant semiconductor package 800, in accordance with the present invention. A die 802 is attached by an epoxy (not shown, but see the epoxy 104 in FIG. 1) to an interposer 804. Fine conductive wires 806 are secured by a first application 808 of a sealant and a second application 810 of the sealant. The first application 808 and the second application 810 are free of contact with each other, the die 802, or the interposer 804. The die 802, the epoxy (not shown), the interposer 804, the wires 806, the first application 808, and the second application 810 are all encapsulated in an encapsulant (not shown, but see the encapsulant 402 in FIG. 4).

Referring now to FIG. 9, therein is shown a side cross-sectional view of still another alternate embodiment of a wire sweep resistant semiconductor package 900, in accordance with an embodiment of the present invention. A die 902 is attached by an epoxy 904 to an interposer 906. A number of fine, conductive wires 908 electrically connect the die 902 to the interposer 906. A sealant 912 secures the fine conductive wires 908 by entirely covering the die 902 and covering the fine, conductive wires 908 where they are bonded to the die 902. The sealant 912 does not contact the interposer 906. The die 902, the epoxy 904, the interposer 906, the fine conductive wires 908, and the sealant 912 are all encapsulated in an encapsulant 914.

Referring now to FIG. 10, therein is shown a flow chart of a method 1000 for manufacturing a wire sweep resistant semiconductor package in accordance with an embodiment of the present invention. The method 1000 includes providing a die attached to an interposer in a block 1002; electrically connecting the die to the interposer by a plurality of conductive wires in a block 1004; applying a sealant to the die and the conductive wires to prevent wire sweep, the sealant being free of contact with the interposer in a block 1006; and encapsulating the die, the, interposer the conductive wires, and the sealant in an encapsulant in a block 1008.

Thus, it has been discovered that the wire sweep resistant method and apparatus of the present invention furnish important and heretofore unknown and unavailable solutions, capabilities, and functional advantages for preventing wire sweep. The resulting process and configurations are straightforward, economical, uncomplicated, highly versatile, accurate, sensitive, and effective, and can be implemented by adapting known components for ready manufacturing, application, and utilization.

While the invention has been described in conjunction with a specific best mode, it is to be understood that many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the aforegoing description. Accordingly, it is intended to embrace all such alternatives, modifications, and variations which fall within the scope of the included claims. All matters hithertofore set forth herein or shown in the accompanying drawings are to be interpreted in an illustrative and non-limiting sense.

THE INVENTION CLAIMED IS:

1. A method for manufacturing a wire sweep resistant semiconductor package, comprising:

providing a die attached to an interposer ;

electrically connecting the die to the interposer with conductive wires;

applying a sealant to the conductive wires and optionally the die to prevent wire sweep, the sealant being applied free of contact with the interposer; and

encapsulating the die, the interposer , the conductive wires, and the sealant in an encapsulant.

2. The method of claim 1 wherein applying the sealant to the conductive wires and optionally the die to prevent wire sweep further comprises applying the sealant to the conductive wires with the sealant completely covering the conductive wires and touching only the conductive wires.

3. The method of claim 1 wherein applying the sealant to the conductive wires and optionally the die to prevent wire sweep further comprises applying discrete drops of the sealant to distinct groups of the conductive wires with each drop of the sealant touching only a respective distinct group of the conductive wires.

4. The method of claim 1 wherein applying the sealant to the conductive wires and optionally the die to prevent wire sweep further comprises:

applying a first application of the sealant to the conductive wires with the first application of the sealant touching only the conductive wires; and

applying a second application of the sealant to substantially the same conductive wires with the second application of the sealant touching only the conductive wires.

5. The method of claim 1 wherein applying the sealant to the conductive wires and optionally the die to prevent wire sweep further comprises applying the sealant to the die and the conductive wires with the sealant entirely covering the die and touching only the die and the conductive wires.

6. A method for manufacturing a wire sweep resistant semiconductor package, comprising:

providing a die attached by an epoxy to a interposer;

electrically connecting the die to the interposer with conductive wires connected around the periphery of the die;

applying a sealant to the conductive wires and optionally the die to prevent wire sweep, the sealant being applied free of contact with the interposer; and

encapsulating the die, the epoxy, the interposer, the conductive wires, and the sealant in an encapsulant.

7. The method of claim 6 wherein applying the sealant to the conductive wires and optionally the die to prevent wire sweep further comprises applying the sealant to the conductive wires with the sealant completely covering the conductive wires and touching only the conductive wires.

8. The method of claim 6 wherein applying the sealant to the conductive wires and optionally the die to prevent wire sweep further comprises:

applying a first drop of the sealant to a first group of conductive wires, the first drop of the sealant touching only the first group of conductive wires;

applying a second drop of the sealant to a second group of conductive wires, the second drop of the sealant touching only the second group of conductive wires;

applying a third drop of the sealant to a third group of conductive wires, the third drop of the sealant touching only the third group of conductive wires; and

applying a fourth drop of the sealant to a fourth group of conductive wires, the fourth drop of the sealant touching only the fourth group of conductive wires.

9. The method of claim 6 wherein applying the sealant to the conductive wires and optionally the die to prevent wire sweep further comprises:

applying a first application of the sealant to the conductive wires with the first application of the sealant touching only the conductive wires; and

applying a second application of the sealant to substantially the same conductive wires with the second application of the sealant touching only the conductive wires.

10. The method of claim 6 wherein applying the sealant to the conductive wires and optionally the die to prevent wire sweep further comprises applying the sealant to the die and the conductive wires with the sealant entirely covering the die, covering the wires at their connected positions on the die, and touching only the die and the conductive wires.

11. A wire sweep resistant semiconductor package, comprising:

a die attached to an interposer;

conductive wires electrically connecting the die to the interposer;

a sealant applied to the conductive wires and optionally the die to prevent wire sweep, the sealant being free of contact with the interposer; and

an encapsulant encapsulating the die, the interposer, the conductive wires, and the sealant.

12. The semiconductor package of claim 11 wherein the sealant applied to the conductive wires and optionally the die to prevent wire sweep further comprises a sealant that touches only the conductive wires.

13. The semiconductor package of claim 11 wherein the sealant applied to the conductive wires and optionally the die to prevent wire sweep further comprises discrete drops of the sealant applied to distinct groups of conductive wires with each drop of the sealant touching only a respective distinct group of the conductive wires.

14. The semiconductor package of claim 11 wherein the sealant applied to the conductive wires and optionally the die to prevent wire sweep further comprises:

a first application of the sealant applied to the conductive wires to prevent wire sweep, the first application of the sealant touching only the conductive wires; and

a second application of the sealant applied to substantially the same conductive wires to prevent wire sweep, the second application of the sealant touching only the conductive wires.

15. The semiconductor package of claim 11 wherein the sealant applied to the conductive wires and optionally the die to prevent wire sweep further comprises the sealant entirely covering the die and touching only the die and the conductive wires.

16. A wire sweep resistant semiconductor package, comprising:

a die;

an interposer ;

an epoxy attaching the die to the interposer;

conductive wires around the periphery of the die electrically connecting the die to the interposer;

a sealant applied to the conductive wires and optionally the die to prevent wire sweep, the sealant being free of contact with the interposer; and

an encapsulant encapsulating the die, the epoxy, the interposer, the conductive wires, and the sealant.

17. The semiconductor package of claim 16 wherein the sealant applied to the conductive wires and optionally the die to prevent wire sweep further comprises the sealant completely covering the conductive wires and touching only the conductive wires.

18. The semiconductor package of claim 16 wherein the sealant applied to the conductive wires and optionally the die to prevent wire sweep further comprises:

a first drop of the sealant applied to a first group of conductive wires, the first drop of the sealant touching only the first group of conductive wires;

a second drop of the sealant applied to a second group of conductive wires, the second drop of the sealant touching only the second group of conductive wires;

a third drop of the sealant applied to a third group of conductive wires, the third drop of the sealant touching only the third group of conductive wires; and

a fourth drop of the sealant applied to a fourth group of conductive wires, the fourth drop of the sealant touching only the fourth group of conductive wires.

19. The semiconductor package of claim 16 wherein the sealant applied to the conductive wires and optionally the die to prevent wire sweep further comprises:

a first application of the sealant applied to the conductive wires to prevent wire sweep, the first application of the sealant touching only the conductive wires; and

a second application of the sealant applied to substantially the same conductive wires to prevent wire sweep, the second application of the sealant touching only the conductive wires.

20. The semiconductor package of claim 16 wherein the sealant applied to the conductive wires and optionally the die to prevent wire sweep further comprises the sealant entirely covering the die, covering the wires at their connected positions on the die, and touching only the die and the conductive wires.