

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
27 May 2004 (27.05.2004)

PCT

(10) International Publication Number
WO 2004/044752 A2

(51) International Patent Classification⁷: **G06F 12/00**

(21) International Application Number:
PCT/US2003/034439

(22) International Filing Date: 29 October 2003 (29.10.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/290,888 8 November 2002 (08.11.2002) US

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(81) Designated States (*national*): AE, AG, AL, AM, AT, AU,
AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU,
CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH,
GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC,
LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW,
MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC,
SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA,
UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM,
KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW),
Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE,
ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO,
SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM,
GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished
upon receipt of that report*

*For two-letter codes and other abbreviations, refer to the "Guid-
ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.*

(54) Title: MEMORY CONTROLLERS WITH INTERLEAVED MIRRORED MEMORY MODES

(57) Abstract: In some embodiments, a memory controller includes first and second memory channel interfaces and memory access control circuitry. The memory access control circuitry is to send first and second primary data sections to the first and second memory channel interfaces, respectively, and send first and second redundant data sections to the second and first memory channel interfaces, respectively. The first and second redundant data sections are redundant with respect to the first and second primary data sections, respectively. Other embodiments are described and claimed.



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