MULTICHIP WAFER LEVEL SYSTEM PACKAGES AND METHODS OF FORMING SAME

TECHNICAL FIELD

Field of the Invention: The present invention relates generally to semiconductor packaging. More particularly, the present invention relates to wafer level multichip packaging such as, for example, a system in a package solution.

BACKGROUND

State of the Art: Semiconductor chips (also referred to as die/dice herein) are found in many electronic products today. As semiconductor dice get smaller and more complex, the problem of making electrical connections between semiconductor dice, connections to carrier substrates such as printed circuit boards, and connections to intermediate substrates such as multichip modules which are, in turn, connected to carrier substrates has been addressed with a variety of constantly evolving solutions.

One of the earlier solutions included wire bonding from signal connection devices, such as bond pads of a semiconductor die, to pins or leads of a lead frame contained in a ceramic or plastic package. Finished packages are mounted to a carrier substrate, such as a printed circuit board, where the pins or leads make electrical connection with contact pads on the carrier substrate.

The term “signal connection devices” as used herein regarding semiconductor devices includes not only contact pads of a substrate and bond pads of a semiconductor device but also I/O connections for a semiconductor device created by adding circuitry from bond pads located on the active surface of the semiconductor device to different locations on the active surface of the semiconductor device. Such additional circuitry is typically effected using a so-called “redistribution layer” extending over the active surface or a surface of a semiconductor die.

An evolution of electrical connection technology occurred when multiple semiconductor dice were mounted on an intermediate substrate. In this instance, the semiconductor dice are typically connected to a lead frame by way of bonding wires. Signals, or electrical connections, required for coupling with an external device, such as a circuit board, are brought out to contact pads, pins or leads of the multichip module

package. Other signals or electrical interconnections may be established between multiple semiconductor dice by way of circuitry formed on the intermediate substrate.

In these solutions, using wires for connecting a semiconductor die to a substrate and wire bonding processes can create problems. Such problems may include, for example, size and pitch (spacing) requirements for the bond pads of the semiconductor die and contact pads of the substrate; inductance in the signals due to the long curved wires; wire bond breakage and wire sweep causing shorting between adjacent wires; and high signal frequency semiconductor dice making the wire bonding process difficult and expensive.

Flip-chip technologies using solder balls or bumps have helped to alleviate some of these problems. For example, instead of wire bonding, conductive bumps such as, for example, balls of solder may be formed at the locations of the bond pads of a semiconductor die. A specialized lead frame, a dielectric tape carrying circuit traces as used in tape automated bonding processes, or other carrier substrates such as a printed circuit board may have electrical connection locations such as terminals which correspond to the placement of the solder balls on the bond pads of the semiconductor die. The semiconductor die is “flipped” upside down so the solder balls are placed, for example, on the contact pads of a carrier substrate. A solder reflow process heats the solder balls until the solder begins to flow and bond with a corresponding contact pad of a carrier substrate. Upon cooling, the solder forms both mechanical and electrical connections between the carrier substrate and the semiconductor die. This packaging solution may alleviate at least some of the inductance problems, allowing for higher frequency performance and better signal integrity of the semiconductor die. Also, to a certain extent, it allows the contact pads of a substrate where conductive bumps were formed to be larger, more widely pitched and placed anywhere on the semiconductor die active surface rather than just around the periphery or down the center thereof.

Chip scale packaging has evolved from various standard flip-chip processes to a configuration wherein the size of a package is reduced to only slightly larger than the size of the semiconductor die. Chip scale packages are typically created using an interposer substrate. The semiconductor die, with solder balls or bumps such as described above, is attached and electrically connected to the interposer substrate and an encapsulation material is applied over the chip for protection thereof from the elements. The interposer substrate can redistribute signal connections to new locations so they are physically

positioned in a desired pattern or arrangement, or to just a different pitch more suitable for mounting to an interposer substrate. An additional set of conductive bumps may then be formed at other contact pad locations on the interposer substrate. The resulting package may then be attached to a carrier substrate such as a printed circuit board.

Chip scale packaging enables small packages using desired ball grid arrays or fine ball grid arrays. However, the interposer substrate is typically made of an organic material which is the same as, or similar to, that used for printed circuit boards. There is conventionally a significant mismatch in the coefficients of thermal expansion (CTE) of the interposer substrate and the semiconductor die, often resulting in substantial stress on the mechanical and electrical interconnections formed between the semiconductor die and interposer substrate (e.g., a reflowed solder connection) during the normal thermal cycling during normal operation of the semiconductor die. The use of a ceramic substrate may alleviate some of the CTE mismatch concerns but at a considerably higher cost relative to more conventional interposer substrates.

Another advance in the area of multichip modules includes wafer scale integration. Wafer scale integration generally comprises fabricating multiple types of functional semiconductor dice on a single wafer. For example, a four-chip system may be created by placing a microprocessor next to a memory controller and two memory-type semiconductor dice. This pattern may then be repeated across the entire wafer. After fabrication, the wafer is sawed into individual segments with each segment containing the four different functions. However, this approach has not been a very satisfactory solution due to yield problems created by the variations in processes for forming processors and various types of memory-type semiconductor dice. For example, if a defect causes any one of the four functions to be inoperable, the entire segment is defective and not usable.

In addition to that described above, there have been advances in bump technologies where the conductive bumps act as the signal connection device. Conventional solder bumps, in some cases, have been replaced by stud bumps. Stud bumps have conventionally been gold, but copper and plated-type stud bumps have also been used recently. The stud bumps may actually comprise short wires or wire stubs applied to a semiconductor die using a conventional wire bonding process. Stud bumping has the advantages of using a more cost effective wire bonding process for application of the bumps in comparison to the more complex, multistep solder bumping process. Further, conductive and conductor-filled adhesives have also been employed to attach the

conductive bumps to a carrier substrate. The conductive or conductor-filled adhesive may provide an amount of flexibility to the mechanical and electrical connection, thereby compensating for some of the problems associated with the mismatch of CTE often associated with solder bump processes as discussed above.

However, in light of the advances made in fabricating semiconductor device packages, there is a continued need for a reliable, cost effective solution with a higher integration of various functional semiconductor dice in a single package to produce, for example, a system on a semiconductor die solution. There is also a need to create smaller packages with more consistent thermal expansion properties while enabling the redistribution of signal connection devices of the various semiconductor dice to a more convenient, possibly denser, and optionally standard configuration for attachment to a carrier substrate.

Finally, it would be advantageous to provide a system on a chip packaging solution using known good dice, such use thereby increasing the yield of usable packages and, thus, improving the efficiency and cost effectiveness associated with producing such packages.

DISCLOSURE OF INVENTION

The present invention includes new packaging implementation methods to solve or at least reduce some of the problems encountered in the prior art. Generally, the present invention provides a multichip multilayer system on a chip-type solution. Greater integration is accomplished using a plurality and variety of known good dice contained within cavities formed in a separate silicon substrate. The term “variety” includes semiconductor dice of not only different types (microprocessor, logic, memory, etc.) but functionally similar semiconductor dice of different dimensions and I/O arrangements. The present invention also contemplates the use of so-called “known good die,” or KGD, as the semiconductor dice to be packaged.

The present invention enables the use of processes for making silicon-type semiconductor dice for creating additional redistribution and interconnect layers in the same plane or same planes vertically offset from the multichip arrangement. These additional layers may then be terminated with conductive bumps, optionally in a standard configuration, at the top layer for typical flip-chip application of the assembly to a carrier substrate such as printed circuit board or other multichip module substrate.

According to one embodiment of the present invention, a plurality of cavities is etched into the top of a substrate, such as a silicon wafer. The cavities are sized, configured and located to physically receive signal connection devices of a plurality and variety of types of semiconductor dice. The signal connection devices on the semiconductor die may be formed, for example, as gold stud bumps. A semiconductor die attach material adhesive with a high dielectric constant is applied to the top surface of the substrate and in the cavities. The substrate, a wafer, having the semiconductor dice thereon is flipped upside down and placed such that the signal connection devices are received by the cavities with the bond pads on the active surface of each semiconductor die making contact with the die attach material. A layer of molding compound is formed over the top of the substrate and over the backs of the various semiconductor dice. This molding compound creates the package structure, adds mechanical stability, and protects the semiconductor dice from the elements. A portion of the back surface of the substrate is removed, such as by back-grinding or another suitable process, until the signal connection devices are exposed through the back surface of the substrate. With the signal connection devices exposed, a dielectric layer is formed over the entire back surface of the wafer. The dielectric layer is then etched to expose the signal connection devices for use in connection to higher-level packaging.

According to another embodiment of the invention, a plurality of cavities is formed in the top surface of a substrate. The cavities are formed to receive the substantial entirety of each of the various semiconductor dice of a plurality to be packaged. Therefore, the cavities are individually sized and configured to correspond with the bond pads of each individual semiconductor die type that is used. It may be desirable to configure the cavities such that the active surface of a semiconductor die placed therein is approximately flush with the surface of the substrate. A die attach material is placed in the die cavities and the semiconductor dice are placed in the cavities with the active surface of each semiconductor die facing upwards and such that the back surfaces of the semiconductor dice contact the die attach material in the bottoms of the cavities. A dielectric layer is formed over the tops of the semiconductor dice, over the top of the substrate and into any gaps between the dice and the cavity sidewalls. Finally, vias are formed in the dielectric layer to expose signal connection devices on the various semiconductor dice.

The semiconductor device packages according to the present invention may further undergo a redistribution layer (RDL) process to form signal interconnections between semiconductor dice of the package or to redistribute signals from the signal connection device locations of the various types of semiconductor dice to more convenient and optionally standard locations for interconnection with an external device or component. In the redistribution layer process, a metal layer is deposited and patterned to create an interconnect layer from the exposed signal connection device (e.g., contact pad or conductive bump) locations to other locations.

Additional signal layers may be formed if so desired. This signal layering process includes three primary acts: first, a new dielectric layer is formed on the wafer; next, vias are formed in the dielectric layer so connections to an underlying metal layer may be formed; and finally, a new layer of metal is deposited and patterned to create an interconnect on this new layer as well as connections to the underlying layer through the vias.

Once the signal layering process is completed for the number of additional interconnect layers desired, a final interconnect layer is formed. At this juncture, a new dielectric layer is formed on the wafer. Next, openings are formed in the dielectric layer sufficient for the formation of new signal connection devices and for connections to the underlying metal layer. Finally the new signal connection devices, such as conductive bumps in the form of solder balls, are formed in the openings.

At this point, if desired, testing may be accomplished through the solder balls on each of the individual silicon wafer segments containing a complete system on a wafer segment including various types of semiconductor dice. Finally, the process is completed by sawing the wafer into multichip segments, creating a plurality of individual multichip multilayer systems on chip packages, each ready for test and assembly.

BRIEF DESCRIPTION OF DRAWINGS

In the drawings, which illustrate what is currently considered to be the best mode for carrying out the invention:

FIGS. 1A through 1F show cross-sectional views of a system package at various stages of fabrication according to an embodiment of the present invention;

FIGS. 2A through 2D show cross-sectional views of a system package at various stages of fabrication according to another embodiment of the present invention;

FIGS. 3A through 3F show cross-sectional views of a system package including a redistribution layer according to another embodiment of the present invention;

FIG. 4 is a plan view showing a wafer including a plurality of sections, each containing a plurality of semiconductor dice, according to the present invention;

FIG. 5 is a plan view showing a plurality of multichip modules according to the present invention on a memory device; and

FIG. 6 is a block diagram showing a memory device including at least one of the multichip modules according to the present invention incorporated in a computing system.

BEST MODE(S) FOR CARRYING OUT THE INVENTION

Referring to drawing FIGS. 1A through 1F, the process of manufacturing a packaged semiconductor device according to an embodiment of the present invention is shown. Illustrated in drawing FIG. 1A is a cross-sectional view of a bare substrate 102. The substrate 102 material may include a conventional silicon wafer or other bulk silicon substrate such as is well known in the art. However, it is understood that this substrate 102 may comprise other well-known substrates such as a ceramic or other suitable material. A plurality of cavities 105 is formed in the top surface 104 of the substrate 102, such as through a conventional anisotropic silicon etching process. The cavities 105 are each defined by a cavity base 108 and cavity walls 110. As indicated in drawing FIG. 1A, the cavity walls 110 may be formed to exhibit a generally rectangular geometry in cross section such that the cavities 105 are generally cubic in shape. However, the cavities 105 may exhibit other geometries such as, for example, cylindrical, conical, frustoconical, pyramidal, frustopyramidal or semispherical.

Referring next to drawing FIG. 1B, the top surface 104 of the substrate 102 is coated with a layer of die attach material 112 such as a die attach material which may be applied in a generally liquid form and then soft-baked or cured to a B-stage. The die attach material may include epoxy resins and polyimides, as well as organic and polymer-based resins. Exemplary die attach materials include resins derived from B-stage benzocyclobutene (BCB) and which are available from Dow Chemical Company of Midland, Michigan. The die attach material 112 may be applied to the substrate using a conventional spin or spray coating process wherein the top surface 104 of the substrate 102 is coated and the cavities 105 are filled with the die attach material 112 as will be appreciated by those of ordinary skill in the art. The die attach material 112

material may desirably exhibit, for example, a dielectric constant up to approximately three to ensure adequate electrically insulative properties. It is noted that the soft-bake or B-stage curing of the die attach material helps to prevent movement of the semiconductor dice 114 relative to the substrate 102 during subsequent baking or curing operations.

A plurality of discrete semiconductor dice 114 is provided, each having a plurality of signal connection devices, shown as conductive bumps 116, attached to bond pads 115. The semiconductor dice 114 are placed upside down with the conductive bumps 116 positioned in the cavities 105 and with the active surface 118 of the semiconductor dice 114 in contact with the die attach material 112. It is noted that the size of the cavities 105 may be etched slightly larger in breadth and/or depth than the size of the conductive bumps 116 in order to ensure proper fit of the conductive bumps 116 within the cavities 105. The conductive bumps 116 may be formed, for example, as gold stud bumps applied with a conventional wire bond process. Other signal connection devices, such as copper stud bumps or plated-type stud bumps may also be used. Although drawing FIGS. 1C through 1F show the conductive bumps 116 as generally spherical balls, the conductive bumps 116 may actually be formed in other shapes, including pillars and columns.

In addition, for simplicity, drawing FIGS. 1A through 1F show a single row of conductive bumps 116 positioned extending down the longitudinal axis of each of the semiconductor dice 114, which longitudinal axis is oriented transverse to the plane of the page. However, other conductive bump arrangements such as, for example, an arrangement around the periphery of a semiconductor die 114 or an array of conductive bumps 116 across the active surface 118 of a semiconductor die 114 are also within the scope of the present invention. Furthermore, the semiconductor dice 114 may be of more than one functional variety appropriately arranged so as to create what is referred to as a system on a chip, as will be described in further detail below.

With the semiconductor dice 114 attached to the substrate 102, a molding or encapsulating layer 119 is formed over the top surface 104 of the substrate 102 and the back side 120 of the semiconductor dice 114 as shown in drawing FIG. 1D. The molding layer 119 may be any of a variety of compounds known in the art for the purpose of encapsulating the semiconductor dice 114 and substrate 102 to form a typical chip scale package. The molding layer 119 may include a filled polymer and may desirably

comprise a material having properties sufficient to allow it to withstand temperatures of up to about 300° C without substantial degradation thereof.

After the molding layer 119 is disposed on the top surface 104 of the substrate 102 and properly cured, a portion of the substrate 102 along its bottom surface 106 is removed as is shown in drawing FIG. 1E. It is noted that, for purposes of clarity, the assembly, as shown in drawing FIG. 1E (as well as in subsequent drawing FIG. 1F), is flipped upside down relative to that which is shown in drawing FIGS. 1A through 1D. The portion of material may be removed from the bottom surface 106 of the substrate 102 by techniques such as back-grinding, abrasive planarization techniques such as chemical-mechanical planarization (CMP), etching or an atmospheric downstream plasma (ADP) process offered by Tru-Si Technologies of Sunnyvale, CA, which is known by those of ordinary skill in the art. Material is removed from the bottom surface 106 of the substrate 102 until the conductive bumps 116 are exposed, creating a new bottom surface 106′ of the substrate 102, as shown in FIG. 1E. With the conductive bumps 116 exposed, a system on a chip structure has been created with an array of exposed conductive bumps 116.

To prepare the wafer for a redistribution layer (RDL) process, a dielectric layer 122 is formed covering the new bottom surface 106′ of the wafer and the conductive bumps 116, as shown in drawing FIG. 1F. Finally, a plurality of vias or openings 124 is formed in the dielectric layer 122 over the conductive bumps 116, such as with a conventional etching process. The assembly may then be subjected to an RDL process to redistribute or relocate the signals to an arrangement of signal device or input/output connections.

Before describing the redistribution layer process, another embodiment of the present invention is described as shown in drawing FIGS. 2A through 2D. The process begins, as in the previously described embodiment, with a substrate 202 such as a silicon wafer as shown in drawing FIG. 2A. Again, cavities 205 are formed in the substrate 202, each cavity being defined by a cavity base 208 and cavity walls 210. However, in the presently described embodiment, the cavities 205 are of a size sufficient to receive substantially the entirety of each individual semiconductor die 214. Additionally, the cavities 205 are formed to a depth short of back side 206 sufficient to allow the active surface 220 of the semiconductor dice 214 to be substantially flush with the top surface 204 of the substrate 202. It is noted that, since different types of semiconductor

dice 214 may be used, the cavities 205 may accordingly differ in size and shape from one cavity to another.

As shown in drawing FIG. 2B, a layer of die attach material 218 is applied in the cavities 205. Discrete semiconductor dice 214 are then placed in the cavities 205 with the active surface 220 of the semiconductor dice 214 facing upwards and the back surface 216 of the semiconductor dice 214 being attached to the base 208 of its respective cavity 205 via the die attach material 218. As shown in drawing FIG. 2C, a first dielectric layer 222 is applied over the top surface 204 of the substrate 202 and which may fill in any gaps 221 between the sides of the semiconductor dice 214 and the cavity walls 210. The first dielectric layer 222 may be applied in a conventional process such as spin coating or spray coating. Finally, as shown in drawing FIG. 2D, a plurality of vias or openings 224 is formed in the first dielectric layer 222, such as by an etching process, thereby exposing the plurality of underlying signal connection devices shown as bond pads 215.

The RDL process, which is applicable to both of the exemplary embodiments discussed above, is shown and described with respect to drawing FIGS. 3A through 3F. Illustrated in drawing FIG. 3A is a general substrate 302 with embedded semiconductor dice 304 and signal connection openings 306 representing any embodiment within the scope of the invention. The process begins, as shown in drawing FIG. 3B, by a metallization layer and patterning process to create a first circuit connection layer 308 of metal covering the plurality of signal connection openings 306. In the exemplary embodiments, the signal connection openings 306 expose either the conductive bumps 116 in the embodiment shown and described with respect to drawing FIGS. 1A through 1F or the bond pads 215 in the embodiment shown and described with respect to drawing FIGS. 2A through 2D. This results in an electrical connection to the underlying semiconductor dice 304 and creates first circuit connection layer 308, shown as circuit lines, to redistribute and possibly connect the signals to other metallization layers.

The RDL process may incorporate metallization layer deposition and etching processes well known in the art to form the pattern of openings and first circuit connection layers 308. Further, the metal layer may be formed of a material including, for example, aluminum, copper, or other alloys known and utilized in the art. It is also noted that signal connection devices (e.g., the conductive bumps 116 of drawing FIG. 1C or the bond pads 215 of drawing FIG. 2C) may be treated or have an under-bump metallization-type

material placed thereon prior to connection with the first circuit connection layer 308 to enhance metallic adhesion therebetween.

A predetermined number of additional metal layers may be added in a basic three-step signal connection layering process as shown in drawing FIGS. 3C and 3D. For example, a new additional dielectric layer 310 is formed over the previous metal and dielectric layers, coating the entire wafer. Next, a plurality of vias or openings 312 is created in the dielectric layer 310, such as by etching, exposing the underlying first circuit connection layer 308 at a desired plurality of circuit connection areas. Finally, a new metallization and patterning process creates a new circuit connection layer 314, shown in drawing FIG. 3D, making desired electrical connections to the underlying first circuit connection layer 308 and redistributing signals to new locations, possibly for connection to higher metal layers. For simplicity, the drawing FIGS. 3A-3D show the formation of only one additional metal layer, However, this process may be repeated a predetermined number of times (for example, three times to create three intermediate signal routing layers), thereby forming a laminate-type structure. Multiple layers may be desired to create power planes, ground planes, and difficult signal interconnections not easily accomplished on two signal layers.

As shown in drawing FIGS. 3E and 3F, a final dielectric layer 316 is applied over the previous dielectric layer 310 and circuit connection layer 314. Again, a conventional etching process is used to create a plurality of vias or openings 318 in the final dielectric layer 316 exposing the underlying circuit connection layer 314. Finally, new signal device connections 320, such as solder balls or other conductive bumps, are formed in the plurality of openings 318 contacting the underlying circuit connection layer 314.

With the new signal device connections 320 formed, if desired, testing could be accomplished through connection with the new signal device connections of each of the individual multichip packages.

Referring now to drawing FIG. 4, an assembly 400 containing a plurality of semiconductor dice 404A-404D (collectively referred to as semiconductor dice 404) is shown according to an embodiment of the present invention. The substrate 402 is sawed into individual segments 406 along sawing lines 408 to form individual systems on chip modules with each segment 406 containing a plurality of semiconductor dice 404A-404D possibly of multiple functional varieties. For example, semiconductor die 404A might be a processor, semiconductor die 404B might be a memory controller and semiconductor

dice 404C and 404D might be memory chips. Although FIG. 4 shows a segment 406 containing four semiconductor dice 404A-404D, it should be understood that the number of semiconductor dice within a segment 406 may be some other number depending on the design and intended use of the resulting semiconductor package.

Referring now to drawing FIG. 5, a memory device 500, also referred to as a memory module, is shown which incorporates at least one packaged multichip semiconductor device 510 according to the present invention. The memory device 500 includes a carrier substrate 520, such as a printed circuit board, to which one or more packaged multichip semiconductor devices 510 may be electrically and operably coupled therewith. A plurality of electrical connectors 530 is formed on the carrier substrate 520 to provide input and output connections with an external device, such as, for example, the motherboard of a computer, to the one or more packaged multichip semiconductor devices 510.

Referring now to drawing FIG. 6, a computing system 600 is shown which includes a carrier substrate 602 such as, for example, a motherboard. The carrier substrate 602 may be operably coupled to at least one processor 604, such as, for example, a central processing unit (CPU), and at least one memory device 606. The memory device 606 may include one or more packaged multichip semiconductor devices 608 such as described above. The carrier substrate 602 is operably coupled with at least one input device 610 such as, for example, a keyboard, a mouse, a sensor or another computing device. The carrier substrate 602 is also operably coupled with at least one output device 612 such as, for example, a printer, a monitor, an actuator or another computing device. Alternatively, the packaged multichip semiconductor device 608 may be coupled directly with the carrier substrate 602.

Specific embodiments have been shown by way of example in the drawings and have been described in detail herein; however, the invention may be susceptible to various modifications and alternative forms. It should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention includes all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.

CLAIMS

What is claimed is:

1. A method of manufacturing a multichip package comprising:

providing a substrate having a top surface and a bottom surface;

forming a plurality of cavities in the top surface of the substrate;

providing a plurality of semiconductor dice, each semiconductor die having a back surface and a plurality of signal connection devices on an active surface thereof;

applying a layer of die attach material to the top surface of the substrate and within the plurality of cavities;

placing the plurality of semiconductor dice on the top surface of the substrate such that the plurality of signal connection devices is at least partially disposed within the plurality of cavities;

applying a molding layer over the top surface of the substrate and the plurality of semiconductor dice; and

removing a volume of material along the bottom surface of the substrate to a depth sufficient to expose the plurality of signal connection devices of the plurality of semiconductor dice.

2. The method of claim 1, further comprising:

forming a first dielectric layer upon the bottom surface of the substrate and the plurality of signal connection devices;

forming a plurality of openings in the first dielectric layer exposing the plurality of signal connection devices therethrough;

forming a first circuit connection layer on the first dielectric layer; and

electrically coupling the first circuit connection layer with the plurality of signal connection devices through the plurality of openings.

3. The method of claim 2, further comprising:

forming at least one additional dielectric layer over the first dielectric layer and the first circuit connection layer;

forming a plurality of openings in the at least one additional dielectric layer exposing a plurality of connection areas on the first circuit connection layer; and

forming a plurality of conductive bumps in the plurality of openings of the at least one additional dielectric layer and electrically coupling the plurality of conductive bumps with the plurality of connection areas on the first circuit connection layer.

4. The method of claim 3, further comprising sawing the substrate into a plurality of sections, each section of the plurality of sections containing at least two of the plurality of semiconductor dice.

5. The method of claim 4, further comprising arranging the plurality of semiconductor dice such that each section of the plurality of sections includes at least a first semiconductor die of a first functional variety and a second semiconductor die of a second functional variety.

6. The method of claim 2, wherein providing the substrate further includes providing a silicon wafer.

7. The method of claim 6, further comprising forming the plurality of signal connection devices to comprise at least one of the group consisting of gold stud bumps, copper stud bumps, and plated stud bumps.

8. The method of claim 7, wherein applying a layer of die attach material includes applying a layer of epoxy material.

9. The method of claim 7, wherein applying a layer of die attach material includes applying a layer of benzocyclobutene.

10. The method of claim 7, further comprising forming each of the plurality of cavities to exhibit a depth which is at least substantially equal to or greater than a height of each of the plurality of signal connection devices.

11. The method of claim 10, wherein applying a layer of die attach material includes applying a layer of dielectric material exhibiting a dielectric constant of up to about three.

12. The method of Claim 11, wherein applying a molding layer includes applying a molding material which is capable of withstanding a temperature of up to about 300° C without substantial degradation thereof.

13. The method of claim 1, further comprising:

forming a laminate structure over the bottom surface of the substrate including:

forming a plurality of dielectric layers and forming a plurality of circuit connection layers such that the plurality of dielectric layers and plurality of circuit connection layers are disposed in an alternately layered manner, wherein each circuit connection layer of the plurality is electrically coupled to an adjacent circuit connection layer, and wherein a circuit connection layer most adjacent to the bottom surface of the substrate is electrically coupled to the plurality of signal connection devices; and

forming a plurality of conductive bumps on an outermost surface of the laminate structure and electrically coupling the plurality of conductive bumps to a circuit connection layer which is most adjacent the outermost surface of the laminate structure.