Method of fabrication of a back-contacted photovoltaic cell, and back-contacted photovoltaic cell made by such a method.

The present invention relates to a method of fabrication of a back contacted photovoltaic cell. Moreover, the present invention relates to a back contacted photovoltaic cell.

A back-contacted photovoltaic cell or solar cell, based on either a monocrystalline or polycrystalline silicon wafer, comprises a metallization scheme in which contacting electrodes of positive and negative polarity are each arranged on a back side of the solar cell. Such a metallization scheme applies either metallization wrap through (MWT) or emitter wrap through (EWT) to bring the contacting electrodes to the back side so as to have a maximal area available for photovoltaic conversion on a front side of the solar cell that in use faces a radiation source (e.g., the sun). The top layer of the solar cell connects to a front side contacting electrode on the backside of the cell by means of one or more metal plugs in holes (also known as "vias") that extend through the wafer.

The back-contacted solar cell of the prior art suffers from a relatively poor efficiency for a number of reasons.

It is known that in conventional MWT or EWT technology the conductance through the vias can be relatively small. The metallization of the vias is typically obtained by means of a screen printing process which presses metal paste into the vias. To obtain vias completely filled with metal by this method is difficult. As a result of the low conductance the efficiency of the solar cell is therefore reduced.

From International Application WO5076960 it is known to improve the conductance within a via by doping the via walls using a diffusion process preceding the screen printing process. The diffusion process must be arranged to obtain a via wall with higher dopant concentration than the optimum (low) dopant concentration of the front side layer of the solar cell. Such diffusion process for the via is complex since it requires additional production steps, which may also adversely interfere with the formation of the front side layer. In particular, a relatively high dopant concentration at

the front side layer of the wafer due to the doping of the via walls may enhance the recombination of minority charge carriers in the front side layer.

Also, it is known to use electroplating for metallisation of the vias in the wafer. However, this technology is relatively costly compared to screen printing.

An embodiment of the present invention seeks to remove or at least reduce the above disadvantages.

According to an aspect of the present invention, there is provided a method of manufacturing a photovoltaic cell, comprising:

- providing a semiconductor substrate of a first conductivity type;
- creating at least one via, being a hole, that extends between a front side and a back side of the semiconductor substrate;
- applying on the backside a front side contacting metal paste over the at least one via, the front side contacting metal paste comprising a first contacting metal;
- annealing the semiconductor substrate so as to melt the first contacting metal, and during annealing, creating at least on the walls of the at least one via an alloy of the first contacting metal and the semiconductor substrate material.

Advantageously, the method provides an enhancement for filling of the at least one via, due to a flow of molten first contacting metal caused by wetting and/or capillary action, which is assisted by the formation of an alloy at the walls of the at least one via.

In an embodiment, the method provides that the first contacting metal of the front side contacting metal paste is a dopant element for the semiconductor substrate, the dopant element causing a second conductivity type, the second conductivity type being opposite to the first conductivity type.

Advantageously, in this embodiment the method allows that the walls of the at least one via can have a conductivity type different from the conductivity type of the substrate material.

In another embodiment, the method provides that the front side contacting metal paste comprises at least one first dopant element causing a second conductivity type, the second conductivity type being opposite to the first conductivity type. Advantageously, in this embodiment the method allows that the walls of the at least one via can have a conductivity type different from the conductivity type of the substrate material.

According to another aspect of the present invention, there is provided a photovoltaic cell comprising:

- a silicon semiconductor substrate of a first conductivity type;
- at least one via, being a hole, that extends from a front side to a back side of the semiconductor substrate;
- on the backside a front side contacting metal pattern over the at least one via, the front side contacting metal pattern comprising a first contacting metal;
the at least one via comprising at least on the walls a layer of an alloy of the first contacting metal and the silicon semiconductor substrate material.

Advantageous embodiments are further defined by the dependent claims.

Below, the invention will be explained with reference to some drawings, which are intended for illustration purposes only and not to limit the scope of protection as defined in the accompanying claims.

Figure 1 shows schematically a cross-section of a back-contacted photovoltaic cell in accordance with an embodiment of the present invention during an initial stage;

Figure 2 shows schematically a cross-section of the back-contacted photovoltaic cell during a next stage;

Figure 3 shows schematically a cross-section of the back-contacted photovoltaic cell during a subsequent stage;

Figure 4 shows schematically a cross-section of the back-contacted photovoltaic cell during yet a next stage;

Figure 5 shows schematically a cross-section of the back-contacted photovoltaic cell during a further stage;

Figure 6 shows schematically a cross-section of the back-contacted photovoltaic cell during yet another subsequent stage;

Figure 7 shows schematically a cross-section of the back-contacted photovoltaic cell in a further embodiment, and

Figure 8 shows a block diagram of a process in accordance with the present invention.

Figure 1 shows schematically a cross-section of a back-contacted photovoltaic cell 1 in accordance with an embodiment of the present invention during an initial stage.

During an initial stage of the manufacturing process, a semiconductor substrate 101 of a first conductivity type is provided.

The substrate can be either a monocrystalline wafer or a polycrystalline wafer of silicon.

The first conductivity type can be either p-type (acceptor type) or n-type (donor type). In a preferred embodiment, the first conductivity type is n-type.

In the substrate 101, one or more vias 102 are created that run from a front side 101a to a back side 101b of the substrate. Vias can be created by laser hole drilling technology.

After creating the vias 102, a top layer 103 is formed on the front side of the substrate 101 and on the walls 102a, 102b of the vias 102, and optional on part of the back side of the substrate. The top layer 103 has a second conductivity type that is opposite to the first conductivity type of the substrate 101.

In a preferred embodiment, the substrate has n-type conductivity and the top layer 103 has p-type conductivity. The p-type top layer 103 can be formed by diffusion of boron (B) as a first dopant element of p-type.

Alternatively, the first dopant element may comprise Al, Ga, or In.

The first dopant element may be formed from a vapor source or a coating source. The coating source may be a paste or a liquid that contains the dopant. This paste or liquid can be screen printed, spin-coated or sprayed on the surface of the substrate and then can be diffused in at high temperature.

Figure 2 shows schematically a cross-section of the back-contacted photovoltaic cell 1 during a next stage.

Next, base contact regions 104 for contacting the substrate 101 are created on the back side 101b.

A mask (not shown) is used to define the regions where the base contacts 104 are to be formed.

In a preferred embodiment, in which the substrate has n-type conductivity, the base contact regions 104 are created by a diffusion of a second dopant element of n-type. The second dopant element may be phosphorous (P). The second dopant element may be formed from a vapor source or a coating source.

After defining or creating the base contact regions 104, the mask is removed.

Alternatively, the second dopant element may be applied locally on the base contact regions 104 by means of a dopant containing paste comprising n-type dopant.

Figure 3 shows schematically a cross-section of the back-contacted photovoltaic cell 1 during a subsequent stage.

Subsequently, a first dielectric layer 105 is formed on the front side of the substrate to cover the top layer 103. Typically, the first dielectric layer 105 is a silicon nitride layer which can be created by a plasma enhanced chemical vapor deposition process (PECVD). Alternatively, the dielectric layer may be formed by a sputter-deposition process or a low pressure CVD (LPCVD) process or any further process as known in the art.

Next, a second dielectric layer 106 is formed on the back side of the substrate. Typically, the second dielectric layer 106 which may have a different composition than the first dielectric layer 105 is a silicon nitride layer which can be also created by a plasma enhanced chemical vapor deposition process (PECVD).

Figure 4 shows schematically a cross-section of the back-contacted photovoltaic cell 1 during yet a next stage.

During this stage, a back side metallization pattern 107 is created on the second dielectric layer at the back side of the substrate. The back side metallization pattern 107 is arranged substantially over the base contact regions 104.

Typically, the back side metallization pattern 107 is created by screen printing of a back side contacting metal paste. Alternatively, the back side metallization pattern 107 may also be created by an other technology, such as stencil printing, inkjet printing, dispensing, decal transfer, electroplating, electroless plating (but not limited thereto). The back side metal paste of the back side metallization pattern 107 may comprise silver (Ag) as second contacting metal.

Figure 5 shows schematically a cross-section of the back-contacted photovoltaic cell 1 during a subsequent stage.

During this stage, a front side contacting metallization pattern 108 is created at the back side of the substrate. The front side contacting metallization pattern is formed over the back side via openings in such a way that the vias 102 are at least partially filled with first contacting metal.

The front side contacting metallization pattern may be created by a second screen printing process of a contacting metal paste, or by other techniques such as those mentioned above with reference to the fabrication of the back side metallisation pattern.

In a preferred embodiment, the contacting metal paste of the front side contacting metallization pattern 108 comprises aluminium (Al) as first contacting metal.

In the case of MWT (metallisation wrap through) an additional metallisation pattern (not shown here) is also applied on the front side of the substrate.

Figure 6 shows schematically a cross-section of the back-contacted photovoltaic cell during yet another subsequent stage.

During this stage, the back-contacted photovoltaic cell is heated at an elevated annealing temperature. The annealing temperature is selected so as to allow the formation of a conductive contact between the second contacting metal of the back side contacting metallization pattern 107 and the base contact regions 104, and to cause melting of at least the first contacting metal in the contacting metal paste of the front side contacting metallization pattern 108.

The melting of the front side contacting metal paste advantageously allows filling of the vias, due to a flow of molten contacting paste material caused by wetting and/or capillary action.

Moreover, the annealing temperature may be chosen so as to have a reaction of the first contacting metal of the front side contacting metallization pattern 108 with the walls 102a, 102b of the via to form an intermetallic compound 109 (e.g., a eutectic alloy).

The via may comprise a plug of a single metal body, in case no reaction occurs with the walls. If a reaction occurs with the walls, then the via may comprise a plug that partially or fully consists of the intermetallic compound 109.

In an embodiment in which the first contacting metal paste comprises aluminium and the semiconductor substrate comprises silicon, the intermetallic compound 109 may comprise the Al-Si eutectoid. Due to the formation of a eutectic alloy at relative low liquidus temperature (about 600 °C) in the Al-Si composition system (or Al-Si phase diagram), an excellent filling of vias can be achieved, in particular due to the relative low viscosity of the eutectic liquid.

Also, it is noted that aluminium can act as a p-type dopant of silicon. As a result, the junction isolation (the isolation of the via metal from the n-type substrate 101) and the conductivity within the via wall is enhanced, which results in further improvement of the efficiency of the back-contacted photovoltaic cell 1.

In an embodiment in which the back side contacting metal paste comprises silver and the front side contacting metal paste comprises aluminium, an annealing

temperature can be chosen between the melting temperature of aluminium and that of silver. In such a case, alloying of aluminium with silicon can occur, while silver paste only opens the silicon nitride layer 106 to contact the base contacts 104.

It is noted that in an alternative embodiment, the back side contacting (by annealing) of the back side contacting metal paste 107 to the base contacts 104 may be done preceding to the screen printing of the front side contacting metal paste 108 and the subsequent anneal to fill the vias with the contacting metal.

Since the annealing temperature to melt aluminium (or Al-Si alloy) is lower than the melting temperature of silver, the back side silver contacts 107 are stable during the filling of the vias.

It is noted that in a further embodiment, the metallic plug in the via may comprise a void in its centre. In that case, the plug may exhibit a (quasi-) tubular shape.

Due to annealing, the front side contacting metal paste solidifies into a front side contacting metal composition comprising the first contacting metal, the back side contacting metal paste solidifies into a back side contacting metal composition comprising the second contacting metal.

Figure 7 shows schematically a cross-section of the back-contacted photovoltaic cell in a further embodiment.

In Figure 7 entities with the same reference number as shown in the preceding figures refer to the corresponding entities.

In this embodiment, the front side contacting metal paste 108 comprises a first contacting metal and a dopant element. During an annealing procedure, both a diffusion reaction of the dopant element diffusing into the substrate material and an alloying reaction of the first contacting metal with the semiconductor substrate material can occur.

Depending on the reaction kinetics of each of these reactions, the plug in the via may comprise a doped layer 111, an intermetallic compound layer 112 and a metal body 110. The ratio of the widths will depend on the reaction kinetics at the selected annealing temperature, as will be known to the skilled person.

In an embodiment, the substrate 101 comprises n-type silicon and the front side contacting metal paste comprises aluminium and boron.

Figure 8 shows a block diagram of a manufacturing process 800 in accordance with an embodiment of the present invention.

The manufacturing process 800 of a back-contacted photovoltaic cell 1 begins at action 801, in which a n-type silicon substrate is provided. The wafer is either monocrystalline or polycrystalline.

In next action 802, holes (vias) for p-type contacts are drilled in the wafer by laser drilling.

Then, in action 803, on the front side of the wafer a top layer with p-type conductivity is formed by boron (p^+) diffusion. This diffusion process may be carried out at elevated temperature using gaseous boron pre-cursor. At the same time, the walls of the vias are covered with a layer of p-type conductivity.

In action 804, contact regions are created on the back side 101b of the wafer by a diffusion of n-type dopant. The n-type dopant may be phosphorous (P).

In subsequent action 805, a first dielectric layer 105 is formed as passivation and anti-reflection layer to cover the top layer 103. This first dielectric layer 105 may be a silicon nitride layer which can be created by a plasma enhanced chemical vapor deposition process (PECVD).

In next action 806, a second dielectric layer 106 is formed as passivation and internal-reflection layer on the back side of the wafer. The second silicon nitride layer can be created by a plasma enhanced chemical vapor deposition process (PECVD).

In action 807, a back side (base) contacting metallization pattern 107 for contacting the back side base contacts is created on the back side of the wafer by screen printing of a back side contacting metal paste comprising silver (Ag).

Then, in action 808, a front side (emitter) contacting metallization pattern 108 is created at the back side of the wafer by screen printing of a contacting metal paste comprising aluminium as first contacting metal. The front side contacting metallization pattern is formed over the back side via openings in such a way that the vias 102 are at least partially filled with front side contacting metal paste.

Next in action 809, the wafer is annealed at an elevated annealing temperature. During annealing a conductive contact between the back side silver metallization pattern 107 and the base contact regions 104 is formed. At the same time, the contacting metal paste melts and fills the vias, due to a flow of the molten contacting

metal paste material caused by wetting and/or capillary action. The aluminium of the front side contacting metal paste reacts with the silicon of the wafer and forms an intermetallic compound that covers the walls of the via. Since aluminium is a p-type dopant for silicon, the junction isolation is enhanced and the efficiency of the photovoltaic cell is improved.

In a following action 810 the wafer is cooled down and processed further to create a photovoltaic cell.

It is noted that in the above description, several intermediate process steps may be present, in particular wet- or dry chemical steps, for example for etching and cleaning. For reason of clarity these intermediate steps which are apparent to the skilled person are not discussed here.

It will be apparent to the person skilled in the art that other embodiments of the invention can be conceived and reduced to practice without departing form the true spirit of the invention, the scope of the invention being limited only by the appended claims as finally granted. The description is not intended to limit the invention.

CLAIMS

1. Method of manufacturing a photovoltaic cell, comprising:
- providing a semiconductor substrate of a first conductivity type;
- creating at least one via, being a hole, that extends between a front side and a back side of the semiconductor substrate;
- applying on the backside a front side contacting metal paste over the at least one via, the front side contacting metal paste comprising a first contacting metal;
- annealing the semiconductor substrate so as to melt the first contacting metal, and
during annealing, creating at least on the walls of the at least one via an alloy of the first contacting metal and the semiconductor substrate material.

2. Method according to claim 1, wherein
- after the creation of the at least one via, a layer of a second conductivity type is formed on at least the front side of the semiconductor substrate and on walls of the at least one via;
the second conductivity type being opposite to the first conductivity type.

3. Method according to any one of preceding claims 1 – 2, wherein the first contacting metal of the front side contacting metal paste is a dopant element for the semiconductor substrate, the dopant element causing a second conductivity type, the second conductivity type being opposite to the first conductivity type.

4. Method according to any one of preceding claims 1 – 3 , wherein the front side contacting metal paste comprises at least one first dopant element causing a second conductivity type, the second conductivity type being opposite to the first conductivity type.

5. Method according to claim 2, wherein, in addition to the formation of the layer of second conductivity type, the method comprises:
- forming base contact regions at the back side of the semiconductor substrate, the base contact regions being of the first conductivity type.

6. Method according to claim 2, wherein after the formation of the layer of second conductivity type, the method comprises:
- forming a first dielectric layer to cover the layer of the second conductivity type.

7. Method according to claim 5, wherein after the formation of the base contact regions at the back side of the semiconductor substrate, the method comprises:
- forming a second dielectric layer to cover the back side of the semiconductor substrate.

8. Method according to claim 7, wherein after the formation of the second dielectric layer, the method comprises:
- applying back side contacting metal paste on the base contact regions; the back side contacting metal paste comprising a second contacting metal.

9. Method according to claim 1, wherein the annealing of the semiconductor substrate being done at a temperature above at least a melting temperature of the first contacting metal.

10. Method according to claim 1, wherein the annealing of the semiconductor substrate being done at a temperature above at least a eutectic temperature of a composition system of the first contacting metal and the semiconductor substrate material.

11. Method according to claim 9 or 10, wherein the first contacting metal has a melting temperature, or a eutectic temperature in association with the substrate material, lower than a melting temperature of the second contacting metal.

12. Method according to claim 1, wherein the first conductivity type is n-type.

13. Method according to claim 9 or 10, wherein
the front side contacting metal paste comprises aluminium as first contacting metal,
the back side contacting metal paste comprises silver as second contacting metal, and
the semiconductor substrate comprises silicon.

14. Method according to claim 4, wherein the at least one first dopant element is selected from at least one of a group of boron, aluminium, gallium and indium.

15. Method according to claim 5, wherein forming base contact regions at the back side of the semiconductor substrate is done by diffusion of a second dopant element of the first conductivity type; the second dopant element being selected from at least one of a group of phosphorous, arsenic and antimony.

16. Photovoltaic cell comprising:
- a silicon semiconductor substrate of a first conductivity type;
- at least one via, being a hole, that extends from a front side to a back side of the semiconductor substrate;
- on the backside a front side contacting metal pattern over the at least one via, the front side contacting metal pattern comprising a first contacting metal;
the at least one via comprising at least on the walls a layer of an alloy of the first contacting metal and the silicon semiconductor substrate material.

17. - Photovoltaic cell according to claim 16, wherein the photovoltaic cell comprises a layer of a second conductivity in between the layer of the alloy and the silicon semiconductor substrate material in the at least one via, and on the front side of the silicon semiconductor substrate; the second conductivity type being opposite to the first conductivity type.

18. Photovoltaic cell according to claim 16, wherein the first contacting metal of the front side contacting metal pattern is a dopant element for the silicon semiconductor of the first conductivity type, the dopant element causing a second conductivity type, the second conductivity type being opposite to the first conductivity type.

19. Photovoltaic cell according to any one of claims 16 or 18, wherein the front side contacting metal pattern comprises at least one dopant element causing the second conductivity type, the second conductivity type being opposite to the first conductivity type.

20. Photovoltaic cell according to claim 19, wherein the first contacting metal has a melting temperature, or a eutectic temperature in association with the substrate material, lower than a melting temperature of the second contacting metal.

21. Photovoltaic cell according to any one of claims 16 – 20, wherein the front side contacting metal pattern comprises aluminum as first contacting metal,
the back side contacting metal pattern comprises silver as second contacting metal, and the semiconductor substrate comprises silicon.

22. Photovoltaic cell according to claim 16 or 21, wherein the at least one first dopant element is selected from at least one of a group of boron, aluminum, gallium and indium.

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