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BACKGROUND OF THE INVENTION

1. Field of the Invention.

The invention relates to the field of clocking for CMOS logic circuits.

2. Prior Art.

5 Most complex VLSI circuits are implemented using synchronous logic, that is, logic that is sequenced by central clocking signals. Virtually all microprocessors, for instance, use such logic. Asynchronous logic is used in only special applications, typically for simple functions. The reading and writing of data from a memory
10 is one such function. The present invention deals with synchronous logic, particularly for complementary metal-oxide-semiconductor (CMOS) circuits.

MOS circuits have inherent capacitance which permits temporary storage of logic states enabling the use of low power
15 dynamic circuits. Typically, an external clocking signal is applied to the integrated circuit, and several internal clock phases are generated to shift signals throughout the chip. A typical arrangement is discussed in conjunction with Figure 1.

One problem associated with multiple clock phases is that
20 these phases must be distributed throughout the chip. Moreover, the phases must be nonoverlapping, otherwise one state may be shifted into a device before the information stored in that device is read. Typically, "dead time" is provided between the phases to assure nonoverlapping operation. In VLSI circuits the propagation time of

Each phase to all corners of the chip must be considered since one phase may have a different propagation time than another. These considerations add to the design complexity. In some instances, the operation of the circuit is slowed since the dead time must be increased when the propagation time of the various phases are taken into account to assure some dead time throughout the chip.

The present invention provides a logic arrangement using a single phase clocking signal. Single phase clocking signals have been used for TTL, ECL and to some extent, in MOS circuits.

A discussion of single phase clocking arrangement for an NMOS circuit can be found in "A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual-Port Memory and Error Checking and Correction", IEEE Journal of Solid-State Circuits, Vol. SC-18, No. 2, April 1983 (see discussion beginning on page 168). The present invention extends these teachings to provide a straightforward approach for CMOS circuits.



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SUMMARY OF THE INVENTION

A single phase clocked logic arrangement for complementary-metal-oxide semiconductor (CMOS) integrated circuits is described. The arrangement includes a first and second logic circuits each of which has input transistors. The first logic
5 circuit is coupled to receive an input signal while the output signal of the first logic circuit is coupled as an input to the second logic signal. Both the first and second logic circuits are coupled to receive the same phase of a clocking signal. The size of the input transistors of the first and second logic circuits are different so
10 as to cause the first logic circuit to accept the input signal during a first period of the clocking signal, and the second logic circuit to accept the output signal from the first logic circuit during a second period of time of the clocking signal. The first and second periods of time are nonoverlapping. In the currently preferred
15 embodiment, both the first and second logic circuits are D-type level-triggered flip-flops, and the input transistors include both n-type and p-type transistors. The combination of the first and second logic circuits comprise a D-type edge-triggered flip-flop. By way of example, one logic circuit is activated when the clocking
20 signal is below one-third of its maximum potential and the other logic circuit is activated when the clocking signal is above two-thirds of its maximum potential. This leaves a safety zone or time when neither of the circuits will be in transition.

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DEFINITION OF THE DRAWINGS

Figure 1 is a circuit diagram of a prior art CMOS logic circuit.

Figure 2 is a circuit diagram of two D-type level-triggered flip-flops forming an edge-triggered D-type flip-flops which are used in describing the present invention.

Figure 3 is an electrical schematic of the currently referred embodiment of the present invention.

Figure 4 illustrates waveforms used to describe the operation of a circuit built in accordance with the present invention.



DETAILED DESCRIPTION OF THE PRESENT INVENTION

A complementary-metal-oxide semiconductor (CMOS) integrated circuit logic arrangement using a single phase clocking signal is described. A specific embodiment of the present invention is described which includes transistor sizes. It will be obvious, however, to one skilled in the art that the present invention may be practiced without these details. Specific details used, for instance, to fabricate the present invention are not described in order not to unnecessarily obscure the present invention and since they are well-known in the art.

Any one of numerous commercially used integrated circuit CMOS processes may be used to fabricate the present invention including processes using p-wells, n-wells and double wells.

In Figure 1, a prior art CMOS logic arrangement is illustrated. The circuit is a dynamic implementation of series coupled D-type bistable circuits (flip-flops). An input signal on line 10 is clocked through transistors 16 and 17 and stored on the parasitic capacitance of the input node of the inverter 12. The output of this inverter is clocked through the transistors 18 and 19 and stored on the parasitic capacitance of the input node of the inverter 14. An output signal from the logic arrangement is present on line 15.

In Figure 1, the timing signals $\phi 1$ and $\phi 2$ and their complements are out of phase with one another and typically are generated from an externally generated clocking signal applied to the chip. By way of example, during a first period of time determined by

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1, the signal on line 10 is transferred through the transistors 16 and 17 to the input node of inverter 12. During this first period of time, the data on line 15 may also be sensed. Then, during a second period of time, as determined by $\phi 2$, the data at the output of the inverter 12 is coupled through the transistors 18 and 19 as these transistors conduct, to the input node of inverter 14. During the second period of time, new data may be applied to line 10. It is apparent from the circuit of Figure 1 that if transistors 16 and 17, and 18 and 19 conduct simultaneously, the data on line 10 is coupled through the inverters 12 and 14 before the data stored on the input node of inverter 14 is read. For this reason, the clock phases $\phi 1$ and $\phi 2$ are typically nonoverlapping, and often a dead time exists between $\phi 1$ and $\phi 2$ to prevent overlapping operation.

Often, the $\phi 1$ and $\phi 2$ signals and their complements are distributed throughout the integrated circuit and thus require an extensive bus network. In some cases, the complementary signals to $\phi 1$ and $\phi 2$ are generated locally through inverters, or other arrangements are used in CMOS circuits where only two clock phases (no complements) are needed.

20 With the present invention, the dynamic storage of Figure 1 is replaced with static storage as is illustrated in Figure 2. A master and slave bistable circuits may be used. In Figure 2, a first bistable circuit (master) includes the cross-coupled gate-pairs. One gate-pair includes the AND gate 21 and NOR gate 22 and the other gate-pair, the AND gate 23 and NOR gate 24. An input signal on line 20 provides an input to gate 21 and an input to the gate 23 through the inverter 25. The single phase clocking signal on line 26

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provides the other inputs to gates 21 and 23.

The second bistable circuit (slave) of Figure 2 also includes cross-coupled gate-pairs. One gate-pair comprises the OR gate 27 and NAND gate 28 and the other gate-pair, the OR gate 29 and NAND gate 30. The outputs of the gates 22 and 24 provide inputs to gates 27 and 29, respectively. The clocking signal on line 26 provides the other input to the gates 27 and 29. The Q and Q/ outputs from the gates 28 and 30 are present on lines 32 and 33, respectively.

With the present invention, as will be described in more detail in conjunction with Figure 3, nonoverlapping operation between the master and slave bistable circuits is achieved through the proper sizing of input transistors to the master and slave circuits.

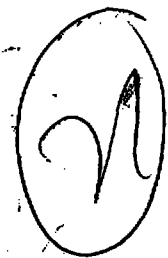
The currently preferred embodiment of the logic arrangement of Figure 2 is illustrated in Figure 3. The input line 20 and output lines 32 and 33 are again illustrated. The single phase clocking signal is again coupled to line 26. The gate-pair 21 and 22 includes transistors 36-41. The p-type transistor 36 is coupled to the V_{CC} (positive potential) and the sources of the p-channel transistors 37 and 38. Transistor 37 is coupled in series with the n-channel transistors 39 and 40; transistor 38 is coupled in series with n-channel transistor 41. The input signal is coupled to the gates of transistors 37 and 39; the clocking signal is coupled to the gates of transistors 38 and 40. The cross-coupling from the gate-pair 23 and 24 is provided through the gates of transistors 36 and 41. The output signal from the gate-pair 21 and 22 is provided from the junctions between transistors 37 and 39 and transistors 38 and 41.

The gate-pair 23 and 24 is connected in a similar manner as the gate-pair 21 and 22 with transistors 44-49. The input signal is coupled through the inverter 25 to the gates of transistors 45 and 47. The clocking signal is coupled to the gates of transistors 46 and 48. The cross-coupling from the gate-pair 21 and 22 is provided through the gates of transistors 44 and 49.

The gate-pair 27 and 28 of Figure 2 is realized with transistors 52-57 in Figure 3. The p-channel transistors 52 and 53 are coupled in series between the VCC potential and the drain of the n-channel transistor 55. The p-channel transistor 54 is coupled in parallel with transistors 52 and 53. Transistor 55 is coupled to the drains of n-channel transistors 56 and 57; the source regions of transistors 56 and 57 are coupled to ground. The output signal from the gate-pair 21 and 22 is coupled to the gates of transistors 53 and 56. The clocking signal is provided to the gates of transistors 52 and 57. The cross-coupling with the gate-pair 29 and 30 is obtained through the gates of transistors 54 and 55.

The gate-pair 29 and 30 of Figure 3 is implemented in a similar manner to the gate-pair 27 and 28 and includes transistors 60-65. The output from the gate-pair 23 and 24 is coupled to the gates of transistors 61 and 64. The clocking signal is coupled to the gates of transistors 60 and 65 and the cross-coupling from the gate-pair 27 and 28 is provided through the gates of transistors 62 and 63.

The input transistors 37 and 38 of the gate-pair 21 and 22 are encircled with a continuous line 67. The input transistors 39 and 40 of this gate-pair are circled with a broken line 68.



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Similarly, for the gate-pair 23 and 24 input transistors 45 and 46 are circled with continuous line 69 and input transistors 47 and 48 are circled with broken line 70.

In the gate-pair 27 and 28, the input transistors 52 and 53 are circled with a broken line 71 and the input transistors 56 and 57 are circled with a continuous line 72. Similarly, for the gate-pair 29 and 30, transistors 60 and 61 are circled with broken line 73 and transistors 64 and 65 are circled with continuous line 74.

In the following table, the relative drawn sizes of the transistors of Figure 3 are shown (only "Z" values are given, this is the channel width; the channel length (distance between source and drain) is 2 microns in all cases).

<u>MASTER</u>		<u>SLAVE</u>	
<u>Transistor</u>	<u>Z</u>	<u>Transistor</u>	<u>Z</u>
36,44	18	52,60	16
37,45	18	53,61	16
38,46	18	54,62	8
39,47	6	55,63	14
40,48	6	56,64	14
41,49	6	57,65	14

The input transistor sizes are selected to provide the operation which will be described in detail in conjunction with Figure 4. More specifically, the transistor size Z/L (width/length) are the transistor parameters varied to obtain the desired result. With the present invention, the transistors shown within the solid lines 67, 69, 72 and 74 are made larger when compared to the transistors shown in the dotted lines 71, 73, 68 and 70, respectively.

Any one of numerous calculations may be used to determine the

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sizes of the transistors. One technique which is currently preferred is to estimate sizes and then simulate the circuit with a computer model. Relatively small adjustments in the transistor sizes can then be readily made to obtain a combination of sizes which provide the best results. The initial sizes, however, are selected in accordance with the present invention for the input transistor.

In the shown embodiment the master and slave flip-flops are each level-triggered devices forming together a D-type edge-triggered device. More particularly a positive-level-triggered master flip-flop and a negative-level-triggered slave flip-flops form a negative-edge-triggered flip-flop. The master circuit can be a negative-level-triggered device and the slave a positive level-triggered device forming a positive-edge-triggered flip-flop.

Referring now to Figure 4, the single phase clocking signal which is applied to line 26 is shown as waveform 26a. A typical input such as would be applied to line 20 is shown as waveform 20a. The desired output (Q output) on line 32 is shown as waveform 32a.

The input transistors for the gate-pairs of Figure 3 are selected such that the master circuit accepts data from the input line 20 when the clocking signal is in a first period. In the presently preferred embodiment, this first period occurs when the potential of the clocking signal exceeds $2/3 V_{CC}$. The input transistors of the slave circuit are selected so that the slave circuit accepts the output from the master circuit when the clocking signal is in a second period. This second period, in the preferred embodiment, is when the potential of the clocking signal is below $1/3 V_{CC}$. These periods are shown on waveform 26a as "master samples"

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and "slave samples", respectively. The period of time between the sampling of the master and slave circuits is shown as the safety zone.

At time 100, the master circuit samples the waveform 20a which is in a low state. At time 101, the slave circuit samples this low state and itself provides a low output on line 32. Assume that the potential on line 20 rises. At time 102 this high potential is sampled by the master circuit and as indicated at time 103 the slave circuit samples this high potential. If the input signal drops in potential, as indicated at time 104, the master samples this new low potential and this low potential is sampled by the slave circuit and is provided on line 32 at time 105.

With the above described operation, the safety zone assures nonoverlapping operation.

On comparing the circuit of Figure 1 with the circuit of Figure 3, the circuit of Figure 3 is considerably more complex. It may appear that the advantage gained from the single phase clock signal are outweighed by this added complexity. However, in practice, in a VLSI circuit, the single phase clocking arrangement of the present invention can be implemented with only a 1 to 2 percent increase in actual circuit area. This increase does not take into account the area saved by eliminating the buses required to distribute the multiple phase signal.

Thus, an improved logic arrangement for CMOS VLSI has been described where only a single phase clocking signal is used.

CLAIMS

1. In a complementary metal-oxide-semiconductor (CMOS) integrated circuit, a clock logic arrangement comprising:

a first logic circuit having first input transistors, said first logic circuit being coupled to receive an input signal;

5 a second logic circuit having second input transistors, the output signal of said first logic circuit being coupled to said second logic circuit;

said first and second logic circuits being coupled to receive the same phase of a clocking signal;

10 the size of said first and second input transistors being different such that said first logic circuit accepts said input signal during a first period of said clocking signal and said second logic circuit accepts said output signal from said first logic circuit during a second period of said clocking signal, said first
15 and second periods being nonoverlapping;

whereby a single clocking signal is used for said first and second logic circuits.

2. The CMOS logic arrangement of Claim 1 wherein said first
20 and second logic circuits are each level-triggered flip-flops forming together an edge-triggered flip-flop.

3. The CMOS logic arrangement of Claim 2 wherein said first
and second periods of said clocking signal are separated by a third
25 period of said clocking signal.



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4. The CMOS logic arrangement of Claim 3 wherein said first and second logic circuits are static circuits.

5. The CMOS logic arrangement of Claim 4 wherein said first and second logic circuits are bistable circuits.

6. In a complementary-metal-oxide (CMOS) integrated circuit, a clocked logic arrangement comprising:

a master bistable circuit comprising a first and a second cross-coupled gates, said master circuit being coupled to receive an input signal, said first and second gates including input transistors at least some of which are coupled to receive said input signal;

a slave bistable circuit comprising cross-coupled third and fourth gates, said third and fourth gates having input transistors some of which are coupled to receive the output signal from said master circuit;

other input transistors of said first, second, third and fourth gates being coupled to receive the same phase of a clocking signal;

the size of certain of said input transistors of said first and second gates being different than the size of said input transistors of said second and third gates such that said master circuit accepts said input signal during a first period of said clocking signal and said slave circuit accepts said output signal from said master circuit during a second period of said clocking signal, said first and second periods being nonoverlapping;



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whereby a single clocking signal is used for said master and slave circuits.

7. The CMOS logic arrangement of Claim 6 wherein said first and second periods of said clocking signal are separated by a third period of said clocking signal.

8. The CMOS logic arrangement of Claim 7 wherein said input signal is coupled to said second gate through an inverter.

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9. The CMOS logic arrangement of Claim 8 wherein said first and second gates each comprise an AND gate and NOR gate and wherein said third and fourth gates each comprise an OR gate and NAND gate.

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10. The CMOS logic arrangement of Claim 7 wherein said input transistors of said first, second, third and fourth gates comprise transistors of both a first and a second conductivity type.

11. A clock logic arrangement substantially as herein described with reference to the accompanying drawings.

