Claims

1. A method for generating a reference clock signal, the method comprising:

discharging a capacitive element to a discharged state, when a reset signal has a predetermined reset state;

charging the capacitive element from the discharged state to a first voltage, when a charge signal has a predetermined charge state;

comparing the first voltage to a zero voltage, when a compare signal has a predetermined compare state;

generating a second voltage based on the comparing of the first voltage to the zero voltage;

generating a clock signal based on the second voltage, using an oscillator; and

generating each of the reset signal, the charge signal and the compare signal, based on the clock signal.

2. The method of claim 1, wherein the zero voltage is a virtual zero voltage at input terminals of an operational amplifier, the operational amplifier being connected to a negative feedback loop.

3. The method of claim 1, wherein the capacitive element is in the discharged state when a voltage across the capacitive element is a negative value of a supply voltage.

4. The method of claim 3, wherein the capacitive element is charged to the first voltage by a resistive element coupled to the supply voltage.

5. The method of claim 4, wherein a time taken to charge the capacitive element from the discharged state to zero voltage is dependent on a capacitance of the capacitive element and a resistance of the resistive element.

6. The method of claim 1, wherein a frequency of the clock signal is dependent on the time taken to charge the capacitive element from the discharged state to zero voltage.

7. The method of claim 1, wherein generating the charge signal comprises dividing the clock signal.

8. The method of claim 1, further comprising:

phase shifting the clock signal to provide a first output signal, a second output signal, a third output signal, a fourth output signal and an output clock signal.

9. The method of claim 8, wherein each of the first output signal, the second output signal, the third output signal, the fourth output signal and the output clock signal is phase-shifted from the clock signal by different multiples of a phase shift constant, respectively.

10. A reference clock signal generator comprising:

a discharging circuit configured to discharge a capacitive element to a discharged state, when a reset signal has a predetermined reset state;

a charging circuit configured to charge the capacitive element from the discharged state to a first voltage, when a charge signal has a predetermined charge state;

a comparison circuit configured to compare the first voltage to a zero voltage when a compare signal has a predetermined compare state, wherein the comparison circuit is further configured to generate a second voltage based on the comparing of the first voltage to the zero voltage;

an oscillator configured to generate a clock signal based on the second voltage; and

a control logic circuit configured to generate each of the reset signal, the charge signal and the compare signal, based on the clock signal.

11. The reference clock signal generator of claim 10, wherein at least one of the discharging circuit or the charging circuit comprises a differential frequency-to-voltage converter.

12. The reference clock signal generator of claim 10, wherein the comparison circuit comprises a differential integrator.

13. The reference clock signal generator of claim 10, wherein the oscillator comprises a voltage-controlled oscillator.

14. The reference clock signal generator of claim 10, wherein the charging circuit comprises a resistive element.

15. The reference clock signal generator of claim 14, wherein the resistive element has a low temperature coefficient.

16. The reference clock signal generator of claim 10, wherein both the discharging circuit and the charging circuit are coupled to a common supply voltage.

17. The reference clock signal generator of claim 10, further comprising:

a plurality of chopping switches coupled to the comparison circuit.

18. The reference clock signal generator of claim 17, wherein the plurality of chopping switches are configured to be operated by a chop signal, the chop signal being dependent on the clock signal.

19. The reference clock signal generator of claim 10, further comprising:

a low pass filter configured to receive the second voltage and further configured to provide a filtered voltage to the oscillator.

20. The reference clock signal generator of claim 10, wherein the comparison circuit comprises an operational amplifier connected to a negative feedback loop, wherein input terminals of the operational amplifier are configured to provide the zero voltage.