

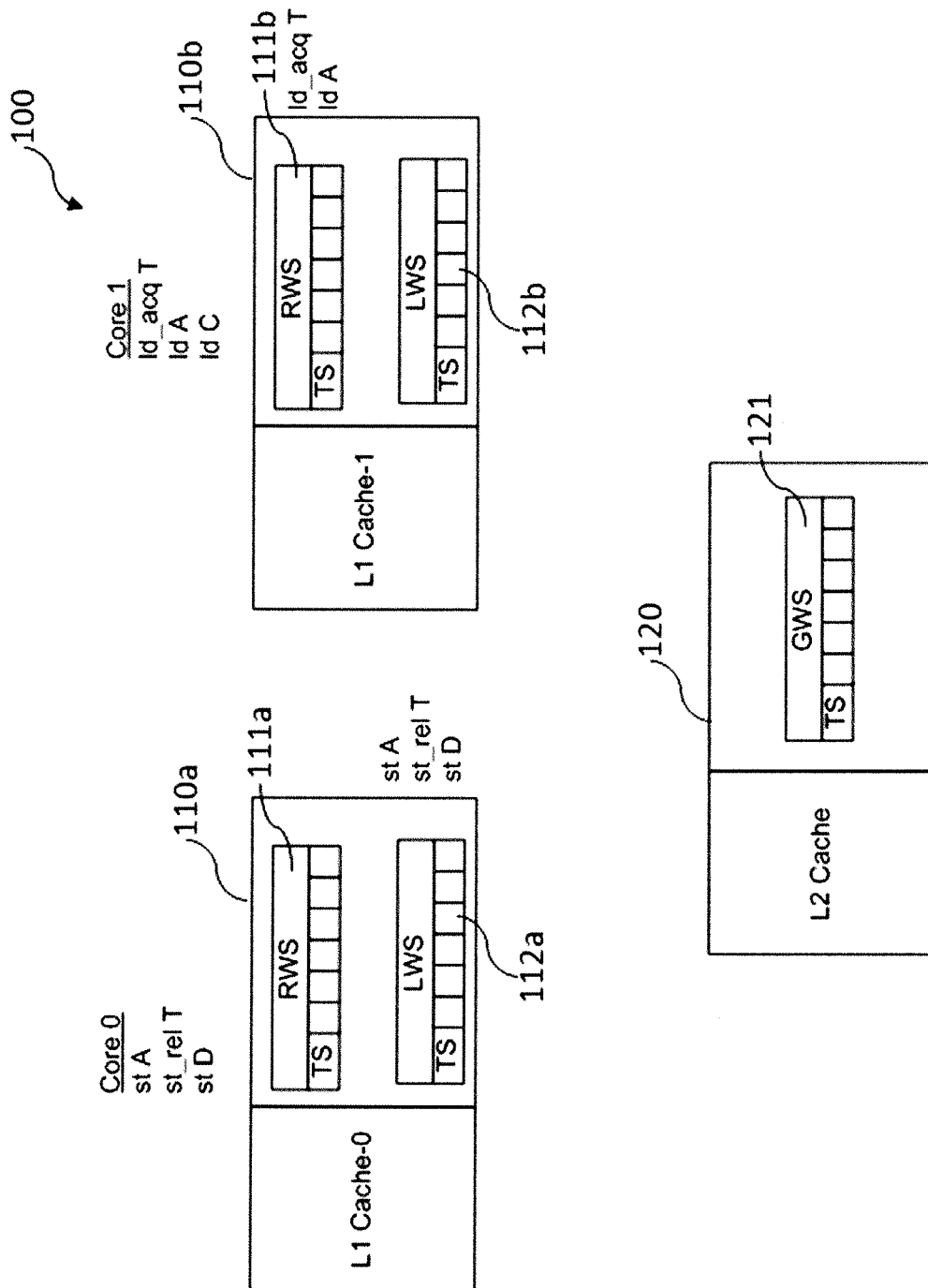


Figure 1(a)

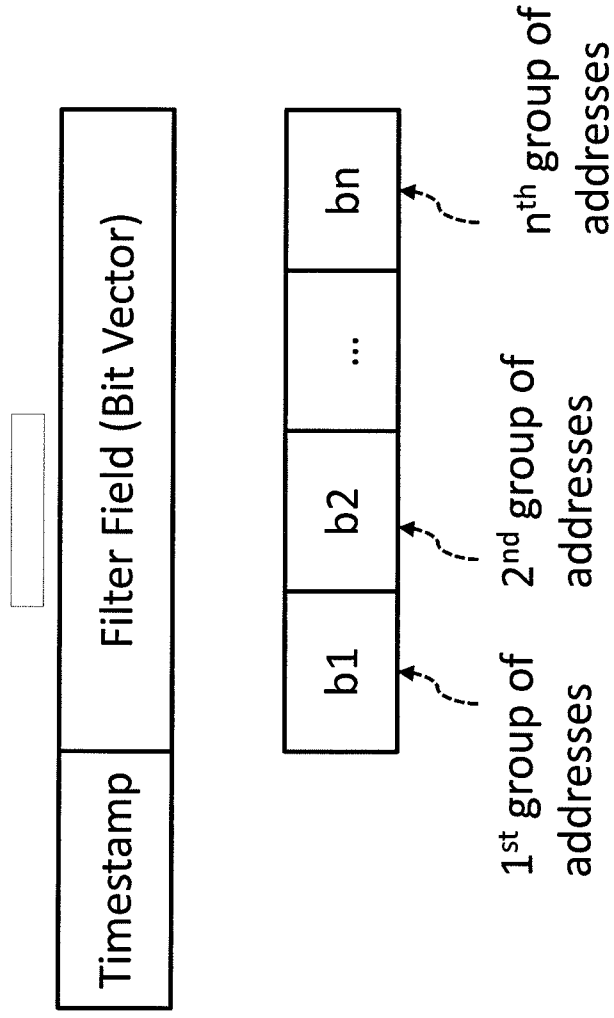


Figure 1(b)

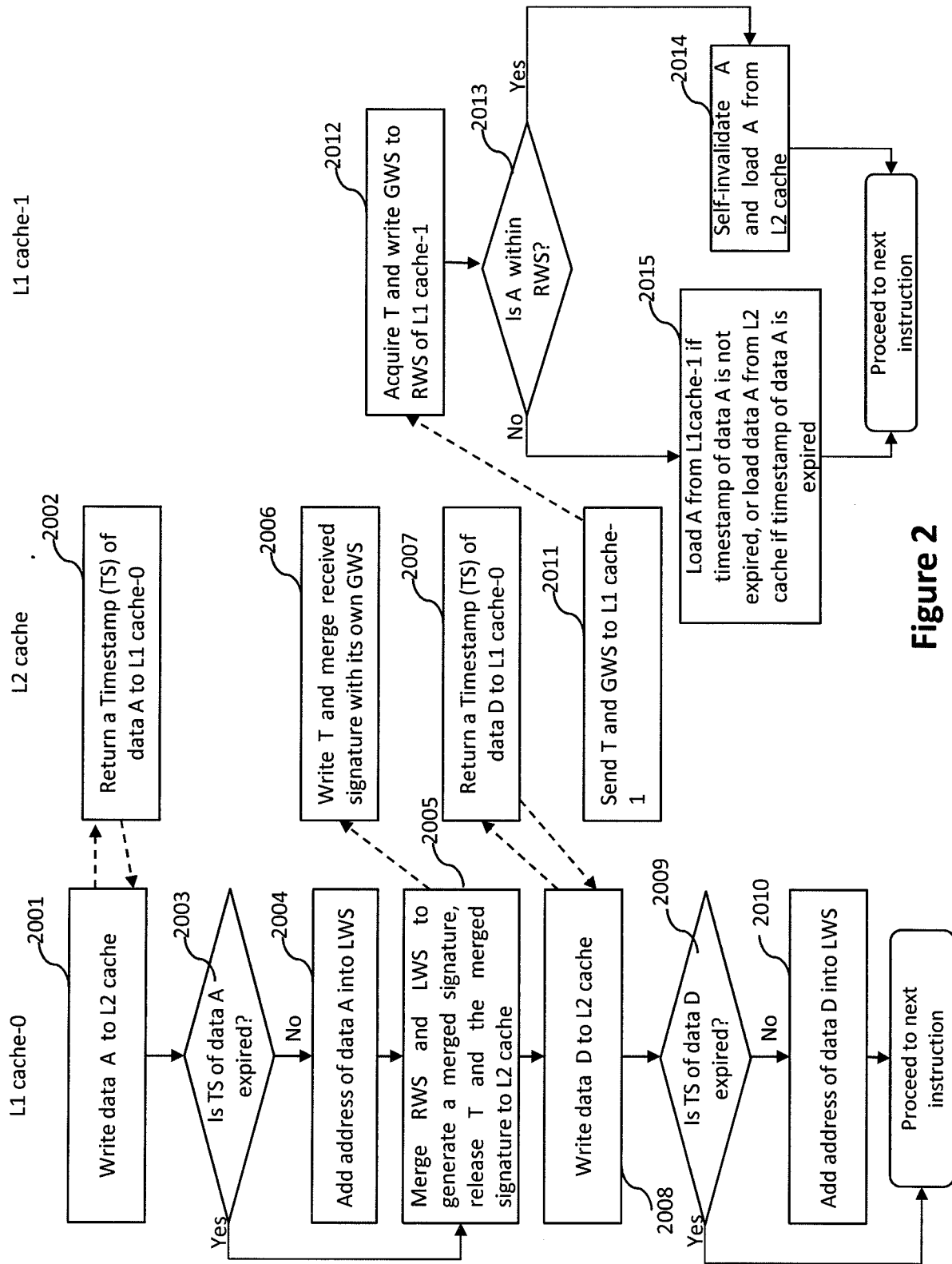


Figure 2

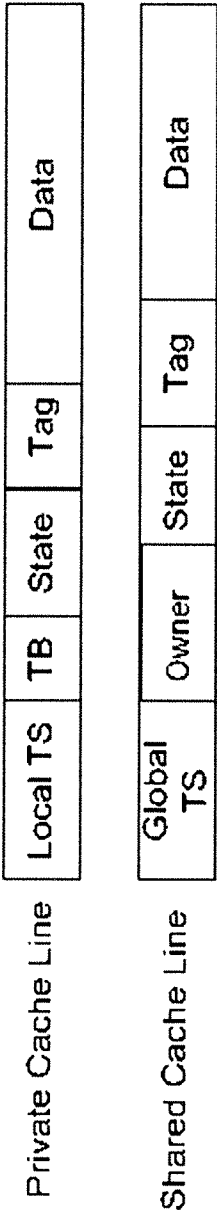


Figure 3

Core 0
st A, 1
st_rel T, 0

Core 1
ld_acq T
R1: ld A
...
R2: ld A

Figure 4

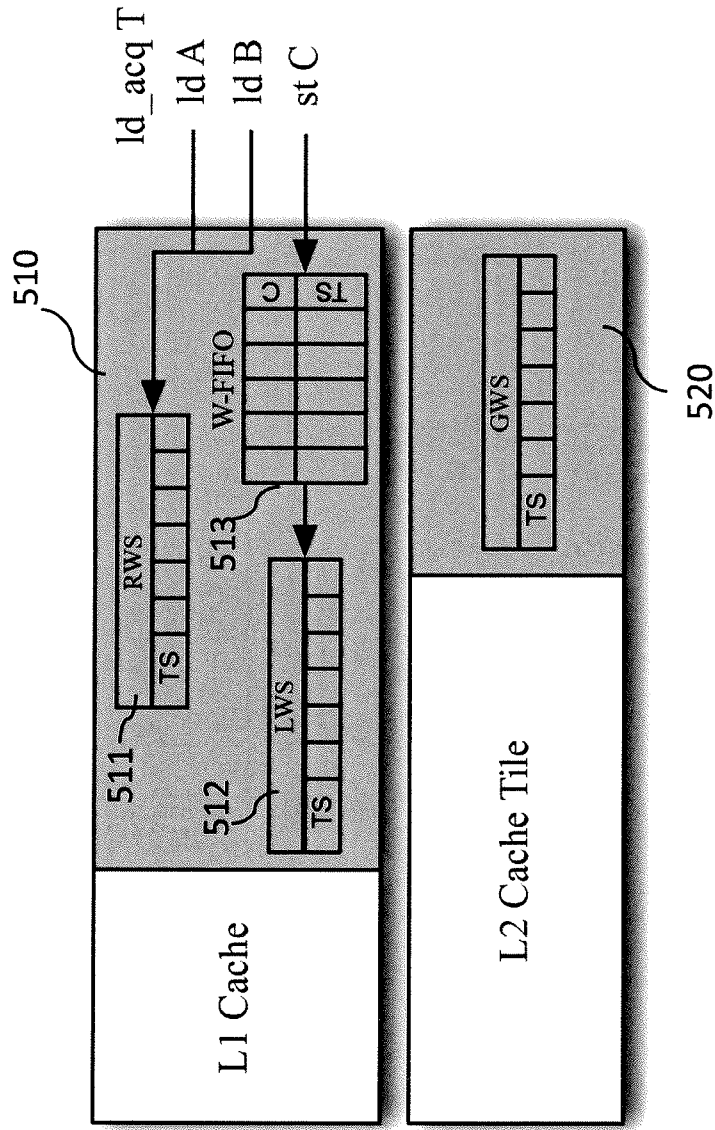


Figure 5