

Semiconductor wafer comprising a monocrystalline group-IIIa nitride layer

Field of the invention

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The present invention relates to a semiconductor wafer comprising a monocrystalline substrate wafer consisting essentially of silicon and a monocrystalline main group-IIIa (IUPAC group 13, Boron family elements) nitride layer, especially $\text{In}_x\text{Al}_z\text{Ga}_{1-(x+z)}\text{N}$ with $0 \leq x, z, (x+z) \leq 1$.

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Background of the Invention

Monocrystalline gallium nitride (GaN) is of increasing importance as a substrate for producing light emitting diodes (LEDs) and field effect transistors (FETs) for high power and high frequency applications. The surface area of the substrate is a key issue for the productivity of the manufacturing process and therefore for the cost of a LED or FET. The deposition of high quality GaN epi layers is hindered by the availability of native or closely matching substrates.

20 As monocrystalline silicon substrates with diameters of up to 300 mm or even up to 450 mm are currently available with high crystal and surface quality, efforts are being made to use monocrystalline silicon as a substrate for the epitaxial growth of GaN. However, due to the large lattice mismatch of 17 % between GaN(0001) and Si(111) and the large difference in the thermal expansion coefficients (TEC) of the two materials, high quality GaN layers cannot be grown directly on silicon (Si). The large difference in lattice and thermal mismatch results in a multitude of defects, high mechanical stresses in the film, wafer warpage and even cracking and delamination of the grown group-IIIa nitride films.

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For this reason, many types of intermediate or buffer layers have been proposed in order to increase the quality of the epitaxially grown GaN layer.

One of the predominantly used methods to grow GaN on Si is depositing AlN as a seed layer followed by engineered buffer layers to reduce strain. Epitaxial lateral over (ELO) growth or Pendeo epitaxy approaches using additional masking layer, e.g. ex-situ SiO₂ or in-situ SiN, are well-known techniques to reduce threading dislocations. However, retaining compressive strain in GaN film during growth is very difficult while using these techniques.

M. Moram et al., *J. Crystal Growth* 308 (2007), 302-308 teach the use of an epitaxial (111) oriented scandium nitride (ScN) buffer layer as a basis for GaN epitaxy. The ScN layers with a thickness ranging from 50 to 450 nm were grown on n-type Si(111) wafers using gas-source molecular beam epitaxy (GS-MBE) with ammonia as the nitrogen precursor. GaN layers were grown on the ScN/Si(111) templates using a Thomas Swan close-coupled showerhead MOVPE reactor operating at 100 Torr. In preparation for GaN growth, each template used was heated to the growth temperature at a rate of 1 K/s under a flow of 10 slm (standard liter per minute) ammonia (NH₃) and 10 slm hydrogen (H₂) in order to remove any native oxide from the surface of the ScN layers. The ScN buffer layer was rough and full of defects. The GaN grew on the ScN surface in the form of dislocation-free islands. By varying the GaN growth temperature, the GaN islands could be caused to coalesce in order to yield a smooth GaN film, but at the same time the density of threading dislocations on the surface of the GaN layer increased considerably up to $5 \times 10^9 \text{ cm}^{-2}$.

W. C. Lee et al., *J. Crystal Growth* 311 (2009), 2006-2009 disclose single-crystalline scandium oxide (Sc₂O₃) as a template for GaN epitaxy. Sc₂O₃ films were deposited using e-beam evaporation from a high-purity powder-packed-sintered Sc₂O₃ oxide source. A few monolayers of aluminum (Al) were deposited on the Sc₂O₃ surface using molecular beam epitaxy (MBE), followed by the exposure to nitrogen plasma for nitridation in order to form a thin aluminum nitride (AlN) layer. GaN was deposited on top of this layer. The substrate temperature for growing AlN was at about 645 °C in the beginning

and was raised to 720 °C, which was also used for the rest of the GaN growth. The method results in a high defect density in the Sc₂O₃ buffer and a limited GaN layer quality. Dislocations occurred in a density in the range of 10¹⁰ cm⁻³. The dislocations propagated throughout the layer starting from the Sc₂O₃/Si interface.

EP 2 779 213 A1 discloses a semiconductor wafer comprising a monocrystalline substrate wafer consisting essentially of silicon and having a (111) surface orientation, a monocrystalline layer of Sc₂O₃ having a (111) surface orientation, a monocrystalline layer of ScN having a (111) surface orientation, and a monocrystalline layer of Al_zGa_{1-z}N with 0 ≤ z ≤ 1 having a (0001) surface orientation.

Another method is deposition on patterned Si substrate to reduce both, line defects and wafer warpage. D. Wang et al., *J. Appl. Phys.* 97, 056103 (2005) "Micro-Raman-scattering study of stress distribution in GaN films grown on patterned Si(111) by metal-organic chemical-vapor deposition" (CVD) investigated AlN followed by GaN directly deposited on arrays of squares and rectangular stripes with a 3.5μm height and different lateral dimensions (1–200μm) on Si substrates.

Problem to be solved

It is still an object of the invention to provide a monocrystalline group-IIIa nitride layer with a reduced defect density grown on a silicon substrate.

Summary of the invention

Subject-matter of the present invention is a semiconductor wafer and a method for producing such a semiconductor wafer according to the independent claims.

The semiconductor wafer comprises a monocrystalline substrate wafer consisting essentially of silicon, preferably a Si(111) or Si(001) wafer. The monocrystalline substrate wafer is structured to have numerous monocrystalline silicon tips on its top surface, the monocrystalline silicon tips being separated from each other. Each monocrystalline silicon tip is covered in the given order with a group-IIIB silicide layer and a group-IIIB nitride layer generating group-IIIB nitride pads or a coalesced group-IIIB nitride film, where group-IIIB stands for IUPAC group 3, Scandium family elements, especially Scandium (Sc) and Yttrium (Y). The group-IIIB silicide layer is a closed layer and preferably consists of $Y_{1-z}Sc_zSi_x$ with $0 \leq z \leq 1$. Preferably, the group-IIIB silicide layer has a thickness which is not less than 5 nm. The group-IIIB nitride layer is preferably either a single layer of ScN or YN, or a double layer of YN and ScN (YN/ScN or ScN/YN), or a multiple mixed (of different stoichiometry) or graded layer of $Y_{1-x}Sc_xN$ with $0 \leq x \leq 1$. Finally, the monocrystalline group-IIIA nitride layer, especially $In_xAl_zGa_{1-(x+z)}N$ with $0 \leq x, z, (x+z) \leq 1$ is grown on the group-IIIB nitride pads or film. The group-IIIA nitride layer can be a coalesced film or a structured layer, e.g. an array of (nano-) rods, blocks, tips or pyramids.

In this invention the prior art problems are addressed using nanoheteroepitaxy technique (single-crystal growth of one semiconductor on another) by structuring of the substrate wafer in such a way that "nanotips", i.e. thin needle like Si structures of e.g. several 1 nm – 10 μm bottom wide and 100 nm – 50 μm high structures with a certain center-to-center distance (period) (100 nm - 10 μm) to each other are created.

Then, the topmost part of the nanotips is transformed from Si to group-IIIB silicide, preferably $ScSi_x$ or YSi_x , keeping the epitaxial relationship of subsequent layers, followed by the deposition of epitaxial group-IIIB nitride, preferably ScN, especially ScN(111). Finally, group-IIIA nitride is deposited on top of group-IIIB nitride. It is advisable that in case of a coalesced group-IIIA nitride film on group-IIIB nitride pads the contact area between the group-IIIB

nitride pads and the coalesced group-IIIA nitride film is not more than 50% of the coalesced group-IIIA nitride film.

According to a preferred embodiment of the invention, the thickness of the
5 group-IIIB silicide layer is not more than 50 nm.

According to a preferred embodiment of the invention, group-IIIB nitride is deposited on top of group-IIIB silicide by in situ nitridation of group-IIIB silicide surface, preferably ScSi_x or YSi_x surface, especially $\text{ScSi}_x(0001)$ or $\text{YSi}_x(0001)$
10 surface, or by MBE technique.

This invention addresses the issue of mechanical strain due to the possibility of the Si nanotips to absorb part of the strain in an elastic manner. Absorption of the strain due to the elastic deformation of epilayer depends upon the volume of
15 3D void network in between Si and group-IIIA nitride layer. Optimized structure releases the stress and avoids cracking of group-IIIA nitride layer upon cooling down from the deposition temperature.

This invention addresses the lattice mismatch by the formation of intermediate
20 layers. Preferably, the group-IIIB silicide topping of the Si nanotips is hexagonal $\text{Y}_{1-z}\text{Sc}_z\text{Si}_x(0001)$ with $0 \leq z \leq 1$ with a lattice mismatch to Si(111) of -4.7%.

According to a preferred embodiment group-IIIB nitride on top of the group-IIIB silicide topping is epitaxial $\text{ScN}(111)$ with a lattice mismatch to GaN of only -0.1% resulting in the suppression of the formation of extended defects like e.g.
25 misfit and threading dislocations which could be detrimental on the operation of a device made out of the deposited group-IIIA nitride layer. In conventional method of group-IIIA nitride film deposition on Si, SiN formation at Si and nitride film interface may cause epitaxial relationship problem. However, this invention avoids the formation of SiN.

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C. Nörenberger et al., *Surf. Sci.* 600, 4126 (2006) "Surface structures of scandium silicides grown on Si(111) studied by STM, AFM and electron

diffraction" investigated the formation of ScSi on Si(111) at different temperatures and revealed that if scandium silicide layers are grown at 900–920°C, they consist of the hexagonal ScSi₂ with the (110) and (101) faces parallel to the Si(111) surface. In the introduction of this publication it is stated, that a few monolayers of the hexagonal ScSi₂ have also been investigated as a possible interfacial layer when growing ScN on Si(111), which is a promising buffer layer for the growth of GaN on Si(111).

The inventive semiconductor wafer can advantageously be used as a substrate for producing light emitting elements (laser diode or LED etc.) and field effect transistors (FETs) for high power and high frequency applications. Light extraction efficiency of light emitting structure and the electrical breakdown voltage of the power transistor structure can be improved by fabricating respective structure on top of the inventive semiconductor wafer than on the classical GaN on Silicon approach.

The inventive semiconductor wafer can advantageously also be used for microstructure printing because well defined patches of GaN can be easily transferred by a separation step from the tips to another substrate.

Further advantages and embodiments of the invention will become apparent from the description and the appended figures.

It should be noted that the previously mentioned features and the features to be further described in the following are usable not only in the respectively indicated combination, but also in further combinations or taken alone, without departing from the scope of the present invention.

In the drawings:

Figure 1 schematically shows preferred steps for producing a silicon wafer having silicon nanotips.

Figure 2 schematically shows a preferred step for silicidation of silicon nanotips and different possibilities to deposit ScN as group-IIIB nitride on the silicidated nanotips to generate ScN pads.

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Figure 3 schematically shows a preferred step for depositing a coalesced film as GaN layer on the ScN pads.

Figure 4 schematically shows a preferred step for depositing nanorods as GaN layer on the ScN pads.

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Detailed description of the invention and the preferred embodiments

In the drawings preferred embodiments for producing a semiconductor wafer according to the invention comprising a monocrystalline substrate wafer consisting essentially of silicon and a monocrystalline GaN layer as group-IIIA nitride layer are shown.

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Within the scope of the invention, a Si nanotips approach (for providing flexible seed area and thus opportunity for antiphase domain (APD) free group-IIIA nitride growth on Si by growth from one critical nucleus only) is combined with an innovative layer stack without using the classical AlN/AlGaIn/GaN approach.

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According to the preferred embodiment of the invention shown in the figures and explained in more detail below it is build up on Si nanotips a layer stack of:

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- 1) ScSi_x as a preferred embodiment of $\text{Y}_{1-z}\text{Sc}_z\text{Si}_x$ with $0 \leq z \leq 1$ in turn as a preferred embodiment of group-IIIB silicide: Epitaxial silicidation (an annealing (sintering) process resulting in the formation of metal-Si alloy (silicide)) of the Si nanotips to avoid GaN reaction with Si.
- 2) ScN as a preferred embodiment of $\text{Y}_{1-x}\text{Sc}_x\text{N}$ with $0 \leq x \leq 1$ in turn as a preferred embodiment of group-IIIB nitride: Epitaxial ScN growth to have zero lattice mismatch growth template

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3) GaN as a preferred embodiment of $\text{In}_x\text{Al}_z\text{Ga}_{1-(x+z)}\text{N}$ with $0 \leq x, z, (x+z) \leq 1$ in turn as a preferred embodiment of group-IIIA nitride: Functional GaN patches e.g. by ELO

so that the resulting preferred heterostructure is given by Si/ScSi_x/ScN/GaN. It

5 is noted that group-IIIB chemistry behaves similar to Al chemistry which provides a good guideline for stability of compounds discussed here.

Referring to figure 1, in a first step, a monocrystalline substrate wafer 1 is provided, which consists essentially of monocrystalline silicon, preferably it
10 consists of 90 % to 100 % silicon, more preferably of 98 % to 100 % silicon. The substrate wafer 1 may comprise the usual dopants or impurities generally known in the field of silicon technology. The substrate wafer 1 for instance has a crystal surface orientation of Si(111). The substrate wafer 1 may have a diameter of 100 mm to 450 mm. The surface of the substrate wafer is preferably
15 polished.

Preferably, the substrate wafer 1 is annealed at high temperature to obtain a high quality silicon surface. The anneal temperature is between 600 and 1250 °C. The annealing may be performed in a vacuum or under a reducing
20 atmosphere, preferably comprising hydrogen, for 30 seconds to 30 minutes, preferably from one to ten minutes.

In a second step, nanotips 2 are formed on the upper surface of the silicon substrate layer 1. In prior art, different techniques for forming nanotips are
25 known, e.g. by defining the tips by photo lithography and removing Si by chemical and/or mechanical processes, e.g. etching, especially anisotropic wet etching. A height H, a width at the base W and a period P of the nanotips can be controlled by the lithography and etching process.

30 The height H advantageously is in the range of 100nm - 50 µm, the width W at the base of a nanotip advantageously is in the range of several 1nm - 10µm, and the period P advantageously is in the range of 100nm - 10µm. The

maximum width ratio of the nanotips (width at the base : width at the top) is preferably 1000 : 1 and the maximum aspect ratio (height : width at the base) 1 : 1.

- 5 In a third step, a growth mask 3, in the shown example amorphous SiO_2 , is deposited on the silicon substrate wafer 1. Different material, e.g. SiN , can also be used.

10 Finally, Si areas on the upper ends of the nanotips are uncovered which form the basis for a subsequent silicidation step. This can be done

- a) by a polishing step, e.g. by duration of chemical mechanical planarization (CMP) process,
- b) by a (wet) etching step, e.g. with hydrofluoric acid (HF), or
- c) by an anisotropic (wet) etching step, e.g. with potassium hydroxide (KOH).

15 Having uncovered tips as shown in b) and c) may lead to a deflection of dislocations in the GaN layer and thus provide a better quality. Examples a) and b) result in a planar surface, whereas example c) results in a rough surface with Si tips being recessed in SiO_2 indentations. b) and c) offer the advantage of
20 dislocation reduction through deflection. a) and b) are advantageous as they offer planar growth. c) can be desirable for specific applications due to a potential rough surface or 3D growth.

25 In figure 2 further steps according to preferred embodiments of the invention are shown. The shown steps are performed on a silicon wafer having silicon nanotips according to example a) of figure 1, shown in the middle of the first line of figure 2.

30 In a first step, a thin scandium (and/or yttrium, in another not shown embodiment) layer 4 is deposited all over the cleaned patterned silicon tip area. Alternatively, a KOH etch might be applied before to achieve $\langle 111 \rangle$ faceted Si tips.

In a second step, higher temperatures are applied to form ScSi_x 5 as a preferred embodiment of $\text{Y}_{1-z}\text{Sc}_z\text{Si}_x$ with $0 \leq z \leq 1$ as group-IIIB silicide at the top of the Si tips (shown on the left of the first line of figure 2). Preferably, the ScSi_x pads 5 have a (0001) orientation. It is to be noted that Ti is neighboring Sc in the periodic system and TiSi_x processes for low resistance contacts are well established in Si microelectronics.

Since group-IIIB silicides exhibit a small lattice mismatch and a variation in their crystal structures it became possible to grow epitaxial group-IIIB silicides on Si(001) and Si(111) by depositing a thin group-IIIB metal layer and annealing (cf. C. Nörenberger et al., ib.; Baptist et al., *Phys. Rev. Lett.* 64, 311 (1990); Rogero et al., *Phys. Rev. B* 66, 235421 (2002)). It is shown by AFM, STM and LEED studies that ScSi_x can be formed with a hexagonal (0001) structure with 4.78% lattice mismatch on Si(111). Depending on the annealing temperature (450°C-920°C) different ScSi_x surface reconstructions with a terrace width up to 200nm were achieved. Thus, epitaxial single domain ScSi_x films are formed on sufficiently small Si nanotips. It is to be noted that such a detailed surface science investigation is not known on Si(001), however XRD results indicate an orthorhombic ScSi structure at 500°C and an hexagonal $\text{ScSi}_{1.7}$ structure at 900°C, which is very similar with the behavior of Sc on Si(111).

In a further step (shown on the left of the second line), the residual Sc metal is removed from SiO_2 areas by hydrochloride acid (HCl) etching resulting in the ScSi_x pads 5 being still embedded in the SiO_2 (example a)).

Optionally, a further HF etching step can be applied to completely uncover the ScSi_x pads 5 (example b)) or to even remove the SiO_2 almost completely (example c)) for reducing strain.

In the following, ScN islands 6 are deposited on the epitaxial ScSi_x passivated surface (shown in line 3) as a preferred embodiment of $\text{Y}_{1-x}\text{Sc}_x\text{N}$ with $0 \leq x \leq 1$

as group-IIIB nitride, e.g. by MBE or CVD process. Preferably, the ScN islands
6 have a (111) orientation.

In-situ nitridation of the (0001) ScSi_x surface provides a few (up to 10) nm thick
5 ScN(111) layer. A thin layer is preferred because of pronounced roughening
tendency of the material. Nitridation is carried out using either NH₃ gas or one of
many plasma sources, including an electron cyclotron resonance (ECR) or a
radio-frequency (rf) nitrogen plasma source.

10 ScN(111) epitaxy can also be grown on ScSi_x using MBE technique (cf. eg. M.
Moram et al., *J. Cryst. Growth* **308**, 302 (2007)). This technique is in particular
an option if thicker ScN films are required.

The morphology (faceting etc.) and size (small islands of a few microns up to a
15 coalesced film) can be controlled by ELO parameters.

These Si/ScSi_x/ScN pillar structures represent ideal nucleation sites for the low-
strain and low-defect growth of group-IIIA nitride structures.

20 With nanopatterned Si substrates like Si nanotips on Si wafers, it becomes
possible that the lattice mismatch strain between the epitaxial film and the
substrate is not only stored in the substrate – like is inevitably the case for
planar bulk Si substrates – but distributed between the growing epitaxial film
and the nanopatterned Si tips. This so called compliant effect is beneficial to
25 favor the formation of coherent, only elastically relaxed interfaces between
lattice mismatched semiconductors on Si. In other words, the so called critical
thickness for the onset of plastic relaxation in the epitaxial film is substantially
delayed; even to infinity in the most favorable conditions.

30 After formation of ScN, in a final optional step (shown in line 4), SiO₂ can be
etched away using HF chemistry from the template to deposit GaN. However, a
thin SiO₂ layer (<10nm thick) can be intentionally left in between and on the side

wall of the nanotips to protect further GaN deposition on these that helps to form a 3D void network as shown on the right of line 3.

Referring now to figures 3 and 4, in a next step GaN is deposited on the ScN islands 6 as a preferred embodiment of $\text{In}_x\text{Al}_z\text{Ga}_{1-(x+z)}\text{N}$ with $0 \leq x, z, (x+z) \leq 1$ as group-IIIa nitride to produce a semiconductor wafer 10 according to a preferred embodiment of the invention. A coalesced GaN film 7 or GaN nanorods 8 (diameter preferably of several nanometers up to $10 \mu\text{m}$; height preferably between several hundred nanometers and $10 \mu\text{m}$) can be formed on the ScN islands 6 controlled by the depositing process parameters.

As mentioned above, growth of high quality GaN epilayers on Si is difficult. High density of threading dislocations due to $\sim -17\%$ in-plane lattice mismatches and severe wafer bow and even layer cracking due to more than 55% coefficient of thermal expansion (CTE) mismatches between GaN and Si are the main challenges. In addition, Si heavily reacts with impinging Ga and NH_3 at high temperature that degrades the layer quality and wafer bow. AlN seed and AlGaIn buffer layers are typically used to overcome these problems. Differently from classical approach, according to the invention the growth area of Si is covered with group-IIIB- Si_x followed by group-IIIB-N. In conventional method of group-IIIa nitride film deposition on Si, SiN formation at Si and nitride film interface may cause epitaxial relationship problem. However, silicidation process avoids the formation of SiN. Proper design of pitch between nanotips and the height can limit the diffusion of reactive species inside the uncovered area in between nanotips. Basically, narrow pitch ($P < 3 \mu\text{m}$) and a longer size ($H > 3 \mu\text{m}$) of nanotips avoid nuclei formation at the bottom as well as on the sidewall of the structure (cf. eg. M.Ali et al., *J. Cryst. Growth* 315, 188 (2011)).

A faster growth of $\langle 0001 \rangle$ facet than $\langle 10\bar{1}1 \rangle$ facet of GaN results in the formation of well-known pyramidal structure on patterned substrate (cf. e.g. A. Strittmatter et al., *Appl. Phys. Lett.* 78, 727 (2001); S. Tanaka et al., *Appl. Phys. Lett.* 79, 955 (2001)). However, due to growth rate anisotropy, lateral or vertical

extension can be controlled by adjusting group-V-IIIa ratio (NH_3 and MO precursor flows), growth temperature and pressure. Lateral growth can be promoted with increased group-V-IIIa ratio and high growth temperature. A coalesced GaN film 7 (figure 3) or nanorod structure 8 (figure 4) can be formed as a template for further device structure. GaN film or nanorod structures may consist of structures having a combination of group-IIIa elements (Al, Ga and In).

One concept of the invention to solve wafer warpage problem in GaN on Si epiwafer and reduce threading dislocation density in GaN epilayer is using nanoheteroepitaxy where the contact area between Si substrate and group-IIIa layer is less than 100%, preferably not more than 50% of the grown film. Thin structure of group-IIIB- Si_x and group-IIIB-N are formed on the contact region between Si and group-IIIa nitride film to reduce the lattice mismatch whereas 3D void network is embedded in the non-contact region to absorb the strain evolving from thermal expansion coefficient mismatch between Si and nitride film.

Size and distribution of growth surfaces for group-IIIa nitride epi can be tuned in a wide range in order to match the requirements for efficient strain management and dislocation reduction. It is possible to grow a coalesced group-IIIa nitride film or nanorod structure by designing the nanotips template structure and growth optimization of group-IIIa nitride.

CLAIMS

1. Semiconductor wafer (10) comprising a monocrystalline substrate wafer (1) consisting essentially of silicon,
the monocrystalline substrate wafer (1) being structured to have tips (3) on its top surface,
each of the tips (3) being covered in the given order with a group-IIIB silicide layer (5) and a group-IIIB nitride layer (6),
the group-IIIB silicide layer (5) having a thickness of not less than 5 nm and
the group-IIIB nitride layer (6) being covered with a monocrystalline group-IIIA nitride layer (7, 8).
2. Semiconductor wafer (10) according to claim 1, wherein a contact area between the group-IIIB nitride layer (6) and the monocrystalline group-IIIA nitride layer (7, 8) is not more than 50% of the grown group-IIIA nitride layer in case of a coalesced film.
3. Semiconductor wafer (10) according to claim 1 or 2, the tips having a height between 100 nm and 50 μm , preferably at least 3 μm .
4. Semiconductor wafer (10) according to any one of the preceding claims, the tips having a bottom width between 1 nm and 10 μm .
5. Semiconductor wafer (10) according to any one of the preceding claims, the tips having a center-to-center distance between 100 nm and 10 μm , preferably at most 3 μm .
6. Semiconductor wafer (10) according to any one of the preceding claims, the group-IIIB nitride layer (6) having a (111) surface orientation and/or being either a single layer of ScN or YN, or a double layer of ScN and YN, or a multiple mixed or graded layer of $\text{Y}_{1-x}\text{Sc}_x\text{N}$ with $0 \leq x \leq 1$.

7. Semiconductor wafer (10) according to any one of the preceding claims, the group-IIIB silicide layer (5) having a (0001) surface orientation and/or being a $Y_{1-z}Sc_zSi_x$ layer with $0 \leq z \leq 1$.
8. Semiconductor wafer (10) according to any one of the preceding claims, the monocrystalline group-IIIA nitride layer (7, 8) being a coalesced film or a structured layer, especially comprising an array of rods, blocks, tips or pyramids.
9. Semiconductor wafer (10) according to any one of the preceding claims, the monocrystalline group-IIIA nitride layer (7, 8) being a monocrystalline $In_xAl_zGa_{1-(x+z)}N$ layer with $0 \leq x, z, (x+z) \leq 1$.
10. Semiconductor wafer (10) according to any one of the preceding claims, the monocrystalline group-IIIA nitride layer (7, 8) having a (0001) surface orientation.
11. Semiconductor wafer (10) according to any one of the preceding claims, the monocrystalline substrate wafer (1) being a Si(111) or Si(001) wafer.
12. Use of a semiconductor wafer (10) according to any one of the preceding claims as a substrate for producing light emitting elements, field effect transistors, or for microstructure printing.
13. Method for producing a semiconductor wafer (10) according to any one of the preceding claims, comprising the steps of:
 - providing a monocrystalline substrate wafer (1),
 - structuring the substrate wafer (1) to form tips (3) on its top surface,
 - covering the tips (3) in the given order with a group-IIIB silicide layer (5) and a group-IIIB nitride layer (6),
 - the group-IIIB silicide layer (5) having a thickness of not less than 5 nm,
 - covering the group-IIIB nitride layer (6) with a monocrystalline group-IIIA nitride layer (7, 8).

14. Method according to claim 13, the step of covering the tips (3) in the given order with a group-IIIB silicide layer (5) and a group-IIIB nitride layer (6) comprises forming the group-IIIB silicide layer (5) by a silicidation process.

15. Method according to claim 13 or 14, the step of covering the tips (3) in the given order with a group-IIIB silicide layer (5) and a group-IIIB nitride layer (6) comprises depositing group-IIIB nitride on top of group-IIIB silicide by in situ nitridation of group-IIIB silicide surface, or by MBE technique.