

The invention relates to a circuit arrangement for the synchronisation of a data processor utilising a serial data stream in accordance with the first part of claim 1

For the serial transmission of digital signals which are arranged in a predefined frame structure, it is known to make use of a data processor which carries out program controlled calculations for the data processing. For the identification of appertaining data items, control signals are transmitted which cause the data processor to perform predetermined program steps.

In highly integrated data processors, restrictions are made regarding the provision of control ports in order to be able to use the standard sized housings or else to keep the dimensions of the housing and the number of connecting pins within limits.

The object of the invention is to develop a circuit arrangement for the synchronisation of a data processor such that different control signals can be fed in via a single control port.

This object is achieved in a circuit arrangement in accordance with the first part of claim 1 by the features given in the characterising part.

With the invention, different control signals are initially obtained of which the first respectively identify an appertaining data sequence and the second indicate the occurrence of a data sequence matching reference values e.g. a synchronising data word. These separate control signals are then brought together and so combined by a logic circuit that the temporal length forms the criterion as to which of the two control signals is present. This solution is particularly advantageous for control signals of which the one occurs less often but always at the same time as the other.

Further developments and advantageous embodiments of the invention are apparent from the further claims, the description and the drawing which illustrates one embodiment.

In the drawing:

Fig. 1 shows a circuit diagram embodying the invention as a component part of a receiver for digital satellite radio broadcasts,

Fig. 2 a pulse diagram for the explanation of the circuit illustrated in Fig. 1.

The receiver for digital satellite radio broadcasts is provided for receiving radio programmes in accordance with the specification for the radio transmission process in TV-Sat. The interleaving of the programmes into a frame structure and the accommodation of additional programme information in special service frames and special service super frames are more fully described in the DE-OS 33 08 025.

Fig. 2 shows, in the upper part, the special service super frame SAÜ in which pieces of information regarding the type of programme of two respective programmes are transmitted in a blockwise manner. The special service super frame SAÜ encompasses eight special service frames SA of which each comprises a synchronising word and items of programme type information for, at the present time, two programmes, i.e. programme 1+2, programme 3+4, ... programme 15+16. The special service super frame SAÜ begins with the special service frame SA which, after the synchronising word, contains the type of programme information for the programme 1 and the programme 2. The synchronising word, which indicates the new beginning of the special service super frame SAÜ including the first special service frame SA, differs slightly in its bit structure from the synchronising words which respectively introduce the second to eighth special service frames SA.

The bits used for the indication of the synchronising words and items of programme type information are the special service bits transmitted in the main frame A in accordance with the above mentioned specification. These are evaluated by a data processor. However, the data processor is not in the position to carry out a monitoring of the synchronising words occurring in the data stream as well as performing the calculations that have to be carried out. An evaluating circuit takes over this task which, on the basis of the evaluated signals, conveys appropriate control signals to the data processor which thereby recognises the start of certain data sequences.

The control signals emitted by the evaluating circuit consist of first control signals A which mark the end of appertaining data words, in this case, those of 8 bits in length, and of second control signals PR1 which indicate the beginning of the items of programme type information for the programme 1. The first control signals should arrive at the data processor as INTR1 and the second as INTR2. An additional control signal INTR3 may then reach the data processor if the evaluating circuit does not recognise any synchronising signals SYOKN.

The circuit illustrated in Fig. 1 is in the position to bring together these three control signals emitted by the evaluating circuit so that they can be supplied to the data processor via a single control lead as altered signals differing in their pulse length.

For the explanation, the time period in which the items of information regarding the type of programme for the programme 1 will be considered. The special service frame contained in this time period is therefore shown expanded, in Fig. 2 below. A clock pulse T32N having a frequency of 32 kHz derived from the sequence of the special service bits in the data stream serves as the data carrier. This clock pulse is led to a divider 1 which can carry out a frequency division in the ratio between 2^1 and 2^6 . The divider 1 is initially set to a defined state at the beginning of an appertaining data word by the evaluation of an SA synchronising word, in that it is loaded with the value 1 by a load command LD1. By logical combination of the first three positions Q1, Q2, Q3 of the divider 4 by means of a logic gate member 2, a signal A, which arrives at a control input of the data processor via a logic gate member 4 as INTR1, is now produced with each eighth clock pulse T32N.

In order to also transmit over the same control lead a piece of information regarding the beginning of the programme type information of programme 1 which are contained in a control signal PR1, the last 3 positions are monitored by the divider 1 together with a logic gate member 6 on the basis of the clock pulses 16 - 23. These clock pulses are chosen because an auxiliary signal can thereby be generated which begins before one INTR1 and ends after the latter but before a further INTR1. The signal waveform is portrayed as F16-23. By logical decombination of the signal F16-23 with both the signal TR1 as well as with the signal A in a logic gate member 7 and by delaying this signal in a flip-flop 3, a signal B is obtained which lags the signal A by one clock period. By logically combining the signal B with the signal A in a logic gate member 4, there appears a signal INTR2 which comprises double the pulse length of the signal INTR1. This signal is processed by the data processor in such a way that the latter is initially induced by INTR1 to receive data and, after the reception of the data, supplements the information received by INTR2, that here, it relates to data for the programme 1.

Finally, the case is then illustrated, that no synchronising signal is received. This is done by SYKON which indicates the lack of synchronisation by means of the state logical H and arrives at the input of a flip-flop 5 serving as a logic gate

member. A clock signal formed by logically combining the clock pulse T32N as well as F16-23 and A by means of a logic gate member 8 is present at the clock input of the flip-flop 5. The signal C appears at the output thereof. By means of the logical combination of the remaining signals A and B, a signal INTR3, which is static at logical H and which e.g. blocks the data processor from further data processing, is produced beyond the logic gate member 4.



Claims

1. Circuit arrangement for the synchronisation of a data processor utilising a serial data stream, characterised in that, there is provided an evaluating circuit (1, 2) for an appertaining data sequence contained in the data stream which delivers first periodic control signals (A), that a comparison circuit is provided which compares data sequences with a predefined reference value sequence and supplies them to a storage circuit (3) which delivers second periodic control signals (A) that are displaced in time relative to the first control signals and that the first and second control signals (A, B) are supplied to the data processor via a gating circuit (4) as control signals (INTR1, INTR2).

2. Circuit arrangement in accordance with Claim 1, characterised in that, the storage circuit (3) is a flip-flop which displaces the second control signals (B) by the pulse duration of the first (A).

3. Circuit arrangement in accordance with Claim 1 or 2, characterised in that, the gating circuit (4) is an OR circuit.

4. Circuit arrangement in accordance with one or more of the Claims 1 to 3, characterised in that, the first periodic control signals (A) are obtained by means of clock signals T32N which are supplied to a frequency divider (1) whose division ratio corresponds to the number of the bits in a related data word.

5. Circuit arrangement in accordance with Claim 4, wherein the data sequence is incorporated into an at least two stage frame structure, characterised in that, the second periodic control signals (B) are also obtained by means of clock signals T32N which are supplied to a frequency divider (1) whose division ratio corresponds to the number of the appertaining data words contained in a frame SA and that output signals (F16 - 23) of the divider (1) are logically combined with the second control signals (PR1).

6. Circuit arrangement in accordance with one or more of the Claims 1 to 4, characterised in that, there is provided a further comparison circuit which compares data sequences with a predefined reference value sequence and delivers third static control signals (SYOKN) and that, after delay by means of a delay member (5), the third control signals (SYOKN) are logically combined as control signals (C) with the first (A) and second control signals (B) via the gating circuit (4) and are supplied to the data processor as (INTR3).