## Description

### BACKGROUND OF THE INVENTION

The present invention generally relates to a common driver circuit for driving a heavy capacitive load, such as a common electrode or the like of a liquid crystal panel.

A conventional common driver circuit built into a conventional liquid crystal display apparatus of this type is shown in Figure 6. A bias voltage is supplied from variable resistor (2) to a buffer amplifier (1) to which a common amplitude signal (frame pulse) (FP) is inputted. The amplitude of the common amplitude signal is adjusted by adjustment of the bias voltage from variable resistor (2). The D.C. bias of the output of the buffer amplifier (1) is removed by capacitor (C1) and the signal output from capacitor (C1) is newly biased by variable resistor (1). The output of the circuit is supplied to the common electrode of a liquid crystal panel.

In this conventional embodiment, in order to obtain an amplitude signal to which a common bias is added, the direct current component must be removed by the capacitor (C1) from the output of the buffer amplifier (1). This requires a large capacitor (C1). Also, as the common bias depends upon the supply voltages Vcc, - Vee supplied to the variable resistor (3), the common bias also changes as the supply voltages change, producing undesirable influences upon the liquid crystal panel.

Figure 6 illustrates a conventional method in which the direct current component of the common output is removed by capacitor (C1) after amplifying the frame pulse, and a bias is subsequently added by the variable resistor. The amplitude of the common output sometimes varied as much as 8 Vpp at its maximum. Also, the -Vee supply connected to variable resistor (3) sometimes could not be adjusted to the voltage of the power source of the panel, depending upon the bias to be applied. Therefore, the -Vee was required to be taken from much lower voltage (-21V) since the voltage varies independently of the variation in the source power voltage of the panel, the direct current bias may be added to the panel when the power is not stable. When the voltage for determining the bias is taken from the same power line as the power supply of the panel, the bias set by variable resistor 3 varies in the same direction as the variation of the power voltage source, with a disadvantage that the direct current is hard to be applied upon the panel. Also, in the specification of the panel, both the variation in the central voltage of the video signal to be applied to the source driver and the variation in the central voltage of the common output were required to be controlled, even during display driving, power variation and so on. In the video signal, the feedback was already applied and was stable, while in the common output, the specification was not necessarily observed because of the above described causes.

EP-A-0199361 discloses a driver circuit for an LCD display in which the DC bias level of a common electrode signal can be varied by shifting the high and low supply voltages applied to a pair of driving transistors.

### SUMMARY OF THE INVENTION

Accordingly, the present invention has been developed with a view to ameliorating the above described drawbacks and aims to provide a common driver circuit which is capable of feeding a common output provided with a stable bias, with little variation of the common bias, without requiring a large capacitor for removing the direct current component of an input signal.

There is provided a driver circuit for driving a liquid crystal display in accordance with supplied drive signals, the circuit comprising:

an output circuit adapted for driving the liquid crystal display, feeding means for feeding the supplied drive signals to said output circuit and setting means for setting a desired DC bias level for the drive signals;

characterised by detecting means for detecting the DC level of the signal output from the output circuit and control means for controlling the feeding means so as to adjust the said DC bias to said desired level in response to outputs of said setting means and detecting means.

According to such construction, as the common bias from the bias setting means is given to the output circuit and furthermore, when the common bias varies, the variation is compensated by the control means, so that it is normally maintained.

### BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects and features of the present invention will become apparent from the following description taken in conjunction with the preferred embodiment thereof with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram showing a liquid crystal display apparatus incorporating a common driver circuit of the present invention;

Fig. 2 is a block diagram showing the schematic construction of a common driver circuit in accordance with one embodiment of the present invention;

Fig. 3 is a circuit diagram showing a detailed circuit of the block diagram of Fig. 2;

Fig. 4 is a waveform chart of the respective signals at each indicated point of Fig. 1 and Fig. 3;

Fig. 5 is a circuit diagram showing a modified embodiment of the circuit of Fig. 3; and

Fig. 6 is a circuit diagram showing a conventional common driver circuit.

## DETAILED DESCRIPTION OF THE INVENTION

Before the description of the present invention proceeds, it is to be noted that like parts are designated by like reference numerals throughout the accompanying drawings.

Embodiment:

Fig. 1 is a block diagram showing the construction of an entire liquid crystal display apparatus into which a common driver circuit is incorporated. Fig. 2 is a block diagram of a common driver circuit according to one embodiment of the present invention. Fig. 3 is a circuit diagram showing the circuit construction of the respective blocks of Fig. 2. Fig. 4 is a signal waveform chart of the signals at each indicated point of Fig. 1 and Fig. 3.

In the liquid crystal display apparatus of Fig. 1, a LCD panel 40 composed of a TFT array (Thin·Film·Transistor·Array) is provided with a gate driver 40a, a source driver 40b, and a common driver 39 so as to input a gate driver driving signal into a gate driver 40a from a liquid crystal panel controller 38, a source driver driving signal into the source driver 40b, and a common signal into the common driver 39.

A video signal is inputted into a synchronous detaching circuit 31 and a Y/C detaching circuit 33. The synchronous signal which has been synchronously detached in the synchronous detaching circuit 31 is supplied to a liquid crystal panel controller 38 and clamp pulse generator 32 in a sine waveform of 10 MHz or more as shown in Fig. 4(a). In Y/C detaching circuit 33, the video signal is detached into a brilliance signal and a cross signal and is inputted into a video cross signal processing circuit 34. Prime color signals of R, G, B are outputted from the video cross signal processing circuit 34 and are inputted into a brightness, contrast, gamma correcting circuit 35. The clamp pulse of a clamp pulse generator 32 is inputted into the video cross signal processing circuit 34 and the brightness, contrast, gamma correcting circuit 35. The prime color signals R, G, B of the brightness, contrast, gamma correcting circuit 35 are processed in an inverter circuit 36, and are inputted into the source driver circuit 40b as the video signal output from a driver circuit 37. A liquid crystal panel controller 38 inputs a synchronizing signal from a synchronous detaching circuit 31, and also, inputs a clock pulse ck, outputs a gate driver driving signal and a source driver driving signal as a control signal of a panel. At the same time, as a frame pulse (FP) synchronized with the signal or an inversion pulse, a horizontal periodic of 0 through 5V of 15MHz for generating a common signal is outputted. The inversion pulse to be outputted from the liquid crystal panel controller 38 is inputted into an inverter 36 and a common driver 39. A horizontal periodic signal of 15KHz, which has a DC level of 0 through 5V as shown in Fig. 4(b), is inputted into a buffer amplifier 11 of common driver 39 as a common amplitude signal (from a terminal 10 shown in Fig. 2). A control portion (12) for controlling bias amplitude is connected with the buffer amplifier (11). The control portion (12) gives a set value established by an amplitude varying means (13) to the buffer amplifier (11), and also, compares a bias set by a bias setting means (14) with a direct current level fed back from the output circuit side by a comparator, so as to vary the bias by comparison with the output and give it to the buffer amplifier (11). In an operational amplifier (15) connected with the buffer amplifier, the output from the above described buffer amplifier (11) is fed into the (+) input terminal as a pulse signal having a DC level of -1V through -7V with a center bias of -4V as shown in Fig. 4(c). The output of the operational amplifier (15) is supplied to transistors (Q1), (Q2) to drive the heavy capacitive load, with voltage feedback being effected from the output point (a) to the (-) input terminal or comparator 15. With this, the operational amplifier (15) and the buffer amplifiers (Q1), (Q2) comprise a voltage follower 18. The voltage follower constitutes an output circuit (18), the output point (a) is connected with the common electrode of the liquid crystal panel, and the output is fed as a pulse signal which has a DC level of -1V through -7V with - 4V being provided as a center bias as shown in Fig. 4(d). It is also connected to a low-pass filter (16) composed of a resistor (R1) and a capacitor (C1). The output of the low-pass filter is fed to the above-described control portion (12) through a feedback circuit (17) as a signal of -4V as shown in Fig. 4(e). The feedback circuit (17) is composed of an operational amplifier, with the output of the above-described low-pass filter (16) being applied to the positive input terminal, the voltage Vcc/2 is applied to the negative input terminal. The output of the feedback circuit (17) is supplied, as a signal of -4V as shown in Fig. 4(f), to one input terminal of the first and second comparators (20,21 of Fig. 3) constituting one portion of the control portion (12). The direct current voltage set by the bias setting means (14) is supplied to the other input terminal of comparator 20. The output of comparator 21 controls the bias to be given to the buffer amplifier (11) so that the direct current voltage to be given through the feedback circuit (17) from the above-described low-pass filter (16) may conform to the direct current voltage from the above-described bias setting means (14) as a pulse signal varied by the means (13) and (14) in both the DC level and the amplitude as shown in Fig. 4(g).

Figure 3 shows a detailed circuit of the block diagram shown in Fig. 2. The buffer amplifier 11 is composed of an amplifier 19 and resistors R1,R2,R3,R4. The voltage follower 18 is composed of the operation-

al amplifier 15 and a pair of transistors Q1, Q2 for buffer use. The feedback circuit 17 is composed of an amplifier 22 and a resistor R6.

The low-pass filter circuit 16 is composed of a resistor R1 and a capacitor C1, with the direct current component thereof being inputted into the amplifier 22 of the feedback circuit 17. The output of amplifier 22 is supplied to a first comparator 20 and a second comparator 21 of the control portion (12). The control portion 12 is composed of a first comparator 20, a second comparator 21, resistors R7,R8,R9,R10 and a capacitor C2. The amplitude varying means (13) associated with the first comparative 21 is to adjust the amplitude of the output signal from the control portion (12). The bias setting means 14 connected with second comparator 20 is to adjust the center bias of the output signal from the control portion (12).

The inversion pulse inputted from the terminal (10) is amplified (or contracted) by the control signal from the control portion (12) by the circuit 11, and at the same time, the bias is also controlled. The control signal of the bias to be made by the amplification circuit (12) is made through the comparison by the feedback circuit (17) between a reference level set by the bias setting means (14) and a level of a signal from the low-pass filter (16). The amplifier of the circuit (11) is controlled so that the output of the voltage follower (18) may become normally constant. The capacitor C3 together with the resistor R6 is provided for smoothing.

The inversion pulse inputted into the common driver 39 is adapted to be added into the liquid crystal panel LCD, with the amplitude stabilized by the circuit of Fig. 3 and the bias being set.

The common driver circuit in accordance with the present invention is composed of a block circuit as shown in Fig. 2, and may be implemented as in the circuit diagram of Fig. 5, as a modified embodiment in addition to the circuit of Fig. 3. In the circuit shown in Fig. 5, the inversion pulse supplied to the input terminal (51) is inputted into the operational amplifier (52). The amplitude of the inputted inversion pulse is adjusted by the variable feedback resistor (53). The output of the amplifier (52) is inputted into the voltage follower (54) and is outputted as the common output. Also, the common bias is extracted by the low-pass filter composed of the resistor R17, and capacitor C12, and is inputted into the comparator (56). In the comparator (56), the level set by the comparator (57) and variable resistor (58) is compared with the above-described low-pass filter output level, and the comparator output is applied to the voltage follower (55) through the low-pass filter comprising the resistor R18 and capacitor C13. The output is applied to the amplifier (52) so that the output of the low-pass filter comprising the resistor R17 and the capacitor C12 may become normally a level set by the variable resistor (58) with the direct current as shown in Fig. 4(g).

The capacitor C11 of Fig. 5 is provided for the by-pass (especially at higher frequency) of the high frequency component. The capacitor C13 smooths the output of the comparator (56), which drops to the reference voltage (the output of comparator 57). The capacitor C14 provides protection against noise.

In Fig. 5, the common output is smoothed by the resistor R17, the capacitor C12, and is inputted into the comparator (56). Also, the bias set VR of the potentiometer (58) is established using both Vcc, Vee from the same power line as the source power voltage of the panel. The bias to be set by the potentiometer (58) sets the bias of the common output, and also, becomes a reference voltage of the direct current feedback, so that it may follow even the variation in the source power voltage. When the source power voltage has been varied, the variation in the voltage to be applied upon the panel becomes smaller because of the movement in accordance with the variation in the reference voltage. Since the circuits are all directly connected in construction, the capacitor for the direct current cutting use in not required. The modified example of Fig. 5 provides the same effect as that of Fig. 3, with the stability that the feedback resistor (53) is varied for amplitude adjustment.

As is clear from the foregoing description, the common driver circuit in accordance with the present invention is of simple construction comprising voltage follower, low-pass filter, feedback and control circuits. The variation in the direct current component which adversely affects signal processing of this type of circuit is inhibited so as to improve reliability. Also D.C. cutting at the front end of the output circuit for providing a common bias is not required, so that a large capacity direct current cutting capacitor becomes unnecessary.

## Claims

1. A driver circuit for driving a liquid crystal display (40) in accordance with supplied drive signals, the circuit comprising:

an output circuit (18;54) adapted for driving the liquid crystal display (40), feeding means (11;amp,$R_{15}$,53) for feeding the supplied drive signals to said output circuit (18;54) and setting means (14;58) for setting a desired DC bias level for the drive signals;

characterised by detecting means ($R_1$,$C_1$; $R_5$,$C_1$; $R_{17}$,$C_{12}$) for detecting the DC level of the signal output from the output circuit (18;54) and control means (12,13,14,17;56, $R_{18}$,55, $C_{13}$, $R_{19}$, 57, $C_{14}$, 58) for controlling the feeding means (11;amp,$R_{15}$,53) so as to adjust the said DC bias to said desired level in response to outputs of said setting means (14;58) and detecting means ($R_1$,$C_1$;$R_5$,$C_1$;$R_{17}$,$C_{12}$).

al amplifier 15 and a pair of transistors Q1, Q2 for buffer use. The feedback circuit 17 is composed of an amplifier 22 and a resistor R6.

The low-pass filter circuit 16 is composed of a resistor R1 and a capacitor C1, with the direct current component thereof being inputted into the amplifier 22 of the feedback circuit 17. The output of amplifier 22 is supplied to a first comparator 20 and a second comparator 21 of the control portion (12). The control portion 12 is composed of a first comparator 20, a second comparator 21, resistors R7,R8,R9,R10 and a capacitor C2. The amplitude varying means (13) associated with the first comparative 21 is to adjust the amplitude of the output signal from the control portion (12). The bias setting means 14 connected with second comparator 20 is to adjust the center bias of the output signal from the control portion (12).

The inversion pulse inputted from the terminal (10) is amplified (or contracted) by the control signal from the control portion (12) by the circuit 11, and at the same time, the bias is also controlled. The control signal of the bias to be made by the amplification circuit (12) is made through the comparison by the feedback circuit (17) between a reference level set by the bias setting means (14) and a level of a signal from the low-pass filter (16). The amplifier of the circuit (11) is controlled so that the output of the voltage follower (18) may become normally constant. The capacitor C3 together with the resistor R6 is provided for smoothing.

The inversion pulse inputted into the common driver 39 is adapted to be added into the liquid crystal panel LCD, with the amplitude stabilized by the circuit of Fig. 3 and the bias being set.

The common driver circuit in accordance with the present invention is composed of a block circuit as shown in Fig. 2, and may be implemented as in the circuit diagram of Fig. 5, as a modified embodiment in addition to the circuit of Fig. 3. In the circuit shown in Fig. 5, the inversion pulse supplied to the input terminal (51) is inputted into the operational amplifier (52). The amplitude of the inputted inversion pulse is adjusted by the variable feedback resistor (53). The output of the amplifier (52) is inputted into the voltage follower (54) and is outputted as the common output. Also, the common bias is extracted by the low-pass filter composed of the resistor R17, and capacitor C12, and is inputted into the comparator (56). In the comparator (56), the level set by the comparator (57) and variable resistor (58) is compared with the above-described low-pass filter output level, and the comparator output is applied to the voltage follower (55) through the low-pass filter comprising the resistor R18 and capacitor C13. The output is applied to the amplifier (52) so that the output of the low-pass filter comprising the resistor R17 and the capacitor C12 may become normally a level set by the variable resistor (58) with the direct current as shown in Fig. 4(g). The capacitor C11 of Fig. 5 is provided for the by-pass (especially at higher frequency) of the high frequency component. The capacitor C13 smooths the output of the comparator (56), which drops to the reference voltage (the output of comparator 57). The capacitor C14 provides protection against noise.

In Fig. 5, the common output is smoothed by the resistor R17, the capacitor C12, and is inputted into the comparator (56). Also, the bias set VR of the potentiometer (58) is established using both Vcc, Vee from the same power line as the source power voltage of the panel. The bias to be set by the potentiometer (58) sets the bias of the common output, and also, becomes a reference voltage of the direct current feedback, so that it may follow even the variation in the source power voltage. When the source power voltage has been varied, the variation in the voltage to be applied upon the panel becomes smaller because of the movement in accordance with the variation in the reference voltage. Since the circuits are all directly connected in construction, the capacitor for the direct current cutting use in not required. The modified example of Fig. 5 provides the same effect as that of Fig. 3, with the stability that the feedback resistor (53) is varied for amplitude adjustment.

As is clear from the foregoing description, the common driver circuit in accordance with the present invention is of simple construction comprising voltage follower, low-pass filter, feedback and control circuits. The variation in the direct current component which adversely affects signal processing of this type of circuit is inhibited so as to improve reliability. Also D.C. cutting at the front end of the output circuit for providing a common bias is not required, so that a large capacity direct current cutting capacitor becomes unnecessary.

## Claims

1. A driver circuit for driving a liquid crystal display (40) in accordance with supplied drive signals, the circuit comprising:

an output circuit (18;54) adapted for driving the liquid crystal display (40), feeding means (11;amp,$R_{16}$,53) for feeding the supplied drive signals to said output circuit (18;54) and setting means (14;58) for setting a desired DC bias level for the drive signals;

characterised by detecting means ($R_1$,$C_1$; $R_5$,$C_1$; $R_{17}$,$C_{12}$) for detecting the DC level of the signal output from the output circuit (18;54) and control means (12,13,14,17;56, $R_{18}$,55, $C_{13}$, $R_{19}$, 57, $C_{14}$, 58) for controlling the feeding means (11;amp,$R_{16}$,53) so as to adjust the said DC bias to said desired level in response to outputs of said setting means (14;58) and detecting means ($R_1$,$C_1$;$R_5$,$C_1$;$R_{17}$,$C_{12}$).



* C L M S *

2. A driver circuit according to claim 1 wherein said detecting means ($R_1$,$C_1$; $R_5$,$C_1$; $R_{17}$,$C_{12}$) is a low-pass filter.

3. A driver circuit according to claim 1 or claim 2 wherein said feeding means (11;amp,$R_{15}$,53) comprises an operational amplifier (19;52) receiving at a first input terminal thereof the supplied drive signals and at a second terminal thereof a control signal from said control means (12,13,14,17;56, $R_{18}$,55,$C_{13}$,$R_{19}$, 57, $C_{14}$,58).

4. A driver circuit according to any preceding claim wherein said output circuit (18;54) is a voltage follower circuit comprising an operational amplifier (15) and a buffer amplifier means ($Q_1$,$Q_2$; $Q_{11}$,$Q_{12}$), the output of said operational amplifier (15) being coupled to said detecting means ($R_1$,$C_1$;$R_5$,$C_1$; $R_{17}$,$C_{12}$).

5. A driver circuit according to any preceding claim, wherein said control means includes an amplitude controller (13) for adjusting the amplitude of the control signal supplied to the feeding means (11).

6. A driver circuit as claimed in any one of claims 1 to 4 wherein the feeding means (11;amp,$R_{15}$,53) includes means (53) for varying the amplitude of the output of said feeding means (11;amp,$R_{15}$, 53).

7. A driver circuit as claimed in any one of the preceding claims wherein said control means includes comparator means (22;56) for comparing the output of said detecting means ($R_1$,$C_1$;$R_5$,$C_1$; $R_{17}$,$C_{12}$) with the output of said setting means (14;58) and varying the control signals supplied to said feeding means (11;amp,$R_{15}$,53) in response thereto.

**Patentansprüche**

1. Treiberschaltung für eine Flüssigkristallanzeige (40) mit einer Ausgangsschaltung (18;54), welche die Flüssigkristallanzeige (40) mit Treibersignalen beaufschlagt, einer Zuführschaltung (11;amp,$R_{15}$,53), welche die Ausgangsschaltung (18;54) mit den bereitgestellten Treibersignalen versorgt, und einer Einstellschaltung (14;58) zur Vorgabe eines gewünschten DC-Biaspegels für die Treibersignale, **gekennzeichnet** durch eine Abtastschaltung ($R_1$,$C_1$;$R_5$,$C_1$;$R_{17}$,$C_{12}$), welche den DC-Pegel des Signal-Ausgangs der Ausgangsschaltung (18;54) prüft, und eine Steuereinrichtung (12,13,14,17;56,$R_{18}$,55,$C_{13}$,$R_{19}$,57, $C_{14}$,58) für die Zuführschaltung (11 ;amp,$R_{15}$,53), um den gewünschten Pegel des DC-Bias in Abhängigkeit vom Ausgang der Einstellschaltung (14;58) und der Abtastschaltung ($R_1$,$C_1$;$R_5$,$C_1$; $R_{17}$,$C_{12}$) vorzugeben.

2. Treiberschaltung nach Anspruch 1, bei der die Abtastschaltung ($R_1$,$C_1$;$R_5$,$C_1$; $R_{17}$,$C_{12}$) ein Tiefpaßfilter ist.

3. Treiberschaltung nach Anpruch 1 oder Anspruch 2, bei der die Zuführschaltung (11;amp,$R_{15}$,53) einen Operationsverstärker (19;52) umfaßt, der an einer ersten Eingangsanschlußstelle die bereitgestellten Treibersignale und an einer zweiten Anschlußstelle ein Steuersignal der Steuereinrichtung (12,13,14,17;56,$R_{18}$,55,$C_{13}$, $R_{19}$,57,$C_{14}$, 58) erhält.

4. Treiberschaltung nach einem der vorgenannten Ansprüche, bei der die Ausgangsschaltung (18;54) ein Spannungsfolger mit einem Operationsverstärker (15) und einem Pufferverstärker ($Q_1$,$Q_2$; $Q_{11}$,$Q_{12}$) ist, wobei der Ausgang des Operationsverstärkers (15) an die Abtastschaltung ($R_1$,$C_1$;$R_5$,$C_1$;$R_{17}$,$C_{12}$) gekoppelt ist.

5. Treiberschaltung nach einem der vorgenannten Ansprüche, bei der die Steuereinrichtung einen Amplitudenprüfer (13) beinhaltet, um die Amplitude des Steuersignals einzustellen, mit dem die Zuführschaltung (11) versorgt wird.

6. Treiberschaltung nach einem der Ansprüche 1 bis 4, bei der die Zuführschaltung (11;amp,$R_{15}$, 53) ein Mittel (53) umfaßt, das die Amplitude des Ausgangs der Zuführschaltung (11;amp,$R_{15}$ 53) verändert.

7. Treiberschaltung nach einem der vorgenannten Ansprüche, bei der die Steuereinrichtung einen Komparator (22;56) beinhaltet, der den Ausgang der Abtastschaltung ($R_1$,$C_1$;$R_5$,$C_1$;$R_{17}$,$C_{12}$) mit dem Ausgang der Einstellschaltung (14;58) vergleicht und die der Zuführschaltung (11;amp,$R_{15}$, 53) bereitgestellten Steuersignale abhängig davon verändert.

**Revendications**

1. Circuit de commande destiné à commander un affichage à cristaux liquides (40) en fonction de signaux de commande fournis, le circuit comprenant :

un circuit de sortie (18;54) adapté pour commander l'affichage à cristaux liquides (40), un moyen d'alimentation (11;amp, $R_{15}$, 53) destiné à délivrer les signaux de commande fournis



* C L M S *

audit circuit de sortie (18;54), et un moyen de réglage (14;58) destiné à régler un niveau de polarisation continue voulu pour les signaux de commande;

caractérisé par un moyen de détection ($R_1$, $C_1$; $R_5$, $C_1$; $R_{17}$, $C_{12}$) destiné à détecter le niveau de courant continu du signal de sortie provenant du circuit de sortie (18;54), et par un moyen de contrôle (12, 13, 14, 17; 56, $R_{18}$, 55, $C_{13}$, $R_{19}$, 57, $C_{14}$, 58) destiné à contrôler le moyen d'alimentation (11; amp, $R_{15}$, 53) afin d'ajuster ladite polarisation continue audit niveau voulu en réponse aux sorties dudit moyen de réglage (14; 58) et dudit moyen de détection ($R_1$, $C_1$; $R_5$, $C_1$; $R_{17}$, $C_{12}$).

2. Circuit de commande selon la revendication 1, dans lequel ledit moyen de détection ($R_1$, $C_1$; $R_5$, $C_1$; $R_{17}$, $C_{12}$) est un filtre passe-bas.

3. Circuit de commande selon la revendication 1 ou la revendication 2, dans lequel ledit moyen d'alimentation (11; amp, $R_{15}$, 53) comprend un amplificateur opérationnel (19; 52) qui reçoit, au niveau de sa première borne d'entrée, les signaux de commande fournis et, au niveau de sa seconde borne, un signal de contrôle provenant dudit moyen de contrôle (12, 13, 14, 17; 56, $R_{18}$, 55, $C_{13}$, $R_{19}$, 57, $C_{14}$, 58).

4. Circuit de commande selon l'une quelconque des revendications précédentes, dans lequel ledit circuit de sortie (18; 54) est un circuit suiveur de tension comprenant un amplificateur opérationnel (15) et un moyen amplificateur séparateur($Q_1$, $Q_2$; $Q_{11}$, $Q_{12}$), la sortie dudit amplificateur opérationnel (15) étant reliée audit moyen de détection ($R_1$, $C_1$; $R_5$, $C_1$; $R_{17}$, $C_{12}$).

5. Circuit de commande selon l'une quelconque des revendications précédentes dans lequel ledit moyen de contrôle comprend un organe de contrôle d'amplitude (13) destiné à ajuster l'amplitude du signal de contrôle fourni au moyen d'alimentation (11).

6. Circuit de commande tel que défini dans l'une quelconque des revendications 1 à 4, dans lequel le moyen d'alimentation (11; amp, $R_{15}$, 53) comprend un moyen (53) destiné à faire varier l'amplitude de la sortie dudit moyen d'alimentation (11; amp, $R_{15}$, 53).

7. Circuit de commande tel que défini dans l'une quelconque des revendications précédentes, dans lequel ledit moyen de contrôle comprend un moyen comparateur (22; 56) destiné à comparer la sortie dudit moyen de détection ($R_1$, $C_1$; $R_5$, $C_1$; $R_{17}$, $C_{12}$) avec la sortie dudit moyen de réglage (14; 58) et à faire varier les signaux de contrôle fournis audit moyen d'alimentation (11; amp, $R_{15}$, 53) en réponse à cette comparaison.



* C L M S *