

"CONTROL CIRCUITS FOR PHASE LOCKED LOOPS"

This invention relates to a control circuit for phase locked loops, and particularly to a bandwidth control circuit for phase locked loops used in a frequency synthesizer.

5 Phase locked loops are used in frequency synthesizers to provide a relatively wide range of selectable frequencies having the stability of a reference oscillator which is typically crystal controlled. Such a wide frequency range requires
10 that the filter in the phase locked loop have a variable bandwidth so that when a frequency change is programmed or required, such a change can be made in a small amount of time. The rate of change depends on the loop control voltage, which in
15 turn is limited first by the amount of loop gain available. Second, the loop control voltage is further limited when a relatively low cutoff frequency filter is inserted into the phase locked loop control line to reduce noise and frequency
20 modulation of the voltage controlled oscillator by the reference frequency. In prior art circuits, most filter switching in a phase locked loop has been accomplished by using a fixed timing circuit (such as a one shot multivibrator) which initially
25 allows locking with a relatively high filter bandwidth. After the timing circuit times out, it switches the filter to a relatively low bandwidth. However, there are several problems associated with such a timing circuit. First,
30 if for some reason the voltage controlled oscillator goes out of lock because of a noise burst or pulse from the power supply voltage, the normal lock

detector might not detect the loss of lock for many milliseconds, so that a transmitter whose frequency source is the voltage controlled oscillator might produce a carrier or high level noise over a good portion of the adjacent frequency spectrum. The second problem is that the fixed time allowed for the voltage controlled oscillator to settle to the new commanded frequency may not be long enough for the particular frequency change involved. When the bandwidth is reduced after this fixed time but before the transmitter has settled to the commanded frequency, the transmitter may produce undesired frequencies with associated interference until its frequency is correct.

From an ideal standpoint, relatively fast and wide frequency changes should be made with a relatively wide bandwidth filter circuit in the phase locked loop. After the voltage controlled oscillator produces the new commanded frequency, the filter circuit should provide a relatively narrow bandwidth.

The present invention provides an improved circuit for controlling the bandwidth of a filter in a phase locked loop. The circuit uses the phase detector output signal and produces both a relatively high signal and a relatively low signal from the phase detector output signal. The low signal is compared in a first comparator with the high signal as delayed by a charging circuit; and the high signal is compared in a second comparator with the low signal as delayed by a charging circuit. For increases in the phase detector output, the first comparator produces an output in response to a relatively low signal exceeding the high signal until the high signal charging circuit delay ends.

For decreases in the phase detector output, the second comparator produces an output in response to a relatively low signal exceeding the high signal until the low signal charging circuit delay ends.

5 The comparator outputs are combined so that a circuit output is produced in response to and for a duration related to either of the comparator outputs, which in turn are related to the magnitude of the output signals from the phase detector. When
10 present, the circuit output can be used to provide a wide bandwidth filter. At the end of the circuit output, the filter bandwidth can be decreased.

By way of example only, an embodiment of the invention is illustrated in the accompanying drawings,
15 in which:

Figure 1 is a block diagram of a frequency synthesizer having a phase locked loop and a control circuit embodying the invention;

20 Figure 2 is a schematic circuit diagram of the control circuit; and

Figure 3 shows waveforms illustrating the operation of the control circuit of Figure 2.

Referring first to the block diagram of Figure 1, this shows a control circuit embodying the
25 invention used with a known frequency synthesizer having a phase locked loop. As known in the art, such a synthesizer may comprise a stable reference oscillator 10 which is normally crystal controlled. The frequency of this oscillator may, if desired, be
30 multiplied up or divided down in frequency after which its output is applied to a first input of a phase detector 11. The output of the phase detector 11 is applied through a filter circuit 12 to the input of a voltage controlled oscillator 13. The output
35 of the oscillator 13 is derived for any suitable use,

such as a radio transmitter or receiver. The output of the oscillator 13 may be divided down in frequency or multiplied up in frequency, depending upon the circuit requirements. In the example shown in Figure 1, it is assumed that the output of the oscillator 13 is divided down in frequency by a divider 14 and applied to a second input of the phase detector 11. As known in the art, a channel selector 15 may be connected to the divider 14 to change the divisor applied to the output signals from the oscillator 13, and thus change the output from the oscillator 13 as provided by the phase locked loop.

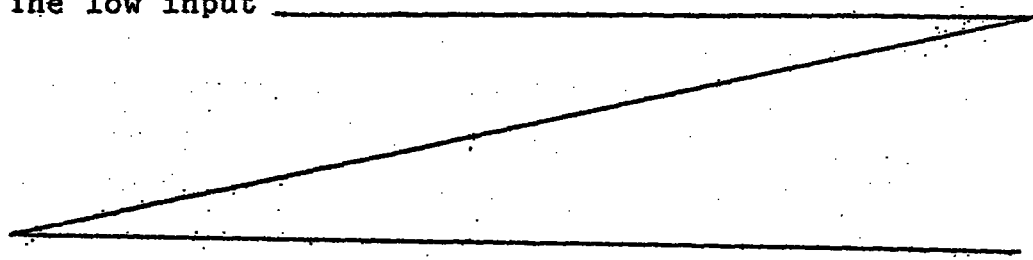
The circuit as described thus far is known in the art. As mentioned earlier, if the channel selector 15 is switched rapidly or causes the divider 14 to change the divisor by a relatively large magnitude, the phase locked loop may require considerable time in order to achieve lock and cause the voltage controlled oscillator 13 to produce the new desired output frequency. This is particularly true if the filter 12 has a relatively narrow bandwidth, a condition normally required to reduce noise or spurious radiations from the oscillator 13. And during the time that the phase locked loop is out of lock, the oscillator 13 may and frequently does produce undesired and widely varying output frequencies. In order to reduce these undesired effects a control circuit 20 receives an output from the phase detector 11 and supplies this output to the filter 12 to cause the filter 12 to switch bandwidths. As will be explained in detail, control circuit 20 produces a first output in response to a relatively low output from the phase detector 11. The first output may be used to cause the filter 12 to have a relatively

16

narrow bandwidth, and hence reduce noise and other undesired radiations from the oscillator 13. The control circuit 20 produces a second output in response to a relatively high output from the phase detector 11 until this high output decreases to the previously mentioned low output. The second output from control circuit 20 may be used to cause the filter 12 to have a relatively wide bandwidth, and thus permit rapid lock of the phase locked loop to be obtained. Control circuit 20 may also be supplied with a frequency change signal which may be derived from the channel selector 15, and with an out-of-lock signal which may be derived from the phase detector 11. These signals permit control circuit 20 to produce the second output signal which may be used to cause the filter 12 to have a wide bandwidth. An output may also be derived from control circuit 20 for application to a transmitter and/or receiver for momentarily cutting these devices off during the time the second output is produced.

Figure 2 is a schematic circuit diagram of control circuit 20. Signals from the phase detector 11 are applied to a voltage divider comprised of resistors R1, R2 connected in series between an input terminal 22 and a point of reference potential, such as ground. This voltage divider causes the phase detector signal to have a relatively high input at the terminal H, and a relatively low input at the terminal L. The high input terminal H is coupled through a resistor R4 to the minus input of an operational amplifier A1 connected as a comparator circuit, and through a resistor R6 to the minus input of an operational amplifier A2 also connected as a comparator circuit. The low input

35



terminal L is coupled through a resistor R3 to the plus input of the amplifier A1, and through a resistor R5 to the plus input of the amplifier A2. A time delay circuit comprising a capacitor C1 is connected between the minus input of the amplifier A1 and ground, and a time delay circuit comprising a capacitor C2 is connected between the plus input of the amplifier A2 and ground. These delay circuits provide a time delay for reasons that will be explained. The outputs of the amplifiers A1, A2 are coupled through isolating diodes D1, D2 to a common output bus 21. The output bus 21 is coupled through an isolating diode D3 to the minus input of an operational amplifier A3 connected as a comparator circuit, and through an isolating diode D4 to the plus input of an operational amplifier A4 also connected as a comparator circuit. A voltage reference circuit is provided by resistors R10, R11 connected in series between a voltage B+ and ground. The plus input of the amplifier A3 and the minus input of the amplifier A4 are connected to the junction of the resistors R10, R11. Also, a filter circuit comprising a resistor R8 and a capacitor C3 is connected between the minus input of the amplifier A3 and ground, and a filter circuit comprising a resistor R9 and capacitor C4 is coupled between the plus input of the amplifier A4 and ground. And finally, the out-of-lock signal is connected through a diode D5 to the common output bus 21, and the frequency change signal is coupled through an isolating diode D6 to the common output bus 21.

The output of the amplifier A3 can be applied to

the transmitter and/or receiver for cutting these devices off, and the output of the amplifier A4 can be connected to the filter 12 for changing its characteristics. The outputs of the amplifiers A1, A2 are
5 applied to the minus terminal of the amplifier A3 and the plus terminal of the amplifier A4. Normally, the amplifier A3 produces an output because its plus terminal is supplied with a positive voltage by the resistor R10. Thus, elimination of the output of the
10 amplifier A3 can be used to cut off either the radio transmitter or the radio receiver, or both if desired. Normally, the amplifier A4 produces no output because its minus terminal is supplied with a positive voltage by the resistor R10. When the amplifier A4 produces no
15 output, this can be used to cause the filter 12 to have a relatively narrow bandwidth. However, when the amplifier A4 produces an output, this can be used to cause the filter 12 to have a relatively wide bandwidth. Such bandwidth can be accomplished in any number of
20 known ways, such as supplying or eliminating capacitors from the filter circuit.

The operation of the circuit of FIGURE 2 will be explained in connection with the waveforms plotted along a common time axis in FIGURE 3. FIGURE 3A shows the
25 input signal applied to my circuit from the phase detector 11. FIGURE 3B shows the inputs applied to the amplifier A1, the dashed line representing the input to the minus terminal and the solid line representing the input to the plus terminal. FIGURE 3C shows the inputs
30 applied to the amplifier A2, the dashed line repre-

senting the input to the minus input, and the solid line representing the input to the plus input. FIGURE 3D shows the output of the amplifier A1, and FIGURE 3E shows the output of the amplifier A2.

5 Prior to the time T1, it is assumed that the input to the circuit as shown in FIGURE 3A is at its stable or normal value. With this normal input, the minus
10 terminal input of the amplifier A1 exceeds the plus terminal input of the amplifier A1 so that the amplifier A1 produces no output. Likewise, the minus terminal
15 input of the amplifier A2 exceeds the plus terminal input of the amplifier A2 so that the amplifier A2 produces no output. With no outputs from the amplifiers A1, A2, and with no out-of-lock and frequency change
20 signals, the amplifier A3 provides an output that can be used to keep a transmitter and/or receiver turned on; and the amplifier A4 provides no output that can be used to cause the filter 12 to have a narrow bandwidth. At
25 the time T1, we assume that the input rises by a relatively small magnitude in response to a phase difference of the reference and controlled oscillator signals. This causes the plus terminal of the amplifier A1 and the minus terminal of the amplifier A2 to
30 increase in the same manner. The minus terminal of the amplifier A1 and the plus terminal of the amplifier A2 also increase, but more slowly because the capacitors C1, C2 must be charged. But because of the small rise in the input, the minus terminal of the amplifier A1 stays above its plus terminal. The minus terminal of the amplifier A2 clearly stays above its plus terminal.

As a result, neither amplifier produces an output at the time T1 as shown in FIGURES 3D and 3E. At the time T2, the input falls to its initial and stable value. The plus terminal of the amplifier A1 and the minus terminal of the amplifier A2 decrease similarly, while the minus terminal of the amplifier A1 and the plus terminal of the amplifier A2 decrease slowly because the capacitors C1, C2 must discharge. However, because of the small decrease, the minus terminals stay above the respective plus terminals so that no amplifier outputs are produced.

At the time T3, we assume that the input decreases a small amount below its normal value. This causes the amplifier terminals to decrease in the manner described at the time T2. In this case, the minus terminals continue to remain above the respective plus terminals, so that no amplifier outputs are produced. At the time T4, we assume that the input rises up to its normal or stable value again. This causes the inputs to the amplifiers A1, A2 to follow a similar variation as described for the time T1. Again, no amplifier outputs are produced.

However, at the time T5, we assume that the input increases by a relatively large amount, at least above a threshold set by the circuit values. Such a large increase would reflect a large phase difference between the reference and controlled oscillator signals. This causes the plus terminal of the amplifier A1 to rise above the minus terminal of the amplifier A1 because an increase of the minus terminal is delayed by the

capacitor C1 having to charge. During the time required for the capacitor C1 to become charged and the minus terminal can exceed the plus terminal of the amplifier A1, the amplifier A1 produces a plus output at the time T5 as shown in FIGURE 3D. However, the amplifier A2 produces no output because the minus input exceeds the plus input as shown in FIGURE 3C. This output from the amplifier A1 causes the amplifier A3 to produce an output that could turn the transmitter and receiver off; and causes the amplifier A4 to produce an output that causes the filter 12 to have a wide bandwidth.

At the time T6, we assume that the input decreases rapidly to its normal value as shown in FIGURE 3A. The amplifier A1 produces no output, as the plus terminal remains below the minus terminal. However, the minus terminal of the amplifier A2 decreases rapidly below the plus terminal, because the plus terminal must discharge through the capacitor C2. During this discharge time, the amplifier A2 produces an output as shown in FIGURE 3E. This output from the amplifier A2 causes the amplifier A3 to produce an output that could turn the transmitter and receiver off; and causes the amplifier A4 to produce an output that causes the filter 12 to have a wide bandwidth.

At the time T7, we assume that the input decreases rapidly to a lower value as shown in FIGURE 3A. This causes the amplifier A2 to produce an output at the time T7 in the same manner described for the operation at the time T6. Because the magnitude of the decrease at the time T7 is greater than the magnitude of the decrease at

(22)

the time T6, the time delay is greater, and the duration of the output at the time T7 is greater than the duration of the output at the time T6.

And finally, at the time T8, we assume that the
5 input rises rapidly to its normal value as shown in
FIGURE 3A. This causes the amplifier A1 to produce an
output and the amplifier A2 to produce no output as
described for the operation at the time T5. Because the
magnitude of the increase at the time T8 is greater than
10 the magnitude of the increase at the time T5, the time
delay is greater, and the duration of the output at the
time T8 is greater than the duration of the output at
the time T5.

While other input changes would cause other dura-
15 tions of outputs, persons skilled in the art will
understand the operation of the circuit from the examples
given and explained in connection with FIGURE 3.

The out-of-lock and frequency change signals
applied through the isolating diodes D5, D6 can also be
20 applied to the minus terminal of the amplifier A3 and
the plus terminal of the amplifier A4 to achieve the
same functions as outputs from the amplifiers A1, A2.
Thus, an out of lock signal or a frequency change signal
could cause the amplifier A3 to eliminate its output and
25 cause the amplifier A4 to provide an output for the
functions described previously.

It will thus be seen that we have provided a new and
improved control circuit for use in a phase locked loop
for the purpose of providing a control signal which has
30 a duration dependent upon the magnitude of change of the

phase detector input signal. While we have described only one embodiment of the invention, persons skilled in the art will appreciate the modifications that may be made. For example, the comparator circuits provided by the amplifiers A1, A2, A3, A4 may take many forms, although we prefer operational amplifiers. Also, delay circuits provided by the capacitors C1, C2 may take other forms, and provide time delays dependent upon circuit requirements.

CLAIMS

1. A control circuit for a phase locked loop having a reference oscillator, a controlled oscillator, a phase detector having inputs coupled to the oscillators, and a filter coupled between an output
5 of the phase detector and a control input of the controlled oscillator, the control circuit comprising:

first and second comparator circuits each having a first input connected to receive a relatively low voltage signal and a second input connected to
10 receive a relatively high voltage signal in response to a voltage at the phase detector output;

a pair of delay circuits respectively coupled to the second input of the first comparator and to the first input of the second comparator such that
15 the increase in the relatively high voltage at the second input of the first comparator in response to an increase in the phase detector output voltage and the decrease in the relatively low voltage at the first input of the second comparator in response
20 to a decrease in the phase detector output voltage are respectively delayed relative to the corresponding change in voltage at the other input such that, when the respective increase or decrease in voltage exceeds a predetermined value, the polarity of the voltages
25 at the first and second inputs of the respective comparators reverses for a predetermined period dependent on the magnitude of the increase or decrease in voltage;

and output means responsive to the said reversal
30 of polarity for providing an output signal to increase the bandwidth of the filter.

2. The control circuit of claim 1 wherein the output means include a comparator circuit having a first input coupled to the outputs of the first and second
35 comparator circuits, and having a second input coupled



to a reference voltage.

3. The control circuit of claim 1 or claim 2 and further comprising an input circuit providing an additional control signal to the output means.

5 4. The control circuit of claim 1 or claim 2 wherein each of the delay circuits comprise a capacitor charging circuit.

5. A phase locked loop control circuit comprising:
10 a voltage divider circuit for receiving a phase detector output signal;

first and second comparator circuits each having a first input connected to receive a relatively low voltage signal from the voltage divider and a second input connected to receive a relatively high
15 voltage signal from the voltage divider;

a pair of time delay circuits respectively coupled to the second input of the first comparator and to the first input of the second comparator such that the increase in the relatively high voltage signal
20 at the second input of the first comparator in response to an increase in the phase detector output voltage and the decrease in the relatively low voltage at the first input of the second comparator in response to a decrease in the phase detector output voltage are
25 respectively delayed relative to the corresponding change in voltage at the other input such that, when the respective increase or decrease in voltage exceeds a predetermined value, the polarity of the voltages at the first and second inputs of the respective
30 comparators reverses for a predetermined period dependent on the magnitude of the increase or decrease in voltage, and output means responsive to the said reversal of polarity for providing an output signal to increase the bandwidth of the filter.

35 6. The control circuit of claim 5 wherein the



comparator circuits comprise operational amplifiers.

7. The control circuit of claim 5 or claim 6 wherein the output means comprise a threshold circuit that produces an output in response to either of the
5 comparator circuit outputs exceeding a selected magnitude.

8. The control circuit of claim 5, 6 or 7 wherein the time delay circuits introduce a time delay to changes in signal level, the time delay being related
10 to the magnitude of the changes in signal level.

9. A control circuit for a phase locked loop, the circuit being substantially as herein described with reference to the accompanying drawings.

15

20

25

30

35

