Description

The invention relates to an error correction method for the transfer of word-wise arranged data, comprising the following steps:

a. receiving a succession of first numbers of data words in a first error encoder and adding to each first number of data words a first series of parity words on the basis of a first generator matrix of a first word correction code;

b. interleaving said first numbers of data words and first series of parity words by means of respective delay times which are all different within each first number and associated first series in order to form a succession of second numbers of words, each second number of words having a number of data words equal to said first number plus a number of check words equal to the number in a first series;

c. receiving a second number of words of said succession in a second error encoder and adding to said second number of words a second series of parity words on the basis of a second generator matrix of a second word correction code so as to form a third number of words:

d. word-by-word modulation of serially linked said third numbers of words in order to form channel words which satisfy, by way of added redundancy, predetermined upper limits and lower limits for the admissible intervals between directly successive signal transitions, said channel words being serially concatenated and pair-wise separated by merging bits which in combination with the channel words also satisfy said upper limits and lower limits in conjunction therewith;

e. demodulation of the channel words and merging bits after the transfer in order to reconstruct said third number of words;

f. receiving said third numbers of words, and from each third number reproducing, and if possible and necessary, correcting said second numbers of words, on the basis of the second parity check matrix associated with the second generator matrix;

g. de-interleaving said second numbers of words, followed by the reproducing therefrom, and if possible and necessary, correcting said first numbers of data words for a user on the basis of the first parity check matrix associated with the first generator matrix.

Part of a transfer with error correction is known from GB—A—2079993 (and BE—A—889322, published 16.10.81). According to prior art, within a second number of words, or within a third number of words, respective limited numbers of words can thus be corrected or a further limited number of words can be detected as being incorrect, said limited numbers being given by the minimum Hamming distance of the code taken over the words or symbols. This capability will be described in detail hereinafter. If the number of incorrect words within a second or third number of words is larger than the relevant admissible value, the error correction or the detection of incorrect words fails. When the error correction fails, either incorrect words are not corrected or words are incorrectly corrected, or both. If the error detection fails, either words are indicated as being incorrect or incorrect words are not indicated as being incorrect, or both. For completeness' sake it is mentioned that prior art includes further interleaving steps before the first error encoding and between the second error encoding and the modulation. Furthermore, the modulation and demodulation has been described in British Patent Application 2083322 published March 17, 1982. The modulation is a kind of coding for realizing a run-length-limited code; the transitions in the signal value are transitions from a channel bit having a first signal value to a channel bit having the second signal value. It is an object of the invention to combine the redundancy introduced into the data transferred by the described modulation with the error correction codes proper, in order to enhance the overall error correction capability. Incorrectly demodulated words should function as indicators for a generally unreliable second number of words.

A first version of the method in accordance with the invention utilizes this principle and is characterized in that during the demodulation a first flag bit is added to the word of said third number of words which is formed from an unrecognizable channel word, wherein before the reproduction of a said second number of words on the basis of the second parity check matrix under the control of an excessive number of first flag bits within a said third number any error locator calculations associated to said second parity check matrix are omitted and a second flag bit is added to each word of the relevant second number of words in order to indicate this number of words as being generally unreliable.

The invention is based on the recognition of the fact that during the transfer (via a broadcast channel, a communication link or a storage medium such as an optical storage disc or a magnetic tape), usually trains of disturbed channel words or burst errors occur which can impart an arbitrary content to a channel word. In such a case the result may be again a correct channel word. The invention is also based on the recognition of the fact that it is attractive to detect the error as soon as possible, that is to say before the first error correction. The redundancy introduced during modulation makes such detection possible. In the case described a limited number of words could be corrected. If more words are indicated as being incorrect, the correction is omitted in order to allow it to be performed, for example, only after de-interleaving. Thanks to the de-interleaving, a number of words which are indicated as being unreliable are spaced further apart, so that the local concentrations of incorrect words is reduced in many cases. A further aspect of the foregoing is that the indication of incorrect channel words makes correction of a larger number of words possible: the method, for

example, is capable of correcting four words localized as being incorrect. For safety reasons correction may still be undertaken in the case of three channel words indicated as being incorrect, but in the case of four incorrect channel words (which themselves are correctable) the second number of words is preferably indicated as being unreliable.

Further advantageous aspects are recited in the dependent Claims.

Brief description of the Figures

The invention will be described in detail hereinafter with reference to some Figures.

Figure 1 is a diagram of a preferred configuration of the channel words,

Figure 2 shows a preferred parity check matrix (H),

Figure 3 is a block diagram of a decoder for use in accordance with the invention,

Figure 4 shows a flow chart relating to the second error correction code, and

Figure 5 show a flow chart relating to the first error correction code.

Description of a preferred embodiment

Figure 1 shows a preferred configuration in which the channel words are presented; the channel words are organized in blocks, one of which is shown. After the beginning at the indication 62, first a synchronization word A (66) is presented and subsequently a control word "0" (68). The further channel words are formed by means of systematic error correction codes in such manner that there are 24 non-redundant channel words (1—24), as indicated by the indication 70, and eight parity channel words which are each indicated by a cross, for example the channel word 72. The block terminates at the indication 64. The meandering line 74 indicates the time sequence. Actually, all channel words indicated directly succeed one another, be it that they are followed each time by three merging bits. With the exception of the synchronization word 66, each channel word consists of fourteen channel bits. The number of directly successive channels bits of the same value is not smaller than three and not larger then eleven. It has been found that this results in 267 feasible combinations, 256 of which are used to represent respective 8-bit code words, the remaining eleven either not being used or being used for special purposes. The merging bits within the chain of channel words also satisfy the upper limits and lower limits imposed as regards the number of directly successive channel bits having mutually the same binary values.

Figure 2 shows a parity check matrix (H) of a word correction code to be used. The generator matrix (G) of this code is given in that the matrix product $(G) \cdot (H)=0$. The number of columns of the matrix (H) equals the number of code words to be processed together. The number of rows of the matrix (H) equals the number of redundancy words included in the code words. It has previously been proposed to supplement a number of 24 data words with four redundancy words in a first error correction code in order to obtain 28 words. Subsequently, these groups of 28 words are interleaved in order to form as many second groups of words (also 28). Finally, four further redundancy words are added to said second numbers of words in a second error correction code in order to form a third number of words which words then are modulated in order to form as many channel words. For the first error correction code the number of columns of the parity check matrix then equals 28; for the second error correction code said number of columns equals 32. In both cases the number of rows of the matrix (H) equals four. The elements $a^0=1$, a^1 ... of the matrix (H) are elements of a Galois field $GF(2^m)$ which are generated by the associated primitive and irreducible generator pelynomial. The number of bits of the relevant words is m, for which $n \leq 2^{m-1}$; in the present embodiment $m=8$. By addition of four redundant code words a minimum Hamming distance over the code words of five can be realized. Two incorrect code words can thus be corrected, without it being necessary to know which code words are incorrect. The redundancy offered by the four redundant words is then sufficient to represent the error vector (the error pattern) as well as the error locator for both words. When the error locator is known, knowing the error vector alone may be sufficient for correction of said incorrect word. When four words are incorrect whose error locator has been obtained in a different manner, a number of four redundant words suffices for the correction of those four incorrect words. If the error locator of two words is known, four redundant words are sufficient for correction of the relevant two words and also for localizing and correcting an incorrect word whose location need not be known. The same code is also capable of detecting four incorrect words. The sum of the number of incorrect words to be detected plus the sum of the number of incorrect words to be corrected whose location has become known in a different manner therefore equals four. For other codes built up in accordance with the restrictions described and involving different numbers of redundant words, corresponding numbers of detectable/correctable incorrect words are applicable.

Figure 3 shows a decoder for use with the invention. It is to be noted that the invention can be used in an encoder as described in U.S. Patent 4413 340 which encoder, therefore, will not be elaborated upon herein. In the set-up shown in Figure 3, the information of the channel words arrives on the input 30 in a bit serial manner. In the demodulator 32, first a series/parallel conversion takes place, so that a complete code word becomes available on the fourteen-fold connection 40. The actual series/parallel converter and the clock system required have been omitted for the sake of simplicity. Block 34 represents a translator which converts a correctly received

fourteen-bit channel word into the corresponding 8-bit code word on the 8-fold connection 38 plus a binary "zero" on the single connection 36. Several possibilities exist when the channel word is not correct: first of all, an arbitrary word, for example "00000000", may be produced on the connection 38 and a logic "1" on the connection 36. Alternatively, the incorrect channel word may be translated into a correct channel word which corresponds as well as possible thereto and which is translated into the corresopnding code word (obviously, this can be performed in one operation). Usually, a single-bit error in a channel word can be repaired; in cases where several code words can be formed with the same probability (the same Hamming distance between incorrect channel word and several correct channel words), one of these correction code words is chosen as a substitute in accordance with the foregoing. Multibit errors generally cannot be corrected in all cases. The translation of a correct channel word into the corresponding 8-bit demodulated word is subsequently performed; this translation may also be implicit, so that the demodulation is performed in a single stroke. Each time a channel word received is detected as being incorrect, the connection 36 carries a logic flag bit"1". It is alternatively possible to construct the line 36 to be multiple in order to indicate whether a channel word received was correct, or whether unambiguous correction was possible, or whether a substitute word has been chosen from several possible substitutes. In many cases an error is accompanied by further errors in neighbouring code bits; this phenomenon is referred to as a burst error. Bit-wise correction of the code bits is then often impossible, and the bit on the connection 36 has the significance valid/invalid. A "valid" code word, therefore, may very well be incorrect. In that case an 8-bit demodulated word appears serially or in parallel on the output 42 of the demodulator 32 in conjunction with at least one flag bit or validity bit. The block 34 may be constructed as a read-only memory with an address input having a width of 14 bits and an output data path having a width of 9 bits (or possibly more bits). The merging bits are ignored for the conversion code bits. If desired, the merging bits may be taken into account for the formation of the valid/invalid bit, because they must also satisfy the modulation restriction. The merging bits may then be considered as forming part of the directly preceding channel word. The control word (68 in Figure 1) is also presented to the input 30 as a 14-bit channel word (with merging bits), so that it can also be provided, if desired, with a valid/invalid bit. The synchronization word 66 and also the control word 68, however, are ignored for the error correction of the other words. Connections 36, 38 may have branchings off for forwarding the control words to a control device, but these elements have not been shown for brevity. Among themselves, the control words may be part of an error correcting code. The valid/invalid flag bit for the demodulated control word may be used in similar ways as the corresponding flag bits for the data are used, to be described hereinafter.

Most of the decoder is known from said state of the art. Block 44 represents a multiplexer which comprises one input 42 and thirty-two parallel outputs. Multiplexing is performed word-wise, so that each output receives one complete word, including the associated validity bit (bits). Blocks which are indicated by the numeral "1", for example the block 46, delay the words applied thereto by a time which corresponds to the period during which exactly 32 words, including the associated validity bit (bits), arrive on the connection 42. Elements such as the element 48 are invertors whereby the parity words of the second error correction code are bitwise inverted. Element 50 is the reproduction and correction element for the second error correction code for implementing the parity check matrix (with n=32) which is shown in Figure 2. Without using the validity bits, two incorrectly received words can be corrected. The processing of the data within the element 50 will be described with reference to a flow chart. Thus, for every 32 words received from the element 44, twenty-eight 8-bit output words arrive on the output of the reproduction and correction element 50, each output word being accompanied by its own validity bit. A logic "0" indicates that the relevant word is reliable; a logic "1" indicates that the relevant word is unreliable. In given cases (see hereinafter), the entire group of 28 words is indicated as being generally unreliable, because all 28 words have a validity bit of the value "1". The data rate on the output (outputs) of the element 50, therefore, amounts to 28/32=7/8 times the word rate on the corresponding input (inputs) of the element 50. The blocks 52 which are denoted by the reference numerals 1 to 27 delay the words received in order to introduce a de-interleaving effect. A "1" in a block indicates a delay which corresponds to the period of time required for the outputting of exactly one group of 28 words by the element 50. An indication "14" indicates a period of time which corresponds to the outputting of fourteen of such successive groups. Each word of a group of 28 words outputted together by the element 50 is thus assigned to a relevant newly formed group of 28 words. The effect of a burst error is thus spread over a large time interval, so that it is ensured that generally each newly formed group of 28 words contains at the most a small number of incorrect words.

Element 54 is the reproduction and correction element for the first error correction code for implementing the parity check matrix (with n=28) which also corresponds to Figure 2. Without using the validity bits, for K redundant words a number K/2 (when K is even; in this case K=4) of incorrect words received can be corrected. The data processing mechanism in the element 54 will be described hereinafter with reference to a flow chart. Thus, on the output of the reproduction and correction element 54 twenty-four 8-bit data

words appear for each group of 28 (interleaved) input words, said data words being accompanied or not by a validity bit having the significance previously described. In some cases (see hereinafter) the entire group of 24 words is indicated as being generally unreliable, because all 24 words comprise a relevant validity bit having the value "1". The data rate on the output of the element 54, therefore, amounts to 24/32=3/4 times the word rate on the input of the element 50. Blocks which are indicated by a digit "2", for example the block 56, delay the words applied thereto by a time which corresponds to the period during which exactly 2×32 words, including the associated validity bit (bits) arrive on the connection 42. Block 58 is a parallel/series converter for presenting 24 words received in the correct sequence (i.e. inverted with respect to the series/parallel conversion between the input 30 and the connection 40) on the output 60 to a user device which is not shown. Thirty-two data bits (i.e. four data words) may form exactly one audio sample signal for stereo reproduction. Alternatively, the data words may represent computer programs, ASCII characters or other information for use in a professional, data processing, or consumer environments. Referring to the first audio definition, should one of the four data words be invalid, either the entire audio signal or a mono portion thereof may be declared invalid and be replaced by an interpolated signal which is derived from one or more neighbouring audio signals. This is not elaborated upon in Figure 3.

Figure 4 shows the processing of the data in the reproduction and correction element 50. The Figure is in the form of a flow chart and concerns a preferred embodiment. When a group of 32 words has been received, the processing may commence (block 100). In block 102 it is detected whether the number of invalid code words amounts to zero. If yes (Y), the multiplication by the parity check matrix is performed in block 104 in order to determine the syndrome variable. The syndrome variable (SYN) indicates whether the number of incorrect words amounts to 0, 1, 2 or more than two; if the number of incorrect words amounts to more than two, often a wrong number will be indicated. If the number of words indicated by the syndrome amounts to 0 or 1, the system proceeds to the block 106 in which the single incorrect word is corrected or a dummy error correction is performed in a conventional manner. If the number f of invalid code words amounts to one, first block 108 is reached, via block 102, and subsequently block 110. The operation in block 110 is the same as that in block 104. If it is detected in block 110 that one word is incorrect, the system goes to the block 106 (the case of zero incorrect words cannot occur unless, as previously described, the redundancy in the channel word has been used to correct a 1-bit error in a channel word) and the real or dummy correction is performed. If it is detected in the block 110 that there were two incorrect words, it is detected in block 112 whether one of the two error locators indicates the (one) invalid word. If this is so (Y), the system proceeds to the block 106 in order to perofrm the correction. If the invalid word is not indicated, correction is not possible and the system proceeds to block 114; this also takes place in the case of a negative (N) test result in the block 104. In the block 114, the validity bits of all words of the relevant group of words are set to "invalid". In block 112 a test for the detection of more than two incorrect words can be implicitly incorporated; this result again leads to the block 114. If the number of invalid words amounts to three or more, the system proceeds to the block 114 via the blocks 102, 108, 116 in order to declare all words of the group generally invalid. If in block 116 the number of invalid words amounts to exactly two, the relevant bits are used as error locators: using these error locators, the correction is performed in block 118. The syndrome may indicate that more than two words are incorrect, so that correction is not possible; in that case the system may proceed to the block 114, but this step is not shown separately. The outputs of the blocks 106, 114 and 118 lead to block 120. This block indicates that the next group of 32 code words must be loaded, because the error correction and reproduction of the 28 output words has been completed. The block 120 also comprises a "stop" output (not shown separately) for the case where no further words are received.

The formation of the syndrome variables in the blocks 104, 110 can be performed in known manner by multiplication of the 32 code words by the parity check matrix (H) previously described. The correction is now possible because the syndrome consists of four syndrome words. This result can be considered as four equations to be formed for producing four unknown variables when solved. These variables may be two error locators and two error vectors; two arbitrary words can thus be corrected. When a word is indicated as being invalid and this indication is accepted as an error locator variable, one additional (linear) equation is effectively formed, so that more unknowns could also be resolved (including the locator which is given by the invalidity bit).

The set-up of the block diagram of Figure 4 may be modified. First of all, the case of f=2 (block 116) can be treated in the same manner as the case f=1 (block 108). Secondly, the case f=3 or both cases f=3, 4 can be treated in the same way as the case shown in the block 116 in the Figure, so that the error locators are given by the invalidity bits. The case f≥5 must always be dealt with via the block 114.

It may also occur that a negative test result in the block 104 leads to the block 114, via error correction (like in the block 106), when the syndrome result indicates exactly two incorrect words. It is advantageous to set the invalidity bits of the corrected words to the state "valid" in the blocks 106, 118. Sometimes (notably in the block 118), however, the invalidity bits will not be modified. It may also be that the test in the block

102 is omitted, so that the system proceeds directly from the block 100 to the block 104.

Figure 5 shows the processing of the data in the reproduction and correction element 54 of Figure 3. This flow chart relates to a preferred embodiment. When a group of 28 words has been received, the processing may commence (block 130). In block 132, the multiplication by the parity check matrix is performed in order to determine the syndrome variable and it is also detected whether this syndrome variable SYN indicates that at the most one incorrect code word is present. If this test is affirmative (Y), the system proceeds to block 134 in which correction takes place, possibly a dummy correction. Any invalidity bit for the code word to be corrected is then set to the state "valid". When the syndrome variable indicates that more than one word is incorrect, it is tested in block 136 whether the number f of invalidity bits is larger than two. If this is the case (Y), no correction can take place and the invalidity bits received are copied on the output code words of the element 54 of Figure 3. When the number of invalidity bits is smaller than three, it is tested in block 140 whether this number equals two. If this is so, the error is corrected in block 142. The result is tested in block 144. This result is incorrect if one or more words comprising an invalidity bit which indicates such "true" invalidity (compare the description of Figure 4) are not corrected. In the case of a "pro forma" validity bit, the correction at this level may also be a dummy correction. If two incorrect words are indicated by the syndrome variable, the correction can be "directly" performed. If it is detected in the block 140 that the number of invalidity bits equals 0 or 1, the system proceeds to the block 146. This also takes place if an "impossible" correction as defined hereabove is detected in the block 144. In the block 146, an invalidity bit (1) is added to all words of the outgoing group of data words (24), so that it is indicated that an error must be concealed in another manner. The flow chart may be modified. For example, a second upper limit for the number of invalidity bits can also be detected in the block 136. If the number is larger than, for example, four, a fault of the entire system is indicated, and all words are indicated as being invalid. It is also possible to use the invalidity bits as error locators in a given range of values for the number of invalid code words as explained with reference to the block 118 of Figure 4. However, this has been omitted from the Figure.

The outputs of the blocks 134, 138, 144, 146 in Figure 5 are connected to the block 148 whose function corresponds to that of the block 120 in Figure 4.

Other embodiments are also feasible within the scope of the invention. For example, the relevant delay times in elements 52 in Fig. 3 may all be chosen to be a factor 4 larger in the encoder/decoder.

Claims

1. An error correction method for the transfer of word-wise arranged data, comprising the following steps:

a. receiving a succession of first numbers of data words in a first error encoder and adding to each first number of data words a first series of parity words on the basis of a first generator matrix of a first word correction code;

b. interleaving said first numbers of data words and first series of parity words by means of respective delay times which are all different within each first number and associated first series in order to form a succession of second numbers of words, each second number of words having a number of data words equal to said first number plus a number of check words equal to the number in a first series;

c. receiving a second number of words of said succession in a second error encoder and adding to said second number of words a second series of parity words on the basis of a second generator matrix of a second word correction code so as to form a third number of words;

d. word-by-word modulation of serially linked said third numbers of words in order to form channel words for transfer, which satisfy, by way of added redundancy, predetermined upper limits and lower limits for the admissible intervals between directly successive signal transitions, said channel words being serially concatenated and pair-wise separated by merging bits which in combination with the channel words also satisfy said upper and lower limits;

e. demodulation of the channel words and merging bits after the transfer in order to reconstruct said third number of words (34);

f. receiving said third numbers of words, and from each third number reproducing, and if possible and necessary, correcting said second numbers of words (50), on the basis of the second parity check matrix associated with the second generator matrix;

g. de-interleaving (52) said second numbers of words, followed by the reproducing therefrom, and if possible and necessary, correcting said first numbers of data words for a user (54) on the basis of the first parity check matrix associated with the first generator matrix;

characterised in that during the demodulation a first flag bit is added to the word of said third number of words which is formed from an unrecognizable channel word, wherein before the reproduction of a said second number of words on the basis of the second parity check matrix under the control of an excessive number of first flag bits (116) within a said third number any error locator calculations associated to said second parity check matrix are omitted and a second flag bit is added (114) to each word of the relevant second number of words in order to indicate this number of words as being generally unreliable.

2. A method as claimed in claim 1, wherein said second error correction code is a systematic code,

102 is omitted, so that the system proceeds directly from the block 100 to the block 104.

Figure 5 shows the processing of the data in the reproduction and correction element 54 of Figure 3. This flow chart relates to a preferred embodiment. When a group of 28 words has been received, the processing may commence (block 130). In block 132, the multiplication by the parity check matrix is performed in order to determine the syndrome variable and it is also detected whether this syndrome variable SYN indicates that at the most one incorrect code word is present. If this test is affirmative (Y), the system proceeds to block 134 in which correction takes place, possibly a dummy correction. Any invalidity bit for the code word to be corrected is then set to the state "valid". When the syndrome variable indicates that more than one word is incorrect, it is tested in block 136 whether the number f of invalidity bits is larger than two. If this is the case (Y), no correction can take place and the invalidity bits received are copied on the output code words of the element 54 of Figure 3. When the number of invalidity bits is smaller than three, it is tested in block 140 whether this number equals two. If this is so, the error is corrected in block 142. The result is tested in block 144. This result is incorrect if one or more words comprising an invalidity bit which indicates such "true" invalidity (compare the description of Figure 4) are not corrected. In the case of a "pro forma" validity bit, the correction at this level may also be a dummy correction. If two incorrect words are indicated by the syndrome variable, the correction can be "directly" performed. If it is detected in the block 140 that the number of invalidity bits equals 0 or 1, the system proceeds to the block 146. This also takes place if an "impossible" correction as defined hereabove is detected in the block 144. In the block 146, an invalidity bit (1) is added to all words of the outgoing group of data words (24), so that it is indicated that an error must be concealed in another manner. The flow chart may be modified. For example, a second upper limit for the number of invalidity bits can also be detected in the block 136. If the number is larger than, for example, four, a fault of the entire system is indicated, and all words are indicated as being invalid. It is also possible to use the invalidity bits as error locators in a given range of values for the number of invalid code words as explained with reference to the block 118 of Figure 4. However, this has been omitted from the Figure.

The outputs of the blocks 134, 138, 144, 146 in Figure 5 are connected to the block 148 whose function corresponds to that of the block 120 in Figure 4.

Other embodiments are also feasible within the scope of the invention. For example, the relevant delay times in elements 52 in Fig. 3 may all be chosen to be a factor 4 larger in the encoder/decoder.

Claims

1. An error correction method for the transfer of word-wise arranged data, comprising the following steps:

a. receiving a succession of first numbers of data words in a first error encoder and adding to each first number of data words a first series of parity words on the basis of a first generator matrix of a first word correction code;

b. interleaving said first numbers of data words and first series of parity words by means of respective delay times which are all different within each first number and associated first series in order to form a succession of second numbers of words, each second number of words having a number of data words equal to said first number plus a number of check words equal to the number in a first series;

c. receiving a second number of words of said succession in a second error encoder and adding to said second number of words a second series of parity words on the basis of a second generator matrix of a second word correction code so as to form a third number of words;

d. word-by-word modulation of serially linked said third numbers of words in order to form channel words for transfer, which satisfy, by way of added redundancy, predetermined upper limits and lower limits for the admissible intervals between directly successive signal transitions, said channel words being serially concatenated and pair-wise separated by merging bits which in combination with the channel words also satisfy said upper and lower limits;

e. demodulation of the channel words and merging bits after the transfer in order to reconstruct said third number of words (34);

f. receiving said third numbers of words, and from each third number reproducing, and if possible and necessary, correcting said second numbers of words (50), on the basis of the second parity check matrix associated with the second generator matrix;

g. de-interleaving (52) said second numbers of words, followed by the reproducing therefrom, and if possible and necessary, correcting said first numbers of data words for a user (54) on the basis of the first parity check matrix associated with the first generator matrix;

characterised in that during the demodulation a first flag bit is added to the word of said third number of words which is formed from an unrecognizable channel word, wherein before the reproduction of a said second number of words on the basis of the second parity check matrix under the control of an excessive number of first flag bits (116) within a said third number any error locator calculations associated to said second parity check matrix are omitted and a second flag bit is added (114) to each word of the relevant second number of words in order to indicate this number of words as being generally unreliable.

2. A method as claimed in claim 1, wherein said second error correction code is a systematic code,

characterized in that during the reproduction of said second number of words on the basis of the second parity check matrix use is made of a number of first flag bits which is at most equal to a first upper limit that is at least equal to half the number of redundant words associated to said second parity check matrix, to act as error locators.

3. A method as claimed in claim 2 wherein said first upper limit is in excess of half said number of redundant words.

4. A method as claimed in claim 1, 2 or 3, characterized in that before the reproduction of a said first number of data words on the basis of the first parity check matrix under the control of an excessive further number of second flag bits within said second number any error locator calculations associated to said first parity check matrix are omitted and a third flag bit is added (146) to the relevant first number of data words in order to indicate them as being generally unreliable.

5. A method as claimed in claim 4, wherein said first error correction code is a systematic code, characterized in that during the reproduction of a said first number of data words on the basis of the first parity check matrix use is made of a number of second flag bits which is at most equal to a second upper limit at least equal to half the number of redundant words associated to said first parity check matrix, to act as further error locators.

6. A method as claimed in Claims 1 or 2 in which said first error correction code is a systematic code, characterized in that during the reproduction of a said first number of data words on the basis of the first parity check matrix under the control of the non-correction to be made in a word and a second flag bit which indicates exactly that word a third flag bit is added to each word of the relevant first number of data words in order to indicate said first number of data words as being generally unreliable.

7. An error correction method for the transfer of word-wide arranged data claimed in any of Claims 1 to 6, characterized in that numbers of merging bits amounting to three and said upper limit and lower limit being eleven and three channel bits, respectively.

8. A method for the demodulation and decoding of data transferred by means of an error correction method as claimed in any of the Claims 1 to 6, characterized in that a non-correctable first number of data words is replaced by substitute data.

9. A method for the demodulation and decoding of data transferred by means of an error correction method as claimed in any of the Claims 1 to 6, furthermore comprising serial-to-parallel by word conversion after the demodulation device (32) and parallel-by-word-to-serial reconversion (58) for transfer to a user.

10. A method as claimed in Claim 8 or 9, characterized in that for the demodulation a group of synchronizing channel bits is ignored, a further group of control bits being ignored for the (possibly correcting) reproduction after demodulation.

11. A method as claimed in Claim 8 or 9, wherein for the demodulation a group of synchronizing bits, accompanying a third group of words, is ignored, while a further group of control bits, is subject to an error correcting decoding as defined on a plurality of such groups of control bits, wherein the demodulator outputs a flag bit for signalling an unrecognizable group of control bits.

Patentansprüche

1. Verfahren zum Übertragen von wortweise geordneten Daten mit Fehlerkorrektur, wobei dieses Verfahren folgende Schritte enthält:

a. Empfang einer Aufeinanderfolge erster Anzahlen von Datenwörtern in einem ersten Fehlercoder und Zufügung zu jeder ersten Anzahl von Datenwörtern einer ersten Reihe von Paritätswörtern auf der Basis einer ersten Generatormatrix eines ersten wortkorrigierenden Codes;

b. Verschachtelung der ersten Anzahlen von Datenwörtern und der ersten Reihen von Paritätswörtern mittels jeweiliger Verzögerungszeiten, die alle in jeder ersten Anzahl und in jeder zugeordneten ersten Reihe verschieden sind, um eine Aufeinanderfolge zweiter Anzahlen von Wörtern zu bilden, wobei jede zweite Anzahl von Wörtern eine Anzahl von Datenwörtern gleich der ersten Anzahl von Wörtern eine Anzahl von Datenwörtern gleich der ersten Anzahl plus eine Anzahl von Prüfungswörtern gleich der Anzahl in einer ersten Reihe enthält;

c. Empfang einer zweiten Anzahl von Wörtern der Aufeinanderfolge in einem zweiten Fehlercoder und Zufügung zu der zweiten Anzahl von Wörtern einer zweiten Reihe von Paritätswörtern auf der Basis einer zweiten Generatormatrix eines zweiten Wortkorrekturcodes zur Bildung einer dritten Anzahl von Wörtern;

d. Wort-für-Wort-Modulation seriell verbundener dritter Anzahlen von Wörtern zur Bildung von Kanalwörtern für die Übertragung, wobei die Kanalwörter mittels ergänzter Redundanz vorgegebenen Obergrenzen und Untergrenzen für die zulässigen Intervalle zwischen direkt aufeinanderfolgenden Signalübergängen entsprechen, wobei die Kanalwörter seriell aneinandergereiht werden und durch Zwischenraumbits paarweise voneinander getrennt sind, die in Kombination mit den Kanalwörten ebenfalls den Ober- und den Untergrenzen entsprechen;

e. Demodulation der Kanalwörter und Zwischenraumbits nach der Übertragung zum Rekonstruieren der dritten Anzahl von Wörten (34);

f. Empfang der dritten Anzahlen von Wörtern und Wiedergabe sowie, so möglich und erforderlich, Korrektur der zweiten Anzahlen von Wörtern (50) aus jeder dritten Anzahl auf der Basis der mit der zweiten Generatormatrix verknüpften zweiten Paritätsprüfmatrix;

g. Entschachtelung (52) der zweiten Anzahlen von Wörtern, gefolgt von der Wiedergabe daraus und, wo möglich und erforderlich, der Korrektur der ersten Anzahlen von Datenwörtern für einen Benutzer (54) auf der Basis der mit der ersten Generatormatrix verbunden ersten Paritätsprüfmatrix;

dadurch gekennzeichnet, dass bei der Demodulation ein erstes Kennzeichenbit zu dem Wort der dritten Anzahl von Wörtern hinzugefügt wird, das aus einem unkenntlichen Kanalwort gebildet ist, wobei von der Wiedergabe einer zweiten Anzahl von Wörtern auf der Basis der zweiten Paritätsprüfmatrix unter der Steuerung einer übermässigen Anzahl erster Kennzeichenbits (116) in einer dritten Anzahl jede mit der zweiten Paritätsprüfmatrix verknüpfte Fehleradressenberechnung weggelassen wird und ein zweites Kennzeichenbit zu (114) jedem Wort der betreffenden zweiten Anzahl von Wörtern zugefügt wird, um diese Anzahl von Wörtern als im allgemeinen unzuverlässig anzuzeigen.

2. Verfahren nach Anspruch 1, in dem der zweite Fehlerkorrekturcode ein systematischer Code ist, dadurch gekennzeichnet, dass bei der Wiedergabe der zweiten Anzahl von Wörtern auf der Basis der zweiten Paritätsprüfmatrix eine Anzahl erster Kennzeichenbits verwendet wird, die höchstens gleich einer ersten Obergrenze ist, die wenigstens gleich der Hälfte der Anzahl redundanter Wörter und mit der zweiten.Paritätsprüfmatrix verbundener Wörter ist, um als Fehleradressen zu dienen.

3. Verfahren nach Anspruch 2, dadurch gekennzeichnet, dass die erste Obergrenze grösser ist als die Hälfte der Anzahl redundanter Wörter.

4. Verfahren nach Anspruch 1, 2 oder 3, dadurch gekennzeichnet, dass vor der Wiedergabe einer ersten Anzahl von Datenwörtern auf der Basis der ersten Paritätsprüfmatrix unter der Steuerung einer übermässigen weiteren Anzahl zweiter Kennzeichenbits innerhalb der zweiten Anzahl jede zu der ersten Paritätsprüfmatrix gehörende Fehleradressenberechnung weggelassen wird und die betreffende erste Anzahl von Datenwörtern zu einem dritten Kennzeichenbit zugefügt (146) wird, um sie als im allgemeinen unzuverlässig anzuzeigen.

5. Verfahren nach Anspruch 4, in dem der erste Fehlerkorrekturcode ein systematischer Code ist, dadurch gekennzeichnet, dass während der Wiedergabe einer ersten Anzahl von Datenwörtern auf der Basis der ersten Paritätsprüfmatrix eine Anzahl zweiter Kennzeichenbits verwendet wird, die höchstens gleich einer zweiten Obergrenze wenigstens gleich der Hälfte der Anzahl redundanter und der ersten Paritätsprüfmatrix zugeordneter Wörter ist, um als weitere Fehleradressen zu dienen.

6. Verfahren nach Anspruch 1 oder 2, in dem der erste Fehlerkorrekturcode eine systematischer Code ist, dadurch gekennzeichnet, dass bei der Wiedergabe einer ersten Anzahl von Datenwörtern auf der Basis der ersten Paritätsprüfmatrix unter der Steuerung der in einem Wort durchzuführenden Nicht-Korrektur und eines zweiten Kennzeichenbits, das genau dieses Wort anzeigt, jedem Wort der betreffenden ersten Anzahl von Datenwörtern zum Anzeigen der ersten Anzahl von Datenwörtern als im allgemeinen unzuverlässig ein erstes Kennzeichenbit zugefügt wird.

7. Fehlerkorrekturverfahren für die Übertragung wortweise geordneter Daten nach einem oder mehreren der Ansprüche 1 bis 6, dadurch gekennzeichnet, dass Anzahlen von Zwischenraumbits drei sind und die Obergrenze und Untergrenze elf bzw. drei Kanalbits betragen.

8. Verfahren für die Demodulation und Decodierung von mit einem Fehlerkorrekturverfahren übertragenen Daten nach einem oder mehreren der Ansprüche 1 bis 6, dadurch gekennzeichnet, dass eine nicht-korrigierbare erste Anzahl von Datenwörtern gegen Ersatzdaten ausgetauscht wird.

9. Verfahren für die Demodulation und Decodierung von mit einem Fehlerkorrekturverfahren übertragenen Daten nach einem oder mehreren der Ansprüche 1 bis 6, dadurch gekennzeichnet, dass weiter eine wortweise Serien/Parallel-Umwandlung nach der Demodulationsanordnung (32) und wortweise Parallel/Serien-Rückwandlung (58) für Übertragung auf einen Benutzer vorgesehen sind.

10. Verfahren nach Anspruch 8 oder 9, dadurch gekennzeichnet, dass für die Demodulation eine Gruppe synchronisierender Kanalbits ausser Betracht gelassen wird, wobei eine weitere Gruppe von Steuerbits für die (mögliche korrigierende) Wiedergabe nach der Demodulation ausser Betracht gelassen wird.

11. Verfahren nach Anspruch 8 oder 9, dadurch gekennzeichnet, dass für die Demodulation eine Gruppe synchronisierender Bits, die eine dritte Gruppe von Wörtern begleitet, ausser Betracht gelassen wird, während eine weitere Gruppe von Steuerbits einer Fehlerkorrekturdecodierung, wie für eine Vielzahl derartiger Gruppen von Steuerbits definiert, unterworfen wird, wobei der Demodulator ein Kennzeichenbit für die Signalisierung einer unkenntlichen Gruppe von Steuerbits ausgibt.

Revendications

1. Procédé de correction d'erreurs pour le transfert de données agencées en mots, comprenant les opérations suivantes:

a. réception d'une succession de premiers nombres de mots de données dans un premier codeur d'erreurs et addition à chaque premier nombre de mots de données d'une première série de mots de parité sur la base d'une première matrice de générateur d'un premier code de correction de mots;

b. imbrication des premiers nombres de mots de données et des premières séries de mots de parité à l'aide de retards respectifs qui sont tous différents dans chaque premier nombre et dans chaque première série associée pour former une succession de seconds nombres de mots, chaque

second nombre de mots comportant un nombre de mots de données égal au premier nombre plus un nombre de mots de contrôle égal au nombre dans une première série;

c. réception d'un second nombre de mots de la dite succession dans un second codeur d'erreurs et addition au second nombre de mots d'une seconde série de mots de parité sur la base d'une seconde matrice de générateur d'un second code de correction de mots de manière à former un troisième nombre de mots;

d. modulation mot par mot des troisièmes nombres de mots reliés en série afin de former des mots de canal pour le transfert, qui satisfont, par ajoute de redondance, à des limites supérieures et à des limites inférieures prédéterminées pour les intervalles admissibles entre des transitions de signaux directement successives, ces mots de canal étant concaténés en série et séparés par paires pare des bits interclassés qui, en combinaison avec les mots de canal, satisfont également aux dites limites supérieures et limites inférieures;

e. démodulation des mots de canal et des bits interclassés après le transfert, afin de reconstruire le troisième nombre de mots (34);

f. réception des troisièmes nombres de mots et reproduction à partir de chaque troisième nombre et, si possible et nécessaire, correction des seconds nombres de mots (50), sur la base de la seconde matrice de contrôle de parité associée à la seconde matrice de générateur;

g. désimbrication (52) des seconds nombres de mots, suivie par la reproduction et, si possible et nécessaire, la correction des premiers nombres de mots de données pour un utilisateur (54) sur la base de la première matrice de contrôle de parité associée à la première matrice de générateur,

caractérisé en ce que, pendant la démodulation, un premier bit indicateur est ajouté au mot du troisième nombre de mots qui est formé à partir d'un mot de canal non reconnaissable, où, avant la reproduction d'un deuxième nombre de mots sur la base de la deuxième matrice de contrôle de parite, sous la commande d'un nombre excessif de premiers bits indicateurs (116) dans un troisième nombre, tous les calculs de localisateurs d'erreurs associés à cette deuxième matrice de contrôle de parité sont omis et un second bit indicateur est ajouté (114) à chaque mot du deuxième nombre de mots en question afin d'indiquer ce nombre de mots comme étant dans l'ensemble non fiable.

2. Procédé suivant la revendication 1, dans lequel le second code de correction d'erreurs est un code systématique, caractérisé en ce que pendant la reproduction du second nombre de mots sur la base de la seconde matrice de contrôle de parité, on utilise un nombre de premiers bits indicateurs qui est tout au plus égal à une première limite supérieure qui est au moins égale à la moitié du nombre de mots redondants associés à la seconde matrice de contrôle de parité, afin de servir de localisateurs d'erreurs.

3. Procédé suivant la revendication 2, dans lequel la première limite supérieure excède cette moitié du nombre de mots redondants.

4. Procédé suivant la revendication 1, 2 ou 3, caractérisé en ce que avant la reproduction d'un premier nombre de mots de données sur la base de la première matrice de contrôle de parité sous la commande d'un autre nombre excessif de seconds bits indicateurs dans le second nombre, tous les calculs de localisateurs d'erreurs associés à la première matrice de contrôle de parité sont omis et un troisième bit indicateur est ajouté (146) au premier nombre en question de mots de données afin de les indiquer comme étant dans l'ensemble non fiables.

5. Procédé suivant la revendication 4, dans lequel le premier code de correction d'erreurs est un code systèmatique, caractérisé en ce que pendant la reproduction d'un premier nombre de mots de données sur la base de la première matrice de contrôle de parité, on utilise un nombre de seconds bits indicateurs qui est tout au plus égal à une seconde limite supérieure au moins égale à la moitié du nombre de mots redondants associés à la première matrice de contrôle de parité, afin de servir d'autres localisateurs d'erreurs.

6. Procédé suivant la revendication 1 ou 2, dans lequel le premier code de correction d'erreurs est un code systématique, caractérisé en ce que pendant la reproduction d'un premier nombre de mots de données sur la base de la première matrice de contrôle de parité sous la commande de la non-correction à effectuer dans un mot et d'un second bit indicateur qui indique exactement ce mot, un troisième bit indicateur est ajouté à chaque mot du premier nombre en question de mots de données afin d'indiquer ce premier nombre de mots de données comme étant dans l'ensemble non fiable.

7. Procédé de correction d'erreurs pour le transfert de données agencées en mots suivant l'une quelconque des revendications 1 à 6, caractérisé en ce que les nombres de bits interclassés s'élévent à trois et la limite supérieure et la limite inférieure sont, respectivement, de onze et de trois bits de canal.

8. Procédé pour la démodulation et le décodage de données transférées au moyen d'un procédé de correction d'erreurs suivant l'une quelconque des revendications 1 à 6, caractérisé en ce qu'un premier nombre de mots de données non corrigibles est remplacé par des données de substitution.

9. Procédé pour la démodulation et le décodage de données transférées au moyen d'un procédé de correction d'erreurs suivant l'une quelconque des revendications 1 à 6 comprenant, en outre, une conversion série-vers-parallèle par mots après le dispositif démodulateur (32) et une reconversion parallèle par mots-vers-série 58) en vue d'un transfert à un utilisateur.

10. Procédé suivant la revendication 8 ou 9, caractérisé en ce que pour la démodulation, un groupe de bits de canal de synchronisation est négligé, un autre groupe de bits de commande

étant négligé pour la reproduction (éventuellement correctrice) après démodulation.

11. Procédé suivant la revendication 8 ou 9, dans lequel, pour la démodulation, un groupe de bits de synchronisation, accompagnant un troisième groupe de mots, est négligé, tandis qu'un autre groupe de bits de commande est soumis à un décodage de correction d'erreurs tel que défini sur plusieurs de ces groupes de bits de commande, où le démodulateur produit un bit indicateur pour signaler un groupe de bits de commande non reconnaissable.