CLAIMS

What is claimed is:

1. A chip package comprising:

a first die comprising an active surface having at least one die pad positioned thereon;

a first adhesive layer having a first surface coupled to the active surface of the first die and a second surface opposite the first surface;

a first dielectric layer having a top surface, wherein a first portion of the top surface of the first dielectric layer is coupled to the second surface of the first adhesive layer; and

wherein a second portion of the top surface of the first dielectric layer, distinct from the first portion, is substantially free of adhesive.

2. The chip package of claim 1 wherein the second portion of the top surface of the first dielectric layer substantially surrounds the first portion of the top surface of the dielectric layer.

3. The chip package of claim 1 wherein the first surface of the first adhesive layer has a surface area approximately equal to a surface area of the active surface of the first die.

4. The chip package of claim 1 further comprising:

a second die comprising an active surface having at least one die pad positioned thereon;

a second adhesive layer having a first surface coupled to the active surface of the second die and a second surface opposite the first surface; and

wherein the second surface of the second adhesive layer is coupled to a third portion of the top surface of the first dielectric layer.

5. The chip package of claim 4 wherein the first and second dies are positioned such that a gap is formed therebetween; and

wherein a portion the top surface of the first dielectric layer that is aligned with the gap is substantially free of adhesive.

6. The chip package of claim 1 wherein the first adhesive layer is non-conductive.

7. The chip package of claim 1 further comprising a first metallization layer coupled to the top surface of the first dielectric layer.

8. The chip package of claim 7 further comprising a first plurality of metalized connections formed through the first dielectric layer and in contact with at least one of the first metallization layer and the at least one die pad.

9. The chip package of claim 1 further comprising a re-distribution layer coupled to a bottom surface of the dielectric layer, opposite the top surface, wherein the re-distribution layer comprises:

a second dielectric layer;

a second metallization layer coupled to the second dielectric layer; and

a second plurality of metalized connections formed through the second dielectric layer and in electrical contact with the first and second metallization layers.

10. A method of forming an integrated chip package comprising:

providing a first semiconductor die comprising an active surface having at least one contact pad positioned thereon;

applying an adhesive layer to the active surface of the first semiconductor die; and

adhering the first semiconductor die having the adhesive layer applied thereto to a top surface of a dielectric substrate by way of the adhesive layer.

11. The method of claim 10 wherein applying the adhesive layer to the active surface of the first semiconductor die comprises applying the adhesive layer to a semiconductor wafer such that a first surface of the adhesive layer is in contact with an active surface of the semiconductor wafer; and

further comprising singulating the first semiconductor die from the semiconductor wafer.

12. The method of claim 11 further comprising coupling a release sheet to a second surface of the adhesive layer, opposite the first surface, prior to singulating the first semiconductor die.

13. The method of claim 11 further comprising B-stage curing the adhesive layer prior to singulating the first semiconductor die.

14. The method of claim 10 further comprising:

providing a second semiconductor die comprising an active surface having at least one die pad positioned thereon;

applying an adhesive layer to the active surface of the second semiconductor die; and

adhering the second semiconductor die having the adhesive layer applied thereto to the top surface of the dielectric substrate.

15. The method of claim 14 further comprising positioning the first semiconductor die and the second semiconductor die on the top surface of the dielectric substrate such that a gap is formed on the top surface of the dielectric substrate between the adhesive layers of the first and second semiconductor die.

16. The method of claim 10 further comprising:

forming a first metallization layer on the top surface of the dielectric substrate; and

forming a first plurality of metalized connections through the dielectric substrate, the first plurality of metalized connections in contact with at least one of the first metallization layer and the at least one contact pad.

17. An integrated chip package comprising:

a dielectric substrate; and

a first die assembly comprising:

a semiconductor die having an active surface with contact pads positioned thereon; and

a non-conductive adhesive layer having a first surface coupled to the active surface of the semiconductor die;

wherein a surface area of the first surface of the adhesive layer is substantially equal to a surface area of the active surface of the semiconductor die; and

wherein a second surface of the adhesive layer, opposite the first surface, is coupled to a surface of the dielectric substrate; and

wherein a subportion of the surface of the flexible substrate adjacent to the first die assembly is substantially free of adhesive.

18. The integrated chip package of claim 17 further comprising:

a second die assembly comprising:

a semiconductor die having an active surface with contact pads positioned thereon; and

an adhesive layer coupled to the active surface of the semiconductor die; wherein a surface area of the adhesive layer is substantially equal to a surface area of the active surface of the semiconductor die; and

wherein the second die assembly is coupled to the surface of the flexible substrate.

19. The integrated chip package of claim 18 wherein a gap formed on the surface of the flexible substrate between the first and second die assemblies is substantially free of adhesive.

20. The integrated chip package of claim 18 wherein the second die assembly is positioned on the surface of the flexible substrate such that the adhesive layer of the first die assembly is not in contact with the adhesive layer of the second die assembly.

21. A method of forming an integrated chip package comprising:

providing a dielectric substrate having a die location positioned on a top surface thereof;

providing a first semiconductor die comprising an active surface having at least one contact pad positioned thereon;

applying an adhesive layer to one of the active surface of the first semiconductor die and the die location of the dielectric substrate, the adhesive layer having a surface area approximately equal to the surface area of the active surface of the first semiconductor die; and

adhering the first semiconductor die to the top surface of the dielectric substrate by way of the adhesive layer.

22. The method of claim 21 further comprising applying the adhesive layer to the active surface of the first semiconductor die prior to adhering the first semiconductor die to the dielectric substrate.

23. The method of claim 21 further comprising applying the adhesive layer to the die location on the top surface of the dielectric substrate die prior to adhering the first semiconductor die to the dielectric substrate.

24. The method of claim 23 further comprising positioning at least one partially-cured adhesive pad on the top surface of the dielectric substrate.

25. The method of claim 23 further comprising performing a masking operation to apply the adhesive layer to the die location on the top surface of the dielectric substrate.

26. The method of claim 23 further comprising:

aligning a metal screen with the top surface of the dielectric substrate such that an opening in the metal screen is aligned with the die location on the top surface of the dielectric substrate; and

dispensing an adhesive through the openings in the metal screen to form the adhesive layer.

27. The method of claim 23 further comprising inkjet printing the adhesive layer on the top surface of the dielectric substrate.

28. The method of claim 21 further comprising applying the adhesive layer such that an area of the top surface of the dielectric substrate surrounding the die location is substantially free of adhesive.

29. A method of forming an integrated chip package comprising:

providing a dielectric substrate having a plurality of die locations positioned on a surface thereof;

applying a patterned adhesive layer onto the plurality of die locations of the dielectric substrate such that a gap is formed on the surface of the dielectric substrate between adjacent die locations, the gap being substantially free of adhesive; and

adhering a plurality of semiconductor dies to the dielectric substrate via the adhesive layer.

30. The method of claim 29 further comprising one of:

inkjet printing the adhesive layer onto the plurality of die locations of the dielectric substrate; and

patterning the adhesive layer onto the plurality of die locations of the dielectric substrate through a screen having a plurality of holes corresponding to the respective die locations formed therein.

31. The method of claim 29 further comprising:

forming a plurality of partially-cured adhesive portions, each adhesive portion having a surface area substantially equal to a surface area of an active surface of a respective semiconductor die; and

positioning the plurality of partially-cured adhesive portions onto the plurality of die locations of the dielectric substrate to form the patterned adhesive layer.

32. The method of claim 29 further comprising partially curing the adhesive layer prior to adhering the plurality of semiconductor dies thereto.

33. The method of claim 29 further comprising fully curing the adhesive layer after adhering the plurality of dies thereto.

34. The method of claim 29 further comprising patterning the adhesive layer such that subportions of the surface of the dielectric substrate surrounding the plurality of die locations are substantially free of adhesive.

35. The method of claim 29 further comprising:

forming a first metallization layer on the surface of the dielectric substrate; and

forming a first plurality of metalized connections through the dielectric substrate, the first plurality of metalized connections in contact with at least one of the first metallization layer and at least one contact pad of a die of the plurality of semiconductor dies.

CLAIMS

What is claimed is:

1. A method of forming an integrated chip package comprising:

providing a first semiconductor die comprising an active surface having at least one contact pad positioned thereon;

applying an adhesive layer to the active surface of the first semiconductor die; and

adhering the first semiconductor die having the adhesive layer applied thereto to a top surface of a dielectric substrate by way of the adhesive layer;

wherein applying the adhesive layer to the active surface of the first semiconductor die comprises:

applying the adhesive layer to a semiconductor wafer such that a first surface of the adhesive layer is in contact with an active surface of the semiconductor wafer; and

singulating the first semiconductor die from the semiconductor wafer.

2. The method of claim **1** further comprising coupling a release sheet to a second surface of the adhesive layer, opposite the first surface, prior to singulating the first semiconductor die.

3. The method of claim **1** further comprising B-stage curing the adhesive layer prior to singulating the first semiconductor die.

4. The method of claim **1** further comprising:

providing a second semiconductor die comprising an active surface having at least one die pad positioned thereon;

applying an adhesive layer to the active surface of the second semiconductor die; and

adhering the second semiconductor die having the adhesive layer applied thereto to the top surface of the dielectric substrate.

5. The method of claim **4** further comprising positioning the first semiconductor die and the second semiconductor die on the top surface of the dielectric substrate such that a gap is formed on the top surface of the dielectric substrate between the adhesive layers of the first and second semiconductor die.

6. The method of claim **1** further comprising:

forming a first metallization layer on the top surface of the dielectric substrate; and

forming a first plurality of metalized connections through the dielectric substrate, the first plurality of metalized connections in contact with at least one of the first metallization layer and the at least one contact pad.