ABSTRACT

METHOD OF VACUUM PACKAGING A SEMICONDUCTOR DEVICE ASSEMBLY

A semiconductor chip device package comprised of a semiconductor substrate having semiconductor devices formed on the semiconductor substrate. At least one dielectric layer is over the semiconductor substrate. At least one layer of interconnects is over the semiconductor devices and within the at least one respective dielectric layer with at least a portion of the interconnects being separated by voids having a vacuum or air therein. A passivation layer is over the uppermost of the at least one layer of interconnects. Wherein the semiconductor chip device is vacuum sealed within a semiconductor chip device package.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)