S P E C I F I C A T I O N

TITLE OF THE INVENTION

Semiconductor Device

BACKGROUND OF THE INVENTION

The present invention relates to a resin-sealed type semiconductor device of an LOC (Lead On Chip) structure and, more particularly, to a technique which is effective when applied to a thin small-sized semiconductor package of a TSOP (Thin Small Outline Package) structure or the like.

A resin-sealed type semiconductor device of an LOC structure of the prior art comprises, as shown in Fig. 22 (see Japanese Patent Laid-Open No. 2-246125/1990), for example, a semiconductor chip 1 including a circuit and a plurality of external terminals formed over a major face of a semiconductor substrate, a plurality of leads each including an inner lead portion 3A having inner leads $3A_1$ having signal inner leads (a first region) and a common inner lead for supplying a power voltage and an earth voltage (a second region: hereinafter referred to as the bus-bar leads or fixed potential leads) $3A_2$, and an outer lead portion 3B formed integrally with the inner lead

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portions 3A, bonding wires 5 for electrically connecting the external terminals (pads) and the signal inner leads $3A_1$ and the bus-bar leads $3A_2$ of the inner lead portions 3A respectively, and a sealer 2A for sealing the semiconductor chip 1, the inner lead portions 3A and the bonding wires 5. The signal inner leads $3A_1$ and the bus-bar leads $3A_2$ are arranged over the major face of the semiconductor chip 1 through an insulating film 4, and the bus-bar leads $3A_2$ are arranged substantially in parallel with the major face of the semiconductor chip 1.

SUMMARY OF THE INVENTION

Here will be described the items which have not been disclosed in the publicly-known document (Japanese Patent Laid-Open No. 2-246125/1990) and have been investigated by the present inventor.

When a resin-sealed type semiconductor device of an LOC structure, as shown in Fig. 22, is applied as it is to a thin small-sized semiconductor package (TSOP), as shown in Figs. 23 and 24(a), the entire package becomes thin (e.g., 1.0 mm), so that the resin over the inner leads $3A_1$ accordingly becomes as thin as 0.195 mm. This makes it necessary to set the loop heights of the wires 5 at small values. However, the

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bonding wires 5 and the bus-bar leads $3A_2$ of the signal wires may contact, causing short circuit, and thereby making it difficult to thin the resin. When the wire loop heights must be suppressed to low levels, a contrivance that an insulating coating material 20 is applied to the bus-bar leads $3A_2$ is needed.

Here will be described the schematic construction of Fig. 23 (a top plan view of a resin-sealed type semiconductor device of a TSOP structure) and Fig. 24 (a section of an essential part of Fig. 23). In this resin-sealed type semiconductor device of the TSOP structure, to a face of a semiconductor substrate of a semiconductor chip 1 (hereinafter referred to as the "major face of the semiconductor chip 1") where a circuit and a plurality of external terminals are formed, inner lead portions 3A which include a plurality of signal line inner leads $3A_1$ and the bus-bar leads $3A_2$ having insulating coating material 20 applied to their upper faces are fixed through the insulating film 4. The inner lead portions 3A and the outer lead portions 3B formed integrally with the former constitute leads 3.

As shown in Figs. 23 and 24, the signal line inner leads $3A_1$ and the bus-bar leads $3A_2$, having the

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insulating coating material 20 applied to their upper faces, of the inner lead portions 3A are arranged over the major face of the semiconductor chip 1 through the insulating film 4, and the bus-bar leads $3A_2$ are arranged substantially in parallel with the major face of the semiconductor chip 1.

The plurality of signal inner leads $3A_1$, the bus-bar leads $3A_2$ and the semiconductor chip 1 are electrically connected through the bonding wires 5 and are sealed with a mold resin (the sealing body) 2A. The thin type package 2 thus sealed is shaped by cutting suspension leads (chip supporting leads) 3C and the outer lead portions 3B from the lead frame.

In a thin small-sized semiconductor package (of a TSOP structure) having been investigated by the present inventor, the mold resin 2A over the semiconductor chip 1 is thin, as shown in Fig. 24(a), there arise problems of appearance defect in which the bonding wires 5 such as Au wires are seen through from the upper face of the package, and of exposure of the wire themselves to the outside. If this thickness is made further smaller (to about 0.5 mm), as shown in Fig. 24(b), the problems of appearance defect and the wire exposure are more critical.

Another problem is that when the mold resin (the

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sealing body) 2A over the major face of the semiconductor chip is thinned, cracks occur thereby deteriorating the reliability.

In order to lower the wire loops, as shown in Fig. 24(c), it is conceivable to disuse the insulating tape 4 and to fix the signal inner leads $3A_1$ and the bus-bar leads $3A_2$ to the major face of the semiconductor chip 1 directly with adhesive. If the distances (spacings) between the major face of the semiconductor chip 1 and the signal inner leads $3A_1$ become short, however, the parasitic capacitance between the major face of the semiconductor chip 1 and the signal inner leads $3A_1$ increases to raise a problem that the electric characteristics are deteriorated.

An object of the invention is to provide a technique capable of thinning the semiconductor package without deteriorating the electric characteristics.

Another object of the invention is to provide a technique capable of suppressing the parasitic capacitance between the major face of the semiconductor chip and the leads even if the semiconductor package is thinned.

Another object of the invention is to provide a

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technique capable of ensuring a proper thickness of the sealer over the semiconductor chip of the semiconductor package even if the entire thickness of the semiconductor package is reduced.

Another object of the invention is to provide a technique capable of balancing the quantities of the upper and lower sealers of the semiconductor chip even if the entire thickness of the semiconductor package is reduced.

The foregoing and other objects and novel features of the invention will become apparent from the following description to be made with reference to the accompanying drawings.

Of the inventions to be disclosed herein, the representative ones will be briefly summarized in the following.

(1) A semiconductor device comprises a semiconductor chip including a circuit and a plurality of external terminals formed over a major face of a semiconductor substrate, a plurality of leads each including an inner lead portion and an outer lead portion formed integrally with the inner lead portions, bonding wires electrically connecting the external terminals and the inner lead portions respectively, and a sealing body for sealing the

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semiconductor chip, the inner lead portions and the bonding wires, wherein the inner lead portions are arranged over the major face of the semiconductor chip at predetermined spacings between the major face and the inner leads, and the portions of the inner leads arranged over the major face are thinner than the other portions of the inner leads.

(2) In a resin-sealed type semiconductor device of the aforementioned invention (1), the portions, arranged over the major face of the semiconductor chip, of the inner lead portions are fixed at their leading end portions to the major face of the semiconductor chip through an insulating film.

(3) In a resin-sealed type semiconductor device of the aforementioned invention (1), the portions, arranged over the major face of the semiconductor chip, of the inner lead portions are fixed at their leading end portions to the major face of the semiconductor chip directly with adhesive.

(4) A semiconductor device comprises a semiconductor chip including a circuit and a plurality of external terminals formed over a major face of a semiconductor substrate, a plurality of leads each including an inner lead portion having a first region, and an inner lead portion having a second region and

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an outer lead portion formed integrally with the inner lead portions bonding wires electrically connecting the external terminals and the first regions and the second regions of the inner lead portions respectively, and a sealing body for sealing the semiconductor chip, the inner lead portions and the bonding wires, wherein the first regions and the second regions of the inner lead portions are arranged over the major face of the semiconductor chip, wherein the first regions of the inner lead portions are arranged at predetermined spacings between the major face and the inner leads, wherein the portions of the inner leads arranged over the major face are thinner than the other portions of the inner leads, and wherein the inner leads arranged over the major face are fixed at their leading end portions to the major face of the semiconductor chip through an insulating film.

(5) In a resin-sealed type semiconductor device of the aforementioned invention (4), the semiconductor chip is rectangular, the second regions of the inner lead portions have portions arranged substantially in parallel with the long sides of the semiconductor chip, and the parallel-arranged portions are arranged between the external terminals and the leading end

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portions of the inner leads.

(6) A semiconductor device comprises a semiconductor chip including a circuit and a plurality of external terminals formed over a major face of a semiconductor substrate, a plurality of leads each including an inner lead portion having a first region, and an inner lead portion having a second region and an outer lead portion formed integrally with the inner lead portions, bonding wires electrically connecting the external terminals and the first regions and the second regions of the inner lead portions respectively, and a sealing body for sealing the semiconductor chip, the inner lead portions and the bonding wires, wherein the first regions and the second regions of the inner lead portions are arranged over the major face of the semiconductor chip, wherein the first regions of the inner lead portions are arranged at predetermined spacings between the major face and the inner leads, and wherein the portions of the inner leads arranged over the major face are thinner than the other portions of the inner leads and are not fixed at their leading end portions to the major face of the semiconductor chip.

(7) In a resin-sealed type semiconductor device of the aforementioned invention (4) or (6), the first

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regions of the inner lead portions are signal leads whereas the second regions are fixed potential leads.

(8) A semiconductor device comprises a semiconductor chip including an integrated circuit and a plurality of external terminals formed over a major face of the semiconductor chip, a plurality of leads each including an inner lead portion and an outer lead portion formed integrally with the inner lead portions, portions of the inner lead portions being arranged over the major face of the semiconductor chip and electrically connected to the corresponding external terminals, and a resin member for sealing the inner lead portions of the plurality of leads and the semiconductor chip, wherein the inner lead portions each include a first surface on the major face side of the semiconductor chip, a second surface on the opposite side to the first surface, a first portion positioned over the major face of the semiconductor chip, and a second portion formed integrally with the first portion and positioned outside the major face of the semiconductor chip, wherein the first portions of the inner lead portions are made thinner than the second portions in the thickness direction of the semiconductor chip, and wherein the first surfaces of the first portions of the inner lead portions are more

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spaced from the semiconductor chip in the thickness direction of the semiconductor chip than the first surfaces of the second portions of the inner lead portions.

(9) In a resin-sealed type semiconductor device of the aforementioned invention (8), the first portions of the inner lead portions are bonded to the major face of the semiconductor chip through an insulating film.

(10) In a resin-sealed type semiconductor device of the aforementioned invention (8), the first portions of the inner lead portions are bonded to the major face of the semiconductor chip through adhesive.

(11) In a resin-sealed type semiconductor device of the aforementioned invention (8), the inner lead portions and the corresponding external terminals are connected through wires.

(12) In a resin-sealed type semiconductor device of the aforementioned invention (11), the plurality of leads include signal leads and fixed potential leads, the inner lead portions of the fixed potential leads are partially arranged over the major face of the semiconductor chip between the plurality of external terminals of the leading ends of the inner lead portions of the signal leads, and the wires

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electrically connecting the inner lead portions of the signal leads and the corresponding external terminals are so arranged as to cross over portions of the inner lead portions of the fixed potential leads.

(13) A semiconductor device comprises a semiconductor chip including an integrated circuit and a plurality of external terminals formed over a major face of the semiconductor chip, a plurality of signal leads each including an inner lead portion and an outer lead portion formed integrally with the inner lead portions, portions of the inner lead portions being arranged over the major face of the semiconductor chip and electrically connected to the corresponding external terminals through wires, fixed potential leads each including an inner lead portion and an outer lead portion formed integrally with the inner lead portions, the inner lead portions being partially arranged over the major face of the semiconductor chip and electrically connected to the corresponding external terminals, and a resin member for sealing the inner lead portions of the plurality of signal leads, the inner lead portions of the fixed potential leads, and the semiconductor chip, wherein the inner lead portions of the signal leads each include a first surface on the major face side of the

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semiconductor chip, a second surface on the opposite side to the first surface, a first portion positioned over the major face of the semiconductor chip, and a second portion formed integrally with the first portions and positioned outside the major face of the semiconductor chip, wherein the first portions of the inner lead portions of the signal leads are made thinner than the second portions in the thickness direction of the semiconductor chip, wherein the first surfaces of the first portions of the inner lead portions the signal leads are more spaced from the semiconductor chip in the thickness direction of the semiconductor chip than the first surfaces of the second portions of the inner lead portions, wherein the inner lead portions of the fixed potential leads are partially arranged over the major face of the semiconductor chip between the leading ends of the inner lead portions of the signal leads and the plurality of external terminals, and wherein the inner lead portions of the fixed potential leads are partially arranged lower in the thickness direction of the semiconductor chip than the leading ends of the inner lead portions of the signal leads.

(14) In a resin-sealed type semiconductor device of the aforementioned invention (13), the inner lead

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portions of the fixed potential leads are partially bonded to the major face of the semiconductor chip with adhesive, and the inner lead portions of the signal leads are spaced at their leading ends from the major face of the semiconductor chip.

(15) In a resin-sealed type semiconductor device of the aforementioned invention (13), the inner lead portions of the signal leads are bonded at their leading ends to the major face of the semiconductor chip through an insulating film.

(16) In a resin-sealed type semiconductor device of the aforementioned invention (13), the wires electrically connecting the inner lead portions of the signal leads and the corresponding external terminals are so arranged as to cross over portions of the inner lead portions of the fixed potential leads.

(17) A semiconductor device comprises a semiconductor chip including an integrated circuit and a plurality of external terminals formed over a major face of the semiconductor chip, a plurality of signal leads each including an inner lead portion and an outer lead portion formed integrally with the inner lead portions, portions of the inner lead portions being arranged over the major face of the semiconductor chip and electrically connected to the

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corresponding external terminals through wires fixed potential leads each including an inner lead portion and an outer lead portion formed integrally with the inner lead portions, the inner lead portions being partially arranged over the major face of the semiconductor chip and electrically connected to the corresponding external terminals, and a resin member for sealing the inner lead portions of the plurality of signal leads, the inner lead portions of the fixed potential leads, and the semiconductor chip, wherein the inner lead portions of the signal leads each includes a first surface on the major face side of the semiconductor chip, a second surface on the opposite side to the first surface, a first portion positioned over the major face of the semiconductor chip, and a second portion formed integrally with the first portion and positioned outside the major face of the semiconductor chip, wherein the first portions of the inner lead portions of the signal leads are made thinner than the second portions in the thickness direction of the semiconductor chip, wherein the first portions of the inner lead portions of the signal leads have leading end portions to be connected to the wires, wherein the first surfaces of the first portions of the inner lead portions of the signal

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leads other than the leading end portions are more spaced from the semiconductor chip in the thickness direction of the semiconductor chip than the first surfaces of the second portions of the inner lead portions, wherein the first portions of the inner lead portions of the signal leads are arranged lower in the thickness direction of the semiconductor chip than the first portions of the inner lead portions of the signal leads other than the leading end portions, wherein the inner lead portions of the fixed potential leads are partially arranged over the major face of the semiconductor chip between the leading end portions of the first portions of the inner lead portions of the signal leads and the plurality of external terminals, and wherein the inner lead portions of the fixed potential leads are partially arranged lower in the thickness direction of the semiconductor chip than the first portions of the inner lead portions of the signal leads other than the leading end portions.

(18) In a resin-sealed type semiconductor device of the aforementioned invention (17), portions of the inner lead portions of the fixed potential leads and the leading end portions of the inner lead portions of the signal leads are bonded to the major face of the

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semiconductor chip with adhesive.

(19) In a resin-sealed type semiconductor device of the aforementioned invention (17), the wires connecting the inner lead portions of the signal leads and the corresponding external terminals are so arranged as to cross over portions of the inner lead portions of the fixed potential leads.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic top plan view showing the construction of a resin-sealed type semiconductor device of Mode 1 of the invention;

Fig. 2 is a section of an essential part of Fig. 1;

Fig. 3 is a schematic top plan view showing the construction of a resin-sealed type semiconductor device of Mode 2 of the invention;

Fig. 4 is a section of an essential part taken along line A - A' of Fig. 3;

Fig. 5 is a section of an enlarged view of a part enclosed by a circle M shown in Fig. 4;

Fig. 6 is a section of an essential part taken along line B - B' of Fig. 3;

Fig. 7 is a diagram for explaining a method of bonding wires to signal line inner leads;

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Fig. 8 is a diagram for explaining another method of bonding wires to signal line inner leads;

Fig. 9 is a schematic top plan view showing the construction of a resin-sealed type semiconductor device of Mode 3 of the invention;

Fig. 10 is a section of an essential part of Fig. 9;

Fig. 11 is a schematic top plan view showing the construction of a resin-sealed type semiconductor device of Mode 4 of the invention;

Fig. 12 is a section of an essential part of Fig. 11;

Fig. 13 is a schematic top plan view showing a construction of a resin-sealed type semiconductor device of Mode 5 of the invention;

Fig. 14 is a section of an essential part taken along line A - A' of Fig. 13;

Fig. 15 is a section of an essential part taken along line B - B' of Fig. 13;

Fig. 16 is a diagram showing a region H where the back faces of the inner lead portions are half-etched;

Fig. 17 is a diagram showing the shape of one of the external leads (outer leads);

Fig. 18 is a schematic top plan view showing the construction of a module of a semiconductor storage

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device of Mode 6 of the invention;

Fig. 19 is a side elevation of Fig. 18;

Fig. 20 is a schematic top plan view showing the construction of an electronic device of Mode 7 of the invention;

Fig. 21 is a side elevation of Fig. 20;

Fig. 22 is a partially cut-away schematic perspective view showing the entire construction of a resin-sealed type semiconductor device of an LOC structure of the prior art;

Fig. 23 is a schematic top plan view showing a construction of a resin-sealed type semiconductor device of a TSOP structure having been investigated by us; and

Fig. 24 is a section of an essential part of Fig. 23.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The invention will be described in detail in connection with its modes with reference to the accompanying drawings.

Throughout all the drawings for explaining the modes of the invention, the portions having identical functions are designated by the identical reference numerals, and their repeated description will be

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omitted.

(Mode 1)

Fig. 1 is a schematic top plan view showing the construction of a resin-sealed type semiconductor device of Mode 1 of the invention; Fig. 2(a) is a section of an essential part taken along line A - A' of Fig. 1; Fig. 2(b) is a section of an essential part taken along line B - B' of Fig. 1; and Fig. 2(c) is a section of an essential part taken along line C - C' of Fig. 1.

Throughout all the modes (embodiments) of the invention, the semiconductor chip is sealed in a resin-sealed type package of TSOP structure. The resin-sealed type package of this kind adopts an LOC (Lead On Chip) structure in which inner lead portions 3A are arranged over a rectangular semiconductor chip 1, as shown in Fig. 1.

The inner lead portions 3A are integral at their one ends with outer lead portions 3B. Signals applied to the outer lead portions 3B conforms to the standards individually and the outer lead portions 3B are correspondingly numbered. In Fig. 1, the upper lefthand end is a 1st terminal, and the lower lefthand end is a 16th terminal. The lower righthand end is a 17th terminal, and the upper righthand end is a 32th

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terminal. In short, the package of the present TSOP structure has 32 terminals.

The 1st, 7th and 16th terminals are for the power voltage Vcc such as the operating voltage of 5 volts (V) or 3 volts (V) of the circuit. The 17th, 27th and 32nd terminals are for the reference voltage Vss of 0 volts (V), for example.

The inner lead portions 3A each includes, as shown in Figs. 1 and 2, a plurality of signal line inner leads (first regions) $3A_1$ and two bus-bar leads (second regions) $3A_2$. The bus-bar leads are leads for feeding the power voltage and the reference voltage to the semiconductor chip and will also be referred to as the "fixed potential leads".

The plurality of signal line inner leads $3A_1$ are extended across the individual long sides of the rectangule of the semiconductor chip 1 to the center side of the semiconductor chip 1.

The signal line inner leads (the first regions) $3A_1$ are arranged, as shown in Fig. 2, over the major face (the major face of the semiconductor substrate, over which the circuit and a plurality of external terminals are formed) of the semiconductor chip 1, at predetermined spacings S (predetermined distances) between the major face and inner leads $3A_{12}$, which are

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made thinner than the other portions of the inner leads $3A_1$.

The leading end portions $3A_{11}$ of the thinned signal line inner leads (the first regions) $3A_{12}$ are fixed to the major face of the semiconductor chip 1 through an insulating film 4, as shown in Fig. 1 and Figs. 2(b) and 2(c).

The individual leading end portions $3A_{11}$ of the plurality of signal line inner leads $3A_1$ are individually connected through bonding wires 5 to bonding pads (the external terminals) 1A arrayed at the central portion of the semiconductor chip 1.

The two bus-bar leads $3A_2$ are formed over the major face of the semiconductor chip 1, as shown in Fig. 1, each include portions $3A_{21}$ arranged substantially in parallel with the long sides of the chip 1, and projections $3A_{22}$ arranged substantially in parallel with the short sides of the chip 1 and having regions to which the bonding wires 5 are bonded, and are made integrally of the same material. At the portions $3A_{21}$ of the bus-bar leads $3A_2$, the projections $3A_{22}$ are made integral with the portions $3A_{21}$ at a plurality of predetermined positions. These projections $3A_{22}$ are fixed with the insulating film 4. The portions $3A_{21}$ are so arranged low by forming steps

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D as to be closer to the major face of the chip 1 than the projections $3A_{22}$. By the steps, it is possible to prevent the bus-bars and the wires 5 for the signal leads from contacting. The object of bonding the wires 5 to the projections $3A_{22}$ is to make uniform the lengths, bondability and electric characteristics of the wires.

The leading end portions $3A_{11}$ of the signal inner leads $3A_{12}$ and the bonding pads 1A of the semiconductor chip 1, and the projections $3A_{22}$ formed at the parallel portions $3A_{21}$ of the bus-bar leads $3A_2$ and the bonding pads 1A of the semiconductor chip 1 are bonded respectively by the bonding wires 5 and are electrically connected. The semiconductor chip 1, the inner lead portions 3A and the bonding wires 5 are sealed with a mold resin (sealing body) 2A. A package 2 of this sealed TSOP structure is shaped by cutting suspension leads (chip supporting leads) 3C and the outer lead portions 3B from the lead frame. In this embodiment, the portions $3A_{21}$ are close to the chip major face, but not bonded with adhesive or the like. The insulating tape 4 has a structure in which an epoxy or polyimide adhesive is applied to both sides of a base made of a polyimide resin.

The bonding wires 5 may be gold wires. The

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method of forming the wires 5 may be the nail head bonding method of the ultrasonic thermocompression bonding method. These gold wires may be replaced by aluminum wires, copper wires or the coated wires which are prepared by coating the surfaces of metal wires with an insulating resin.

The dimensions of the essential portion of the resin sealed type semiconductor device of Mode 1 are as follows, as shown in Fig. 2 (the unit is millimeter: mm), the thickness of the resin-sealed type semiconductor device is 0.5 to 0.6 mm, the thickness of the mold resin (the sealing body) over the inner lead portions 3A on the major face of the semiconductor chip 1 is 0.06 to 0.11 mm, and the thickness of the sealer 2A below the face opposed to the major face of the semiconductor chip 1 is 0.06 to 0.11 mm, the thickness of the sealer 2A over the crests of the bonding wires 5 is 0.07 mm or more (the minimum value is 0.07 mm).

The thickness of the semiconductor chip 1 is 0.2 to 0.28 mm; the thickness of the portions $3A_{21}$, arranged over the major face of the semiconductor chip 1, of the bus-bar leads $3A_2$ is 0.06 to 0.07 mm; the thickness of the signal inner leads $3A_{12}$ is 0.06 to 0.07 mm; the thickness of the insulating film 4 is

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0.05 mm; and the thicknesses of the inner lead portions 3A and the outer lead portions 3B are individually about 0.125 mm.

Next will be briefly described the assembling steps of arranging the inner lead portions 3A over the major face of the semiconductor chip 1.

Assembling Steps:

①: Preparing a flat frame which includes the inner lead portions 3A having the plurality of signal line inner leads $3A_1$ and the two bus-bar leads $3A_2$, and the outer lead portions 3B integrated with the inner lead portions 3A;

②: Sticking the insulating tape 4 to the plurality of signal line inner leads $3A_1$ of the inner lead portions 3A, and shaping the two bus-bar leads $3A_2$ to form the steps D;

③: Positioning the lead frame over the semiconductor chip 1 in such a way that the plurality of signal line inner leads $3A_1$ are extended across the individual long sides of the rectangle of the semiconductor chip 1 and to the center side of the semiconductor chip 1 (see Figs. 1 and 2); and

④: After this positioning, performing a heat treatment (at 400°C for 1 sec.) so as to bond the major face of the semiconductor chip 1 and the lead

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frame through the insulating tape.

Here will be later described the forming method of making the inner leads $3A_{12}$ thinner than the other portions of the inner leads $3A_1$. The steps of the leads may be formed before the tape is stuck. The insulating tape 4 is given a structure in which a thermoplastic polyimide adhesive having a thickness of 0.015 mm is applied to both sides of a thermoplastic polyimide tape having a thickness of 0.03 mm, and the adhesive has a thickness of about 0.05 mm as a whole.

In the resin-sealed type semiconductor device of the TSOP structure shown in Fig. 24(a): the thickness of the resin-sealed type semiconductor device is 1.0 mm; the thickness of the mold resin (the sealing body) over the inner lead portion 3A is 0.06 to 0.11 mm; the thickness of the mold resin (the sealing body) below the face, opposed to the major face, of the semiconductor chip 1 is 0.32 mm; the thickness of the mold resin (the sealing body) 2A over the crests of the bonding wires 5 is 0.07 mm or more (the minimum value is 0.07 mm); the thickness of the semiconductor chip 1 is 0.28 mm; the thickness of the bus-bar leads $3A_2$ is 0.125 mm; the individual thicknesses of the signal inner leads $3A_1$ and the outer leads 3B are 0.125 mm; and the thickness of the insulating film 4

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is 0.08 mm.

In Mode 1, as seen from Figs. 2 and 24(a), over the major face of the semiconductor chip 1, there are provided predetermined spacings S between the major face and the inner leads $3A_{12}$, which are made thinner than the other portions of the inner leads $3A_1$. As a result, the semiconductor package 2 can be made thin without causing short-circuit between the bonding wires 5 of the signal lines and the bus-bar leads $3A_2$, even if an insulating coating material 20 is not applied to the bus-bar leads $3A_{21}$. Since the upper faces of the inner leads $3A_{11}$ to which the wires are connected can be lowered, moreover, the heights of the wire loops can be lowered to reduce the thickness of the package. The thicknesses of the outer leads are made thicker than the inner leads $3A_{12}$ in such a way that a mechanical strength strong enough to prevent deformation of the leads, as might otherwise be caused by an undesired external force applied from the outside of the package, and to support the weight of the package, when the package is surface-mounted. Consequently, the reliability of the package can be improved.

Even if the semiconductor package 2 is made thin, moreover, the parasitic capacitance can be reduced to

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speed up the operation of the resin-sealed type semiconductor device by providing predetermined spacings S through the insulating film 4 (the thickness is 0.05 mm) between the major face of the semiconductor chip 1 and the inner lead portions 3A.

Even if the semiconductor package 2 is made thin, moreover, it is possible to ensure a proper thickness (about 0.06 to 0.11 mm) of the sealer over the major face of the semiconductor chip 1 of the semiconductor package 2.

By making the inner leads $3A_{12}$ thinner than the other portions of the inner leads $3A_1$, moreover, the sealers over and under the semiconductor chip 1 can be balanced in quantity by bringing the projections of the outer lead portions 3B closer to the central portion in the thickness direction of the semiconductor package 2, even though this semiconductor package 2 is thinned. This makes it possible to prevent the semiconductor package 2 from being warped because of thermal expansion. At this time, it is preferable that the lower faces of the inner leads $3A_1$, not arranged over the chip 1, be positioned below the major face of the semiconductor chip 1.

In Mode 1, moreover, in place of the insulating

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film 4, adhesive may be employed to bond the leading end portions $3A_{11}$ of the inner leads to the major face of the chip. Though the parasitic capacitance between the chip and the leads increases, the leading end portions $3A_{11}$ can be lower by the thickness of the base of the insulating film 4, so that the wire loops can be lowered. As a result, it is possible to thin the package as a whole. This package is suited especially for such flash memories whose operating speeds, do not need to be relatively high.

(Mode 2)

Fig. 3 is a schematic top plan view showing the construction of a resin-sealed type semiconductor device of Mode 2 of the invention; Fig. 4 is a section of an essential part taken along line A - A' of Fig. 3; Fig. 5 is an enlarged view of a part enclosed by a circle M of Fig. 4; and Fig. 6 is a section of an essential part taken along line B - B' of Fig. 3.

In a resin-sealed type semiconductor device of Mode 2, as shown in Figs. 3 to 6, the portions $3A_{21}$, arranged substantially in parallel with the long sides of the semiconductor chip 1, of the bus-bar leads $3A_2$ are fixed directly with adhesive 6. The plurality of signal line inner leads $3A_1$ are lifted at their leading ends $3A_{11}$ from the chip major face, and no

insulating film is interposed to provide spacings (distance of 0.05 mm) S between the major face of the semiconductor chip 1 and the thinned portions $3A_{12}$ of the plurality of signal line inner leads $3A_1$. The adhesive 6 employed is, e.g., a thermoplastic polyimide adhesive. This adhesive 6 has a thickness of about 0.01 mm after applied.

As shown in Fig. 4, the plurality of signal inner leads $3A_1$ are electrically connected to the semiconductor chip 1 by bonding the bonding wires (gold wires) 5 directly to the bonding pads 1A on the major face of the semiconductor chip 1. Specifically, the semiconductor chip 1 and the signal line inner leads $3A_1$ are electrically connected by pressing the lifted thin portions A_{12} of the signal line inner leads $3A_1$ to the major face of the semiconductor chip 1 by a lead frame presser to bond the bonding wires 5 to the leading end portions $3A_{11}$ and by bonding the other ends of the bonding wires 5 to the bonding pads 1A on the major face of the semiconductor chip 1.

Likewise, as shown in Fig. 6, the protrusions $3A_{22}$ and the joints $3A_{21}'$ of the bus-bar leads $3A_2$ and the bonding pads 1A on the major face of the semiconductor chip 1 are individually bonded by the bonding wires 5 to connect the semiconductor chip 1 and the bus-bar

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leads $3A_2$ electrically. After this, they are sealed with the sealer (resin) 2A.

The bonding pads 1A on the major face of the semiconductor chip 1 have a structure in which an insulating oxide film $1B_2$ is formed on an inner electrode $1B_1$ on an Si substrate 1B and in which there are sequentially formed thereover a first tungsten (W) alloy $1B_3$, a second tungsten (W) alloy $1B_4$, an aluminum (Aℓ) alloy $1B_5$, a first titanium (Ti) alloy $1B_6$, a second titanium (Ti) alloy $1B_7$, a first insulating oxide film $1B_8$, a second insulating film $1B_9$ and a PiQ $1B_{10}$. Moreover, a hole is formed to expose the face of the aluminum (Aℓ) alloy $1B_5$ to the outside.

Even if the inner lead portions 3A is fixed to the major face of the semiconductor chip 1 directly with the adhesive 6, the insulating polyimide resin (PiQ) is formed at the uppermost layer of the major face of the semiconductor chip 1, as shown in Fig. 5, so that the insulation of the portions other than inner lead portions 3A and the bonding pads 1A of the semiconductor chip 1 can be ensured.

Here will be briefly described the assembling steps of arranging the inner lead portions 3A over the major face of the semiconductor chip 1 of the resin-sealed type semiconductor device of Mode 2.

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Assembling Steps:

①: Preparing a flat frame having a plurality of leads 3;

②: Applying adhesive 6 to the two bus-bar leads $3A_2$, and shaping the lead frame to form the steps D. Here, the adhesive 6 may be applied after the step formation;

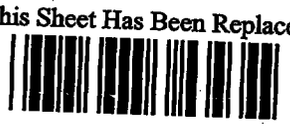
③: Over the semiconductor chip 1, positioning the lead frame in such a way that the plurality of signal line inner leads $3A_1$ may extend across the individual long sides of the rectangle of the semiconductor chip 1 and to the center side of the semiconductor chip 1 (see Fig. 3); and

④: After this positioning, bonding the chip and the lead frame with the adhesive 6.

Fig. 7 is a diagram for explaining a method for bonding the bonding wires 5 to the signal line inner leads. Fig. 7(a) shows the state before the wire bonding; Fig. 7(b) shows the state in the wire bonding; and Fig. 7(c) shows the state after the wire bonding. Numeral 21 designates a stage, and numeral 22 designates a lead frame presser.

In a method of bonding the bonding wires 5 by pressing the listed leading end portion $3A_{11}$ of the signal line inner lead $3A_1$ to the major face of the

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semiconductor chip 1, as shown in Fig. 7(a), the semiconductor chip 1 is disposed over the stage 21 to position the lifted leading end portion $3A_{11}$ of the signal line inner lead $3A_1$. Next, as shown in Fig. 7(b), after the positioning of the inner lead, the lead frame presser 22 is lowered, but the stage 21 is raised to bond the bonding wire 5 to the leading end portion $3A_{11}$ while pressing the signal line inner lead $3A_1$ to the major face of the semiconductor chip 1 over the stage 21. After this, as shown in Fig. 7(c), the lead frame presser 22 is raised, but the stage 21 is lowered to release the pressing force thereby to return the leading end portion $3A_{11}$ of the signal line inner lead $3A_1$ to the lifted state.

Fig. 8 is a diagram for explaining another method for bonding the bonding wire 5 to the signal line inner lead. Fig. 8(a) shows the state before the wire bonding; Fig. 8(b) shows the state in the wire bonding; and Fig. 8(c) shows the state after the wire bonding. In another method of bonding the bonding wire 5 to the signal line inner lead, as shown in Fig. 8(a), the semiconductor chip 1 is disposed over the fixed stage 21 to position the lifted leading end portion $3A_{11}$ of the signal line inner lead $3A_1$. Next, as shown in Fig. 8(b), after the positioning of the

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inner lead, the lead frame presser 22 is lowered to bond the bonding wire 5 to the leading end portion $3A_{11}$ while pressing the signal line inner lead $3A_1$ on the major face of the semiconductor chip 1 over the stage 21. After this, as shown in Fig. 8(c), the lead frame presser 22 is raised to release the pressing force thereby to return the leading end portion $3A_{11}$ of the signal line inner lead $3A_1$ to the lifted state.

In Mode 2, the portions $3A_{21}$, arranged substantially in parallel with the long sides of the semiconductor chip 1, of the bus-bar leads $3A_2$ are fixed directly with the adhesive 6 in such a way that the plurality of signal line inner leads $3A_1$ are lifted at their leading ends, no insulating film is interposed and the spacings (the distances are 0.05 mm) S are provided between the major face of the semiconductor chip 1 and the plurality of signal line inner leads $3A_1$. As a result, the parasitic capacitance can be reduced to achieve effects similar to those of Mode 1. Moreover, the insulating film 4 (having the thickness of 0.05 mm) is not interposed between the major face of the semiconductor chip 1 and the inner lead portions 3A, so that the manufacture steps and cost can be accordingly reduced.

(Mode 3)

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Fig. 9 is a schematic top plan view showing the construction of a resin-sealed type semiconductor device of Mode 3 of the invention, and Fig. 10 is a section of an essential part taken along line A - A' of Fig. 9.

In the resin-sealed type semiconductor device of Mode 3, as shown in Figs. 9 and 10, the invention is applied to the case in which the portions $3A_{21}$ arranged substantially in parallel with the long sides of the semiconductor chip 1, of the bus-bar leads $3A_2$ of the inner lead portions 3A of Mode 1 are not used. The structure of the other portions is identical to that of Mode 1.

Here will be briefly described the assembling steps of arranging the inner lead portions 3A over the major face of the aforementioned semiconductor chip 1.

Assembling Steps:

①: Preparing a flat frame having the insulating film 4;

②: Over the semiconductor chip 1, positioning the lead frame in such a way that the plurality of signal line inner leads $3A_1$ may extend to the center side of the semiconductor chip 1 (see Figs. 9 and 10); and

③: After this positioning, bonding the lead frame to the major face of the semiconductor chip 1 through the

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insulating film 4.

With this construction, it is possible to achieve effects similar to those of Mode 1. Since the bus-bar leads $3A_2$ are not employed, moreover, the manufacture steps and cost can be accordingly reduced.

(Mode 4)

Fig. 11 is a schematic top plan view showing the construction of a resin-sealed type semiconductor device of Mode 4 of the invention, and Fig. 12 is a section of an essential part taken along line A - A' of Fig. 11.

In the resin-sealed type semiconductor device of Mode 4, as shown in Figs. 11 and 12, the leading ends $3A_{11}$ of the plurality of signal line inner leads $3A_1$ of Mode 3 are fixed to the major face of the semiconductor chip 1 directly with the adhesive 6, and no insulating film 4 is interposed, the spacings (the distances are 0.05 mm) for reducing the parasitic capacitance are provided between the major face of the semiconductor chip 1 and the plurality of signal line inner leads $3A_{12}$.

Here will be briefly described the assembling steps of arranging the inner lead portions 3A over the major face of the aforementioned semiconductor chip 1 of the resin-sealed type semiconductor device of Mode

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4.

Assembling Steps:

①: Preparing a frame which are worked to form a step and of which the leading ends $3A_{11}$ of the inner lead portions 3A are coated with the adhesive 6.

②: Over the semiconductor chip 1, positioning the lead frame in such a way that the plurality of signal line inner leads $3A_1$ may extend to the center side of the semiconductor chip 1 (see Figs. 11 and 12); and

③: After this positioning, bonding the major face of the semiconductor chip 1 and the lead frame through the adhesive 6.

With this construction, it is possible to achieve effects similar to those of Mode 3. Since the bus-bar leads $3A_2$ and the insulating film 4 are not employed, moreover, the manufacture steps and cost can be accordingly reduced.

(Mode 5)

Fig. 13 is a schematic top plan view showing a construction of a resin-sealed type semiconductor device of Mode 5 of the invention, Fig. 14 is a section of an essential part taken along line A - A' of Fig. 13; and Fig. 15 is a section of an essential part taken along line B - B' of Fig. 14.

In the resin-sealed type semiconductor device

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Mode 5, as shown in Figs. 13 and 14, the portions $3A_{21}$, arranged substantially in parallel with the major face of the semiconductor chip 1, of the bus-bar leads $3A_2$ are fixed directly with the adhesive 6. The individual leading ends of the plurality of signal line inner leads $3A_1$ are fixed to the major face of the semiconductor chip 1 directly with the adhesive 6, and the spacings (the distances are 0.05 mm) for ensuring the proper capacitance are provided without any insulating film between the major face of the semiconductor chip 1 and the plurality of signal line inner leads $3A_1$.

Here will be briefly described the assembling steps of arranging the inner lead portions 3A over the major face of the semiconductor chip 1 of the resin-sealed type semiconductor device Mode 5.

Assembling Steps:

①: Preparing a flat frame, and shaping the frame to form steps D;

②: Applying adhesive to the portions $3A_{21}$, arranged substantially in parallel with the long sides of the semiconductor chip 1, of the bus-bar leads $3A_2$, the projections A_{22}, and the leading end portions $3A_{12}$ of the plurality of signal line inner leads $3A_1$;

③: Over the semiconductor chip 1 of the lead frame,

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positioning the portions $3A_{21}$, arranged substantially in parallel with the long sides of the semiconductor chip 1, of the bus-bar leads $3A_2$ in such a way that the leading end portions $3A_{11}$ of the plurality of signal line inner leads $3A_1$ may extend to the center side of the semiconductor chip 1 (as shown in Fig. 15); and

④: After this positioning, bonding the lead frame to the major face of the semiconductor chip 1 with the adhesive 6 (see Figs. 14 and 15).

After this bonding, the semiconductor chip 1 and the signal line inner leads $3A_1$ are electrically connected by bonding the one ends of the bonding wires 5 to the leading end portions $3A_{11}$ of the inner leads $3A_{12}$ and by bonding the other ends of the bonding wires 5 to the bonding pads 1A on the major face of the semiconductor chip 1. Likewise, the semiconductor chip 1 and the bus-bar leads $3A_2$ are electrically connected by connecting the portions $3A_{22}$ integrated with the portions $3A_{21}$ arranged substantially in parallel with the long sides of the semiconductor chip 1, and the bonding pads 1A on the major face of the semiconductor chip 1 through the bonding wires 5. After this, they are sealed with the resin 2A by a transfer mold method.

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With this construction, it is possible to achieve effects similar to those of Mode 1. Since the insulating film 4 is not used, moreover, it is possible to reduce the manufacture steps and cost. Since the leading end portions $3A_{11}$ of the signal inner leads $3A_1$ are arranged closer to the chip major face, moreover, it is possible to lower the levels of the wire loops.

In Modes 1 to 5, the thinned portions $3A_{11}$ and $3A_{12}$ of the signal line inner leads $3A_1$ and the thinned portions $3A_{21}$ and $3A_{21}'$ of the bus-bar leads $3A_2$ are formed by half-etching or coining the back faces of the inner lead portions which are provided in the area H (of a slightly larger rectangular shape than the chip) enclosed by a broken line in Fig. 16.

The external leads (outer leads) are worked into a J-bend (letter J) shape, as shown in Fig. 17(a), and are worked, if necessary, into a flat shape, as shown in Fig. 17(b), an inverted L shape, as shown in Fig. 17(c), or a Z shape, as shown in Fig. 17(d).

Here, the structure of the foregoing Modes having one semiconductor chip 1 of one layer have been described, but the thin resin-sealed type semiconductor device of the invention can also be applied to the case in which two or more semiconductor

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chips or semiconductor packages are stacked to increase the storage capacity.

(Mode 6)

Fig. 18 is a schematic top plan view showing a construction of a semiconductor storage module of Mode 6 of the invention, and Fig. 19 is a side elevation of Fig. 18. Reference numeral 30 designates a mounting board; numeral 31 a stack in which two semiconductor storage devices such as DRAMs are stacked; numeral 32 a chip capacitor; and numeral 33 the terminals of the semiconductor storage module. Any of the packages of Modes 1 to 5 can be applied to the individual packages constituting the stack 31.

In the semiconductor storage module of Mode 6, as shown in Figs. 18 and 19, eight stacks 31, in which two semiconductor storage devices such as DRAMs are individually stacked, are mounted on both sides of the board 30. The chip capacitors 32 are mounted on one peripheral portion of the plane of the mounting board 30, and the terminals 33 of the semiconductor storage module are mounted on one edge face of the mounting board 30. With this construction, it is possible to provide a small-sized large-capacity thin semiconductor storage module. The thicknesses of the stacks 31 are about 1.2 to 1.3 mm at the maximum.

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(Mode 7)

Fig. 20 is a schematic top plan view showing the construction of an electronic device of Mode 7 of the invention. Fig. 20(a) shows a top plan view of one face, Fig. 20(b) shows a top plan view of the other face, and Fig. 21 is a side elevation of Fig. 20. In Figs. 20 and 21, numeral 34 designates a QFP in which a microcomputer is mounted; numeral 35 a QFP in which a driver IC is mounted; and numeral 36 a stack in which two semiconductor storage devices such as flash memories are stacked. Any of the packages of Modes 1 to 5 are applied to the individual packages constituting the stack 36.

In the semiconductor storage module of Mode 7, as shown in Figs. 20 and 21, there are mounted on one face (front face) of the board 30, three stacks 36 in which semiconductor storage devices such as flash memories are stacked, a microcomputer (QFP) 34, a driver (QFP) 35 and chip capacitors 32, and there are mounted on the other face (back face) eight stacks 36 in each of which two semiconductor storage devices such as flash memories are stacked, and chip capacitors 32. With this construction, it is possible to provide an electronic device of a small size having a large storage capacity. As a result, it is possible

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to provide an electronic card capable of processing massive information highly accurately. The thicknesses of the stacks 36 are 1.2 to 1.3 mm at the maximum, which are substantially equal to those of the QFPs 34 and 35.

Although our invention has been specifically described in conjunction with its Modes, it should not be limited thereto but can naturally be modified in various manners without departing from the gist thereof.

The effects of the representatives of the inventions disclosed herein will be briefly described in the following.

(1) In the resin-sealed type semiconductor device having the bus-bar leads, the signal inner leads (the first regions of the inner lead portions) are so arranged over the major face of the semiconductor chip as to provide predetermined spacings between the major face and the inner leads, and portions of the inner leads are made thinner than those of the other portions. As a result, even if no insulating coating material is applied to the bus-bar leads, the thickness of the semiconductor package can be thinned without causing any short-circuit between the signal line bonding wires and the bus-bar leads.

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(2) In the resin-sealed type semiconductor device having the bus-bar leads, even if the semiconductor package is thinned, a proper capacitance can be ensured by sandwiching the insulating film between the major face of the semiconductor chip and the inner lead portions to provide predetermined spacings. As a result, the electric characteristics can be achieved by the proper capacitance of the resin-sealed type semiconductor device.

(3) In the resin-sealed type semiconductor device having the bus-bar leads, even if the semiconductor package is thinned, it is possible to ensure a proper thickness for the sealer over the major face of the semiconductor chip of the semiconductor package.

(4) In the resin-sealed type semiconductor device having the bus-bar leads, even if the semiconductor package is thinned, the upper and lower sealers of the semiconductor chip can be balanced by bringing the projections of the outer leads closer to the central portion in the direction of the thickness of the semiconductor package. As a result, it is possible to prevent warpage which might otherwise be caused by the difference in the coefficients of thermal expansion of the semiconductor package.

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(5) In the resin-sealed type semiconductor device having the bus-bar leads, the signal inner leads (the first regions of the inner lead portions) are so arranged over the major face of the semiconductor chip as to provide predetermined spacings between the major face and the inner leads, and only the bus-bar leads are directly fixed to the major face of the semiconductor chip with adhesive. As a result, the manufacture steps and cost can be reduced correspondingly to the disuse of the insulating film.

(6) In the resin-sealed type semiconductor device not having bus-bar leads, the signal inner leads are so arranged over the major face of the semiconductor chip as to provide predetermined spacings between the major face and the inner leads, and the portions of the inner leads are made thinner than those of the other portions and fixed at their leading end portions to the major face of the semiconductor chip through the insulating film. This ensures the insulation between the semiconductor chip and the leads.

(7) In the resin-sealed type semiconductor device not having bus-bar leads, even if the semiconductor package is thinned, a proper capacitance can be ensured by interposing the insulating film

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between the major face of the semiconductor chip and the inner lead portions to provide predetermined spacings. As a result, the electric characteristics can be achieved by the proper capacitance of the resin-sealed type semiconductor device. As a result, the manufacture steps and cost can be reduced correspondingly to the disuse of the insulating film.

(8) In the resin-sealed type semiconductor device not having bus-bar leads, even if the semiconductor package is thinned, it is possible to ensure a proper thickness for the sealer over the major face of the semiconductor chip of the semiconductor package.

(9) In the resin-sealed type semiconductor device not having bus-bar leads, the predetermined spacings are provided not by interposing the insulating film between the major face of the semiconductor chip and the inner lead portions, and only the leading end portions of the inner lead portions are fixed to the major face of the semiconductor chip directly with adhesive. However, the uppermost layer of the major face of the semiconductor chip is the insulating film capable of ensuring the insulation between the semiconductor chip and the leads. As a result, the manufacture steps and

cost can be reduced correspondingly to the disuse of the bus-bar leads and the insulating film.

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WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor chip including a circuit and a plurality of external terminals formed over a major face thereof,

a plurality of leads each including an inner lead portion and an outer lead portion formed integrally with said inner lead portions,

bonding wires electrically connecting said external terminals and said inner lead portions respectively, and

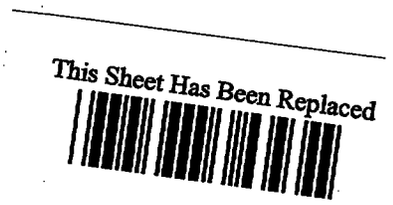
a resin member for sealing said semiconductor chip, said inner lead portions and said bonding wires,

wherein said inner lead portions are arranged over the major face of said semiconductor chip at predetermined spacings between said major face and said inner leads, and

wherein the portions of the inner leads arranged over said major face are thinner than the other portions of said inner leads.

2. A semiconductor device according to Claim 1,

wherein the portions, arranged over the major face of said semiconductor chip, of said inner lead



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portions are fixed at their leading end portions to the major face of said semiconductor chip through an insulating film.

3. A semiconductor device according to Claim 1, wherein the portions, arranged over the major face of said semiconductor chip, of said inner lead portions are fixed at their leading end portions to the major face of said semiconductor chip directly with adhesive.

4. A semiconductor device comprising:

a semiconductor chip including a circuit and a plurality of external terminals formed over a major face of a semiconductor substrate,

a plurality of leads each including an inner lead portion having a first region, and an inner lead portion having a second region and an outer lead portion formed integrally with said inner lead portions,

bonding wires electrically connecting said external terminals and the first regions and the second regions of said inner lead portions respectively, and

a resin member for sealing said semiconductor

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chip, said inner lead portions and said bonding wires,

wherein the first regions and the second regions of said inner lead portions are arranged over the major face of said semiconductor chip,

wherein the first regions of said inner lead portions are arranged at predetermined spacings between said major face and said inner leads,

wherein the portions of the inner leads arranged over said major face are thinner than the other portions of said inner leads, and

wherein the inner leads arranged over said major face are fixed at their leading end portions to the major face of said semiconductor chip through an insulating film.

5. A semiconductor device according to Claim 4,

wherein said semiconductor chip is rectangular,

wherein the second regions of said inner lead portions have portions arranged substantially in parallel with the long sides of said semiconductor chip, and

wherein said parallel-arranged portions are arranged between said external terminals and the leading end portions of said inner leads.

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6. A semiconductor device comprising:

a semiconductor chip including a circuit and a plurality of external terminals formed over the major face of a semiconductor substrate,

a plurality of leads each including an inner lead portion having a first region, and an inner lead portion having a second region and an outer lead portion formed integrally with said inner lead portions,

bonding wires electrically connecting said external terminals and the first regions and the second regions of said inner lead portions respectively, and

a resin member for sealing said semiconductor chip, said inner lead portions and said bonding wires,

wherein the first regions and the second regions of said inner lead portions are arranged over the major face of said semiconductor chip,

wherein the first regions of said inner lead portions are arranged at predetermined spacings between said major face and said inner leads, and

wherein the portions of the inner leads arranged over said major face are thinner than the other portions of said inner leads but are not fixed at their leading end portions to the major face of said

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semiconductor chip.

7. A semiconductor device according to Claim 4 or 6, wherein the first regions of said inner lead portions are signal leads whereas said second regions are fixed potential leads.

8. A semiconductor device comprising:

a semiconductor chip including an integrated circuit and a plurality of external terminals formed over a major face of said semiconductor chip,

a plurality of leads each including an inner lead portion and an outer lead portion formed integrally with said inner lead portions, portions of said inner lead portions being arranged over the major face of said semiconductor chip and electrically connected to the corresponding external terminals, and

a resin member for sealing the inner lead portions of said plurality of leads and said semiconductor chip,

wherein said inner lead portions each include a first surface on the major face side of said semiconductor chip, a second surface on the opposite side to said first surface, a first portion positioned over the major face of said semiconductor chip and a



second portion formed integrally with said first portion and positioned outside the major face of said semiconductor chip,

wherein the first portions of said inner lead portions are made thinner than said second portions in the thickness direction of said semiconductor chip, and

wherein the first surfaces of the first portions of said inner lead portions are more spaced from said semiconductor chip in the thickness direction of said semiconductor chip than the first surfaces of the second portions of said inner lead portions.

9. A semiconductor device according to Claim 8, wherein the first portions of said inner lead portions are bonded to the major face of said semiconductor chip through an insulating film.

10. A semiconductor device according to Claim 8, wherein the first portions of said inner lead portions are bonded to the major face of said semiconductor chip through adhesive.

11. A semiconductor device according to Claim 8, wherein said inner lead portions and the

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corresponding external terminals are connected through wires.

12. A semiconductor device according to Claim 11,

wherein said plurality of leads include signal leads and fixed potential leads,

wherein the inner lead portions of said fixed potential leads are partially arranged over the major face of said semiconductor chip between said plurality of external terminals of the leading ends of the inner lead portions of said signal leads, and

wherein the wires connecting the inner lead portions of said signal leads and the corresponding external terminals are so arranged as to cross over portions of the inner lead portions of said fixed potential leads.

13. A semiconductor device comprising:

a semiconductor chip including an integrated circuit and a plurality of external terminals formed over a major face of the semiconductor chip,

a plurality of signal leads each including an inner lead portion and an outer lead portion formed integrally with said inner lead portions, portions of said inner lead portions being arranged over the major

face of said semiconductor chip and electrically connected to the corresponding external terminals through wires,

fixed potential leads each including an inner lead portion and an outer lead portion formed integrally with said inner lead portions, said inner lead portions being partially arranged over the major face of said semiconductor chip and electrically connected to the corresponding external terminals, and

a resin member for sealing the inner lead portions of said plurality of signal leads, the inner lead portions of said fixed potential leads, and said semiconductor chip,

wherein said inner lead portions of said signal leads each include a first surface on the major face side of said semiconductor chip, a second surface on the opposite side to said first surface, a first portion positioned over the major face of said semiconductor chip, and a second portion formed integrally with said first portions and positioned outside the major face of said semiconductor chip,

wherein the first portions of said inner lead portions of said signal leads are made thinner than said second portions in the thickness direction of said semiconductor chip,

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wherein the first surfaces of the first portions of said inner lead portions of said signal leads are more spaced from said semiconductor chip in the thickness direction of said semiconductor chip than the first surfaces of the second portions of said inner lead portions,

wherein the inner lead portions of said fixed potential leads are partially arranged over the major face of said semiconductor chip between the leading ends of the inner lead portions of said signal leads and said plurality of external terminals, and

wherein the inner lead portions of said fixed potential leads are partially arranged lower in the thickness direction of said semiconductor chip than the leading ends of the inner lead portions of said signal leads.

14. A semiconductor device according to Claim 13,

wherein the inner lead portions of said fixed potential leads are partially bonded to the major face of said semiconductor chip with adhesive,

wherein the inner lead portions of said signal leads are spaced at their leading ends from the major face of said semiconductor chip.

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15. A semiconductor device according to Claim 13, wherein the inner lead portions of said signal leads bonded at their leading ends to the major face of said semiconductor chip through an insulating film.

16. A semiconductor device according to Claim 13, wherein the wires for connecting the inner lead portions of said signal leads and the corresponding external terminals are so arranged as to cross over portions of the inner lead portions of said fixed potential leads.

17. A semiconductor device comprising:

a semiconductor chip including an integrated circuit and a plurality of external terminals formed over a major face of the semiconductor chip,

a plurality of signal leads each including an inner lead portion and an outer lead portion formed integrally with said inner lead portion, portions of said inner lead portions being arranged over the major face of said semiconductor chip and electrically connected to the corresponding external terminals through wires,

fixed potential leads each including an inner lead portion and an outer lead portion formed

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integrally with said inner lead portions, said inner lead portions being partially arranged over the major face of said semiconductor chip and electrically connected to the corresponding external terminals, and

a resin member for sealing the inner lead portions of said plurality of signal leads, the inner lead portions of said fixed potential leads, and said semiconductor chip,

wherein said inner lead portions of said signal leads each includes a first surface on the major face side of said semiconductor chip, a second surface on the opposite side to said first surface, a first portion positioned over the major face of said semiconductor chip, and a second portion formed integrally with said first portion and positioned outside the major face of said semiconductor chip,

wherein the first portions of said inner lead portions of said signal leads are made thinner than said second portions in the thickness direction of said semiconductor chip,

wherein the first portions of said inner lead portions of said signal leads have leading end portions to be connected to said wires,

wherein the first surfaces of the first portions of said inner lead portions of said signal leads other

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than said leading end portions are more spaced from said semiconductor chip in the thickness direction of said semiconductor chip than the first surfaces of the second portions of said inner lead portions,

wherein the first portions of said inner lead portions of said signal leads are arranged lower in the thickness direction of said semiconductor chip than the first portions of said inner lead portions of said signal leads other than said leading end portions,

wherein the inner lead portions of said fixed potential leads are partially arranged over the major face of said semiconductor chip between the leading end portions of the first portions of the inner lead portions of said signal leads and said plurality of external terminals, and

wherein the inner lead portions of said fixed potential leads are partially arranged lower in the thickness direction of said semiconductor chip than the first portions of the inner lead portions of said signal leads other than said leading end portions.

18. A semiconductor device according to Claim 17,

wherein portions of the inner lead portions of said fixed potential leads and the leading end

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portions of the inner lead portions of said signal leads are bonded to the major face of said semiconductor chip with adhesive.

19. A semiconductor device according to Claim 17, wherein the wires connecting the inner lead portions of said signal leads and the corresponding external terminals are so arranged as to cross over portions of the inner lead portions of said fixed potential leads.

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