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(71) Applicant: INTEL CORPORATION [US/US]; 2625 Walsh Avenue, Santa Clara, CA 95051 (US).

(72) Inventors: STEVENS, Kenneth, S.; 3909 N.E. Jackson School Road, Hillsboro, OR 97124 (US). ROTEM, Shai; Morad – Hanahal Street 11, 40295 Hofit (IL). GINOSAR, Ran; 13870 S.W. 20th Street, Beaverton, OR 97008 (US).

(74) Agent: VIKSNINS, Ann, S.; Schwegman, Lundberg, Woessner & Kluth, P.O. Box 2938, Minneapolis, MN 55402 (US).

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(54) Title: CIRCUIT SYNTHESIS AND VERIFICATION USING RELATIVE TIMING

(57) Abstract

A system and method of synthesizing and/or verifying a circuit from a behavioral description of that circuit. A signal ordering of signals in the circuit is defined, wherein defining a signal ordering of signals in the circuit includes specifying a relative ordering of a plurality of events within the circuit. The behavioral description is modified as a function of the signal ordering. The circuit is then synthesized and/or verified as a function of the modified behavioral description.