SEMICONDUCTOR WAFER HAVING THROUGH-HOLE VIAS ON SAW STREETS WITH BACKSIDE REDISTRIBUTION LAYER

Field of the Invention

The present invention relates in general to semiconductor packaging and, more particularly, to stackable semiconductor die having through-hole vias formed along saw streets with backside redistribution layers.

Background of the Invention

Semiconductor devices are found in many products used in modern society. Semiconductors find applications in consumer items such as entertainment, communications, networks, computers, and household items markets. In the industrial or commercial market, semiconductors are found in military, aviation, automotive, industrial controllers, and office equipment.

The manufacture of semiconductor devices involves formation of a wafer having a plurality of die. Each die contains hundreds or thousands of transistors and other active and passive devices performing a variety of electrical functions. For a given wafer, each die from the wafer typically performs the same electrical function. Front-end manufacturing generally refers to formation of the

semiconductor devices on the wafer. The finished wafer has an active side containing the transistors and other active and passive components. Back-end manufacturing refers to cutting or singulating the finished wafer into the individual die and then packaging the die for structural support and/or environmental isolation.

Semiconductor manufacturers are increasingly adopting packaging techniques which involve three-dimensional (3D) interconnects between the semiconductor devices. The 3D interconnects provide advantages such as size reduction, reduced interconnect length, and integration of devices with different functionality into an overall 3D package. One way of implementing 3D interconnects involves the use of through-hole vias (THV). THVs are typically located around the perimeter of the die along its saw street guides. Most, if not all, semiconductor packages use the THVs to route signals between adjacent die. However, THVs alone limit signal routing options and reduce signal routing density. Present day high density packaging require high density and flexible interconnect capability, which is difficult to achieve through THVs.

A need exists to increase signal routing options and density in a semiconductor wafer having THVs.

Summary of the Invention

In one embodiment, the present invention is a method of making a semiconductor device comprising the steps of providing a plurality of semiconductor die with a plurality of contact pads disposed over a first surface of the semiconductor die, forming a trench between the semiconductor die, depositing an insulating material in the trench, forming a plurality of conductive vias through the insulating

material, forming a plurality of conductive traces over the first surface electrically connecting a first portion of the conductive vias to the contact pads, and forming an RDL over a second surface of the semiconductor die opposite the first surface. The RDL extends across the second surface of the semiconductor die to route electrical signals to areas on the second surface including a central region of the semiconductor die. A second portion of the conductive vias is electrically isolated from the conductive traces. The method further includes the step of forming a repassivation layer over the second surface of the semiconductor die for electrical isolation between portions of the RDL.

In another embodiment, the present invention is a method of making a semiconductor device comprising the steps of providing a plurality of semiconductor die with a plurality of contact pads disposed over a first surface of the semiconductor die, depositing an insulating material around the semiconductor die, forming a plurality of conductive vias through the insulating material, forming a plurality of conductive traces over the first surface electrically connecting a first portion of the conductive vias to the contact pads, and forming an RDL over a second surface of the semiconductor die opposite the first surface. A first portion of the RDL is electrically connected to the conductive vias and a second portion of the RDL is electrically isolated from the conductive vias. The method further includes the step of forming a repassivation layer over the second surface of the semiconductor die for electrical isolation between portions of the RDL.

In another embodiment, the present invention is a method of making a semiconductor device comprising the steps of providing a plurality of semiconductor die, depositing an insulating material around the semiconductor die, forming a

plurality of conductive vias through the insulating material, forming a plurality of conductive traces over a first surface of the semiconductor die electrically connecting the conductive vias to contact pads of the semiconductor die, and forming an RDL over a second surface of the semiconductor die opposite the first surface. A first portion of the RDL is electrically connected to the conductive vias.

In another embodiment, the present invention is a method of making a semiconductor device comprising the steps of providing a plurality of semiconductor die, depositing an insulating material around the semiconductor die, forming a plurality of conductive vias through the insulating material, forming a plurality of conductive traces over a first surface of the semiconductor die, and forming an RDL over a second surface of the semiconductor die opposite the first surface. A first portion of the RDL is electrically connected to the conductive vias.

Brief Description of the Drawings

FIGs. 1a-1b illustrate top and side views of a semiconductor wafer having a plurality of die separated by saw street guides;

FIGs. 2a-2b illustrate top and side views of the semiconductor wafer with cut saw street guides;

FIGs. 3a-3b illustrate top and side views of an expansion of the saw streets;

FIGs. 4a-4b illustrate top and side views of the expanded saw streets filled with organic material;

FIGs. 5a-5b illustrate top and side views of forming via holes through the organic material in the saw streets;

FIGs. 6a-6b illustrate top and side views of forming conductive traces between the contact pads and via holes;

FIGs. 7a–7b illustrate top and side views of depositing conductive material in the via holes;

FIGs. 8a–8b illustrate top and side views of forming backside redistribution layers and repassivation layers;

FIGs. 9a–9b illustrate top and side views of cutting the metal vias into two half-circle vias;

FIGs. 10a–10b illustrate top and side views of a semiconductor die with metal vias formed along the saw streets;

FIGs. 11a–11b illustrate top and side views of two side-by-side metal vias formed along the saw streets with redistribution layers on the backside of the die;

FIGs. 12a–12b illustrate top and side views of cutting the organic material between the two side-by-side metal vias to separate the die;

FIGs. 13a–13b illustrate top and side views of a semiconductor die with metal vias along the saw streets;

FIG. 14 illustrates die-to-die stacking using direct metal-to-metal via bonding;

FIG. 15 illustrates the semiconductor die with metal vias connected to a second die with solder bumps;

FIG. 16 illustrates the semiconductor die with metal vias connected to a second die with bond wires;

FIG. 17 illustrates another embodiment of interconnecting die using metal vias on saw streets and backside RDL; and

FIG. 18 illustrates another embodiment of interconnecting die using metal vias on saw streets and backside RDL.

Detailed Description of the Drawings

The present invention is described in one or more

embodiments in the following description with reference to the Figures, in which like numerals represent the same or similar elements. While the invention is described in terms of the best mode for achieving the invention's objectives, it will be appreciated by those skilled in the art that it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims and their equivalents as supported by the following disclosure and drawings.

The manufacture of semiconductor devices involves formation of a wafer having a plurality of die. Each die contains hundreds or thousands of transistors and other active and passive devices performing one or more electrical functions. For a given wafer, each die from the wafer typically performs the same electrical function. Front-end manufacturing generally refers to formation of the semiconductor devices on the wafer. The finished wafer has an active side containing the transistors and other active and passive components. Back-end manufacturing refers to cutting or singulating the finished wafer into the individual die and then packaging the die for structural support and/or environmental isolation.

A semiconductor wafer generally includes an active front side surface having semiconductor devices disposed thereon, and a backside surface formed with bulk semiconductor material, e.g., silicon. The active front side surface contains a plurality of semiconductor die. The active surface is formed by a variety of semiconductor processes, including layering, patterning, doping, and heat treatment. In the layering process, semiconductor materials are grown or deposited on the substrate by techniques involving thermal oxidation, nitridation, chemical vapor deposition, evaporation, and sputtering. Patterning involves use of

photolithography to mask areas of the surface and etch away undesired material to form specific structures. The doping process injects concentrations of dopant material by thermal diffusion or ion implantation. The active surface is substantially planar and uniform with electrical interconnects, such as bond pads.

Flip chip semiconductor packages and wafer level chip scale packages (WLP) are commonly used with integrated circuits (ICs) demanding high speed, high density, and greater pin count. Flip chip style packaging involves mounting an active area of the die facedown toward a chip carrier substrate or printed circuit board (PCB). The active area contains active and passive devices, conductive layers, and dielectric layers according to the electrical design of the die. The electrical and mechanical interconnect is achieved through a solder bump structure comprising a large number of individual conductive solder bumps or balls. The solder bumps are formed on the bump pads which are disposed on the active area. The bump pads connect to the active circuits by conduction tracks or traces in the active area. The solder bumps are electrically and mechanically connected to the contact pads on the carrier substrate by a solder reflow process. The flip chip semiconductor package provides a short electrical conduction path from the active devices on the die to conduction tracks on the carrier substrate in order to reduce signal propagation, lower capacitance, and achieve overall better circuit performance.

In the present discussion, a WLP is provided having through-hole vias (THV) formed along saw streets. The backside of the wafer has redistribution layers (RDL) for interconnect flexibility separated by repassivation layers. WLP with THV formed along saw streets are described in U.S. Patent Application Serial No. 11/744,657, entitled "Through-

Hole Via on Saw Streets", and further in U.S. Patent Application Serial No. 11/768,844, entitled "Package on Package Using Through-Hole Via Die on Saw Streets", which are incorporated herein by reference.

Turning to FIG. 1a, a semiconductor wafer 30 is shown having a plurality of die 32. The die are separated by inter die wafer area 36, commonly known as saw street guides. The saw street guides are routed around the wafer such that there is a saw street on every side of each die on the wafer, i.e., around a perimeter of the die. Each die 32 has a plurality to contact pads 38 formed on an active side of the die. Contact pads 38 are made of aluminum, copper, or aluminum/copper alloys. Contact pads 38 electrically connect to active and passive devices through conduction tracks or layers formed on die 32. The contact pads can be disposed side-by-side a first distance from the edge of the die, as shown in FIG. 1a. Alternately, the contact pads can be offset in multiple rows such that a first row of contact pads are disposed a first distance from the edge of the die, and a second row of contact pads alternating with the first row are disposed a second distance from the edge of the die. A solder bump or wire bond will later be formed to connect to each metal contact pad for electrical and mechanical interconnect to a chip carrier substrate or printed circuit board (PCB).

FIG. 1b is a cross-sectional view of wafer 30, taken along line 1b-1b in FIG. 1a, showing die 32 separated by saw street guides 36. In one embodiment, die 32 may have dimensions ranging from 2x2 millimeters (mm) to 15x15 mm. The saw streets provide cutting areas to singulate the wafer into individual die. A first die 32 is disposed to the left of the leftmost saw street 36. A second die 32 is disposed between the saw streets 36. A third die 32 is disposed to the right of the rightmost saw street 36. Once the wafer is singulated,

each set of contact pads disposed on the respective die will provide the electrical and mechanical interconnect for that die.

In FIG. 2a, semiconductor wafer 30 is again shown with its plurality of die 32, separated by saw street guides 36. Dicing tape 40 is applied to the back of semiconductor wafer 30 for structural support of the wafer during the following manufacturing operations, as shown in FIG. 2b which is a cross-sectional view taken along line 2b-2b in FIG. 2a. Saw streets 36 are cut by cutting tool 44. In one embodiment, cutting tool 44 can be a saw or laser. Note that the cutting tool completely severs through wafer 30 to form a well or trench 42. The bottom of trench 42 is defined by dicing tape 40. The formation of trench 42 arises from a first singulation of wafer 30, which creates a trench width that is less than a width of the channel of saw street guide 36.

In FIG. 3a, semiconductor wafer 30 is shown with its plurality of die 32, separated by cut saw street guides 36. Wafer 30 undergoes a wafer expansion step to increase the width of saw street guides 36. FIG. 3b is a cross-sectional view of wafer 30, taken along line 3b-3b, showing the die being pulled using a wafer expansion table as shown by directional arrows 46. Alternately, the die can be picked and placed onto a wafer support system. In any case, the die are positioned farther apart following the steps of FIGs. 3a-3b to create wider saw street guides. In one embodiment, the die separation increases from 50 micrometers (μm) to 200 μm. The expanded dimension depends on the design embodiment, i.e. half via, full via, single row via, or double/multiple row via.

In FIG. 4a, semiconductor wafer 30 is shown with its plurality of die 32, separated by cut saw street guides 36. Organic material 48 is deposited in trench 42 by spin-coating or needle dispensing. Organic material 48 can be

benzocyclobutene (BCB), polyimide (PI), or acrylic resin. FIG. 4b is a cross-sectional view of wafer 30, taken along line 4b-4b, showing organic material 48 deposited in trench 42. Organic material 48 fills trench 42 from dicing tape 40 up to the top surface of die 32.

In FIG. 5a, semiconductor wafer 30 is shown with its plurality of die 32, separated by saw street guides 36 filled with organic material 48. A via hole 50 is cut into organic material 48 along saw streets 36. The via cutting operation uses a laser drill or etching process. Via holes 50 are placed along die 32 adjacent to contact pads 38. In one embodiment, contact pads 38 and via holes 50 have a minimum separation distance of about 20 μm to 150 μm, depending on the diameter and depth of the via.

In FIG. 5b, the cross-sectional view of wafer 30, taken along line 5b-5b, shows via hole 50 cut into organic material 48 down to dicing tape 40. The laser drilling operation is centered about the channel of the saw street guide and makes a hole having a diameter less than the width of trench 42, which leaves a layer of organic material 48 surrounding via hole 50. The width of trench 42 is dependent on the width of saw street width, but typically smaller than the saw street width. The diameter of via hole 50 is typically about 10 μm to 100 μm, depending on the required via depth.

In FIG. 6a, semiconductor wafer 30 is shown with its plurality of die 32, separated by saw street guides 36 with via holes 50. A metal track or trace 52 is routed from each contact pad 38 to the corresponding via hole 50. Trace 52 is formed by a metal patterning process to connect contact pads 38 to via holes 50, which will be filled with conductive material in a later step. Traces 52 are provided for each contact pad and via hole pairing as shown. Some via holes 50

are dummy vias performing no electrical function. Accordingly, metal trace 52 need not be routed to every via depending on the device function. FIG. 6b is a cross-sectional view of wafer 30, taken along line 6b-6b, showing metal trace 52 connecting contact pad 38 to via hole 50.

In FIG. 7a, semiconductor wafer 30 is shown with its plurality of die 32, separated by saw street guides 36 with metal-filled vias 54. A conductive material is deposited into via hole 50 through a deposition process such as plating or plugging to form metal vias 54. The conductive material can be copper (Cu), aluminum (Al), tungsten (W), or alloys thereof, or mixtures of other conductive materials. Metal vias 54 are formed in and are surrounded by organic material 48. Metal via 54 electrically connects to contact pad 38 by way of trace 52. Traces 52 are provided for each contact pad and metal via pairing as shown. FIG. 7b is a cross-sectional view of wafer 30, taken along line 7b-7b, showing metal-filled via 54 electrically connecting to contact pad 38 through trace 52. The bottom of metal via 54 coincides with dicing tape 40.

In FIG. 8a, semiconductor wafer 30 is shown with its plurality of die 32, separated by saw street guides 36 with metal-filled vias 54. Dicing tape 40 is removed. Wafer 30 is inverted such that contact pads 38 and traces 52 are facing down, as shown in FIG. 8b which is a cross-sectional view of wafer 30 taken along line 8b-8b. Wafer support structure 56 is attached to the bottom side of wafer 30. Wafer support structure 56 can be made from glass, silicon substrate, or other material suitable for structurally supporting the wafer. A backside RDL 58 is formed on the backside of wafer 30. RDL 58 can be made with nickel (Ni), nickel vanadium (NiV), Cu, or Cu alloy. RDL 58 operates as an intermediate conductive layer to route electrical signals to various areas of the die, including active and passive circuits, and provides various

electrical interconnect options during package integration, such as shown in FIGs. 15-18. Repassivation layer 60 is formed between the individual nodes of backside RDL 58 for electrical isolation. The repassivation layer can be made with silicon nitride (SiN), silicon dioxide (SiO2), silicon oxynitride (SiON), polyimide, benzocyclobutene (BCB), polybenzoxazole (PBO), or other insulating material.

In FIG. 9a, semiconductor wafer 30 is shown with its plurality of die 32, separated by saw street guides 36 with its plurality of die 32 having contact pads 38 connected to metal vias 64 by traces 52. Wafer support structure 56 is removed. Wafer 30 is again inverted such that contact pads 38 and traces 52 are facing up, as shown in FIG. 9b which is a cross-sectional view of wafer 30 taken along line 9b-9b. Dicing tape 62 is attached to the bottom side of semiconductor wafer 30 for structural support of the wafer during the second or final singulation to separate die 32. Metal vias 54 are cut through center area 68 by cutting tool 70 as shown in FIG. 9b. In one embodiment, cutting tool 70 can be a saw or laser. The cut extends down through RDL 58 to dicing tape 62 to completely sever metal vias 54 into two equal half-circle vias 64. A pick and place operation removes die 32 as individual units from dicing tape 62.

In FIG. 10a, semiconductor die 32 is shown with contact pads 38 connected to metal vias 64 by traces 52. FIG. 10b is a cross-sectional view of die 32, taken along line 10b-10b, showing a metal via on saw street configuration, as produced by the manufacturing steps of FIGs. 1-9. Solder bumps or balls 72 are formed on RDL 58.

In FIG. 11a, semiconductor die 32 is shown with contact pads 38 connected to metal vias 80 by traces 52. FIG. 11b is a cross-sectional view of die 32, taken along line 11b-11b, showing metal vias 80 along saw street 36. The metal

full-circle vias are produced by the steps described in FIGs. 1-9, with the exception that two via holes like 50 are formed side-by-side in organic material 48. The side-by-side via holes 50 are separated by organic material 48. Conductive traces 52 connect contact pads 38 and via holes 50. The side-by-side via holes are filled with conductive material to form metal vias 80.

In FIG. 12a, semiconductor die 32 is shown with contact pads 38 connected to metal vias 80 by traces 52. Dicing tape is applied to the back of semiconductor wafer 30 for structural support of the wafer during the final singulation to separate die 32, as shown in FIG. 12b which is a cross-sectional view taken along line 12b-12b. The second or final singulation to separate the plurality of die 32 is cut through organic material 48 along line 82 between the side-by-side vias 80 with a cutting tool like 70. The singulation between the vias 80 results in the metal vias on saw street configuration.

In FIG. 13a, semiconductor die 32 is shown with contact pads 38 connected to metal vias 80 by traces 52. FIG. 13b is a cross-sectional view of die 32, taken along line 13b-13b, showing a metal via on saw street configuration. The metal full-circle vias are produced by the steps described in FIGs. 1-9 and 11-12. The side-by-side via holes like 50 are separated by organic material 48. Conductive traces like 52 connect the contact pads and via holes. The side-by-side via holes are filled with conductive material to form metal vias 80. The final singulation to separate the plurality of die 32 is cut through organic material 48 between the side-by-side metal vias 80 resulting in the metal vias on saw street configuration.

FIG. 14 illustrates direct die-to-die stacking using direct via metal bonding. A plurality of die 32 is stacked as

shown to suit a particular application. Each of the metal half-vias 64 can be joined together as shown by union 90 using a direct via metal bonding process or solder paste. Alternately, semiconductor die 32 with metal full-vias 80 can be joined together by union 90 using a direct via metal bonding process or solder paste. The top semiconductor die is shown stacked in the inverted position to make use of backside RDL 58 for interconnect to other devices and packages (not shown). RDL 58 is separated and electrically isolated by repassivation layer 60. The bottom semiconductor die 32 has solder bumps 72 formed on RDL 58 separated by repassivation layers 60 for electrical isolation. The backside RDL 58 provides intermediate interconnect from solder bumps 72 to the active surface of the bottom semiconductor die 32. The interconnection between RDLs in the die-to-die stacking can be used with or without solder bumps 72.

In FIGs. 15-18 shows various packaging applications using, in part, an interconnect technique with the THVs formed on saw streets with backside RDLs. FIG. 15 has semiconductor die 100 connecting through solder bumps 102 to backside RDL 58 on die 32. Backside RDL 58 electrically connect to active circuits on die 32, as well as providing interconnect to die 100. Die 32 is supported by substrate 104. Contact pads 38 and/or metal vias 64 or 80 electrically connect to solder bumps 106 through conductive layer 108. The packages are sealed by epoxy encapsulant 110.

FIG. 16 shows semiconductor die 120 electrically connected to contact pad 38 and metal vias 64 or 80 through bond wires 122 and conductive layer 124. Backside RDL 58 electrically connects to active circuits on die 32 and solder bumps 126, which in turn electrically connect to solder bumps 128 through conductive layer 130. Die 32 is supported by substrate 132. The packages are sealed by epoxy encapsulant

134. An underfill material 136 can be used for stress relief.

FIG. 17 shows semiconductor die 140 electrically connected through bond wires 142 to backside RDL 58 of semiconductor die 32. Backside RDL 58 electrically connect to active circuits on die 32, as well as providing interconnect to die 140. Passive devices 144 also connect to backside RDL 58 with solder paste 146. Metal vias 64 electrically connect to solder bumps 145 through conductive layer 147. Die 32 is supported by substrate 148. The packages are sealed by epoxy encapsulant 149.

FIG. 18 shows semiconductor die 150 electrically connected to metal vias 64 or 80 by way of bond wires 152. Solder bumps 154 electrically connect the backside of RDL 58 to conductive layer 156, which connect semiconductor die 160 with solder bumps 162 by way of bond wires 164, bond wires 166, and conductive layer 168. Die 32 is supported by substrate 170. The packages are encased by epoxy encapsulant 172. An underfill material 174 can be used for stress relief.

In summary, stackable semiconductor die has been described with THVs formed in the saw streets. The semiconductor die use a redistribution layer, separated by a repassivation layer, to increase signal routing options and density. The RDL, in addition to the THV, provides more signal routing functionality and flexibility within the package.

While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims

Claims

What is claimed:

1. A method of making a semiconductor device, comprising:

providing a plurality of semiconductor die with a plurality of contact pads disposed over a first surface of the semiconductor die;

forming a trench between the semiconductor die;

depositing an insulating material in the trench;

forming a plurality of conductive vias through the insulating material;

forming a plurality of conductive traces over the first surface electrically connecting a first portion of the conductive vias to the contact pads;

forming a redistribution layer (RDL) over a second surface of the semiconductor die opposite the first surface, the RDL extending across the second surface of the semiconductor die to route electrical signals to areas on the second surface including a central region of the semiconductor die, wherein a second portion of the conductive vias is electrically isolated from the conductive traces; and

forming a repassivation layer over the second surface of the semiconductor die for electrical isolation between portions of the RDL.

2. The method of claim 1, further including expanding a space between the semiconductor die to increase a width of the trench.

3. The method of claim 1, further including singulating the semiconductor device through the conductive vias to separate the semiconductor die.

4. The method of claim 1, further including forming the conductive vias side-by-side in the insulating material.

5. The method of claim 1, further including singulating the semiconductor device between the conductive vias to separate the semiconductor die.

6. The method of claim 1, further including:

stacking a plurality of semiconductor die; and

electrically connecting the stacked semiconductor die through the RDL and conductive vias.

7. A method of making a semiconductor device, comprising:

providing a plurality of semiconductor die with a plurality of contact pads disposed over a first surface of the semiconductor die;

depositing an insulating material around the semiconductor die;

forming a plurality of conductive vias through the insulating material;

forming a plurality of conductive traces over the first surface electrically connecting a first portion of the conductive vias to the contact pads;

forming a redistribution layer (RDL) over a second surface of the semiconductor die opposite the first surface, wherein a first portion of the RDL is electrically connected to the conductive vias and a second portion of the RDL is electrically isolated from the conductive vias; and

forming a repassivation layer over the second surface of the semiconductor die for electrical isolation between portions of the RDL.

8. The method of claim 7, wherein a second portion of the conductive vias is electrically isolated from the conductive traces.

9. The method of claim 7, wherein the RDL extends across the second surface of the semiconductor die to route electrical signals to areas on the second surface including a central region of the semiconductor die.

10. The method of claim 7, further including singulating the semiconductor device through the conductive vias to separate the semiconductor die.

11. The method of claim 7, further including forming the conductive vias side-by-side in the insulating material.

12. The method of claim 7, further including singulating the semiconductor device between the conductive vias to separate the semiconductor die.

13. The method of claim 7, further including:

stacking a plurality of semiconductor die; and

electrically connecting the stacked semiconductor die through the RDL and conductive vias.

14. A method of making a semiconductor device, comprising:

providing a plurality of semiconductor die;

depositing an insulating material around the semiconductor die;

forming a plurality of conductive vias through the insulating material;

forming a plurality of conductive traces over a first surface of the semiconductor die electrically connecting the

conductive vias to contact pads of the semiconductor die; and

forming a redistribution layer (RDL) over a second surface of the semiconductor die opposite the first surface, wherein a first portion of the RDL is electrically connected to the conductive vias.

15. The method of claim 14, further including forming a repassivation layer over the second surface of the semiconductor die for electrical isolation between portions of the RDL.

16. The method of claim 14, wherein a second portion of the RDL is electrically isolated from the conductive vias.

17. The method of claim 14, wherein the RDL extends across the second surface of the semiconductor die to route electrical signals to areas on the second surface.

18. The method of claim 14, further including singulating the semiconductor device through or between the conductive vias to separate the semiconductor die.

19. The method of claim 14, further including:

stacking a plurality of semiconductor die; and

electrically connecting the stacked semiconductor die through the RDL and conductive vias.

20. A method of making a semiconductor device, comprising:

providing a plurality of semiconductor die;

depositing an insulating material around the semiconductor die;

forming a plurality of conductive vias through the insulating material;

forming a plurality of conductive traces over a first surface of the semiconductor die; and

forming a redistribution layer (RDL) over a second surface of the semiconductor die opposite the first surface, wherein a first portion of the RDL is electrically connected to the conductive vias.

21. The method of claim 20, further including forming a repassivation layer over the second surface of the semiconductor die for electrical isolation between portions of the RDL.

22. The method of claim 20, wherein a second portion of the RDL is electrically isolated from the conductive vias.

23. The method of claim 20, wherein the RDL extends across the second surface of the semiconductor die to route electrical signals to areas on the second surface.

24. The method of claim 20, further including singulating the semiconductor device through or between the conductive vias to separate the semiconductor die.

25. The method of claim 20, further including:

stacking a plurality of semiconductor die; and

electrically connecting the stacked semiconductor die through the RDL and conductive vias.